

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD4004 ChipCorder series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD4004 Series Product Summary table on the second page to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

DURATION

To meet end system requirements, the ISD4004 series products are single-chip solutions at 8, 10, 12, 16 minutes.

FLASH STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded (typically) over 100,000 times.

MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO, \overline{SS}) SPI interface is provided for ISD4004 control and addressing functions. The ISD4004 is configured to operate as a peripheral slave device, with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers occurs through this SPI interface. An interrupt signal (INT) and internal read-only Status Register are provided for handshake purposes.

PROGRAMMING

The ISD4004 series is also ideal for playback-only applications, where single or multiple message Playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA} , V_{CCD})

To minimize noise, the analog and digital circuits in the ISD4004 devices use separate power busses. These +3 V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA} , V_{SSD})

The ISD4004 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 Ω . The backside of the die is connected to V_{SS} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SS} or left floating.

Figure 1: ISD4004 Series TSOP and PDIP/SOIC Pinouts

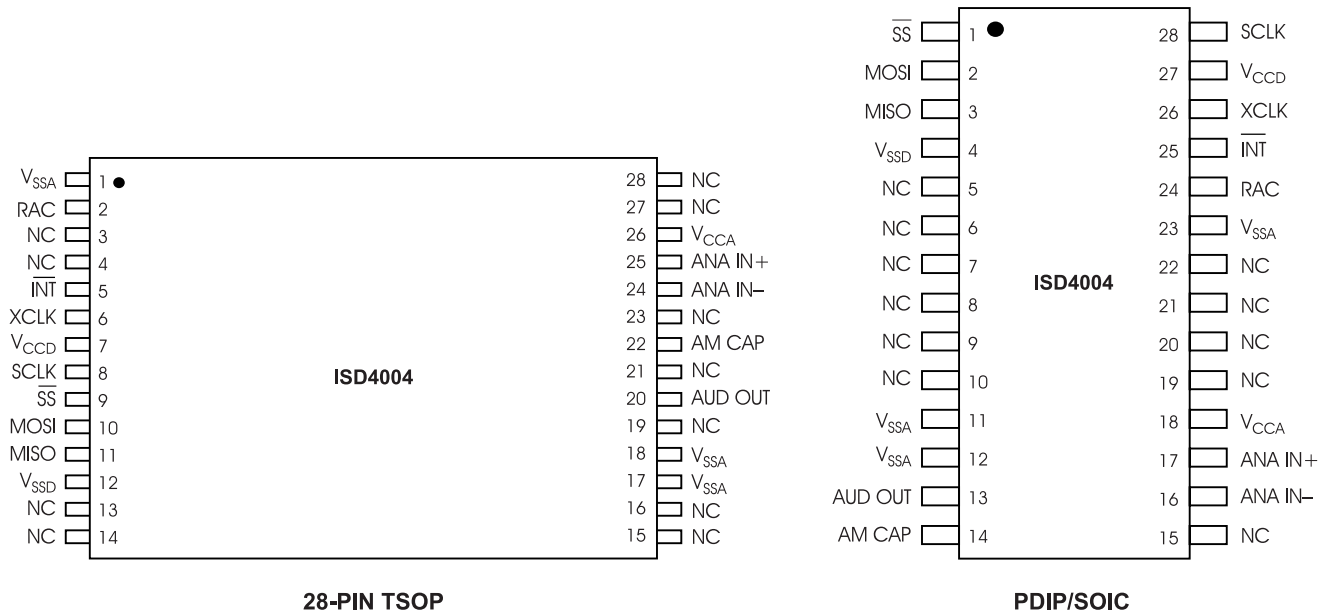
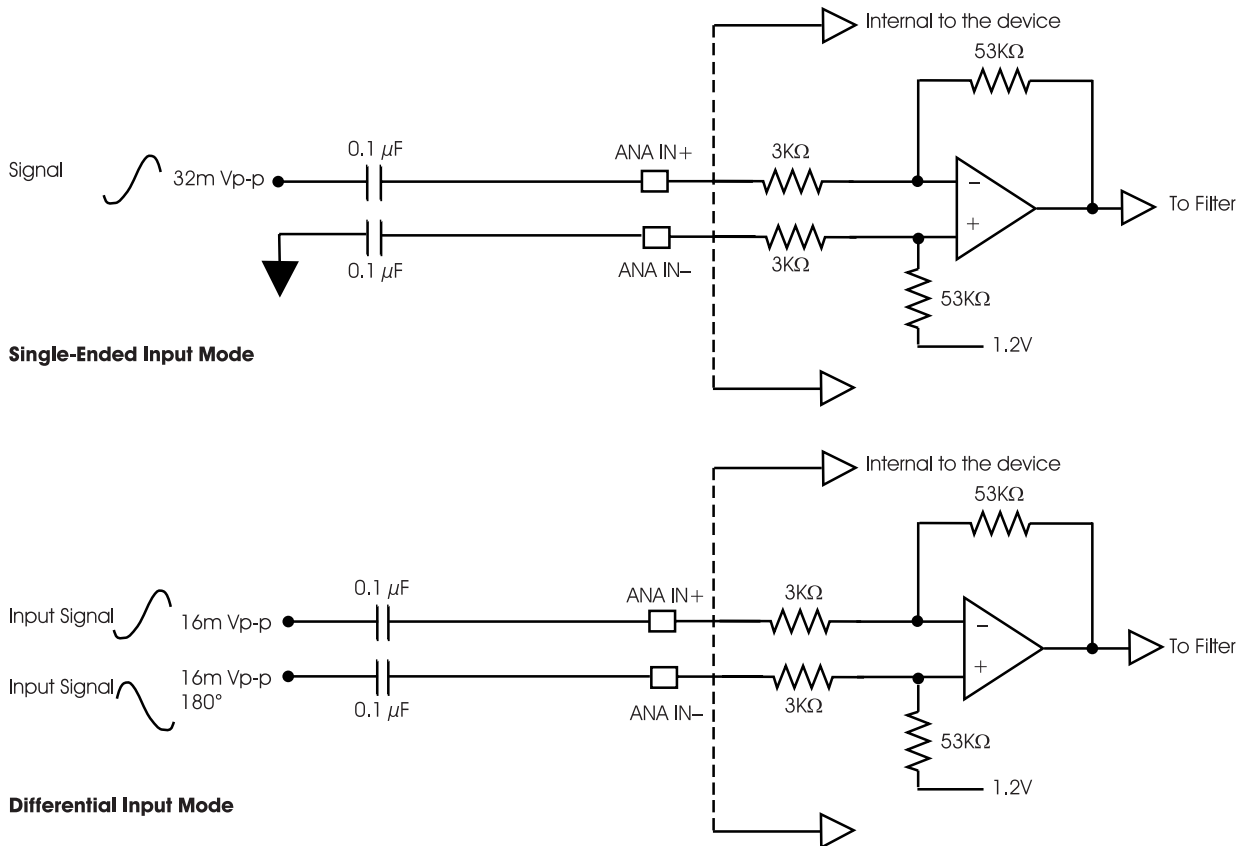


Figure 2: ISD4004 Series ANA IN Modes



NON-INVERTING ANALOG INPUT (ANA IN+)

This pin is the non-inverting analog input that transfers the signal to the device for recording. The analog input amplifier can be driven single ended or differentially. In the single-ended input mode, a 32 mVp-p (peak-to-peak) maximum signal should be capacitively connected to this pin for optimal signal quality. This capacitor value, together with the 3 K Ω input impedance of ANA IN+, is selected to give cutoff at the low frequency end of the voice passband. In the differential-input mode, the maximum input signal at ANA IN+ should be 16 mVp-p for optimal signal quality. The circuit connections for the two modes are shown in Figure 2 on page 2.

INVERTING ANALOG INPUT (ANA IN-)

This pin is the inverting analog input that transfers the signal to the device for recording in the differential-input mode. In this differential-input mode, a 16 mVp-p maximum input signal at ANA IN- should be capacitively coupled to this pin for optimal signal quality as shown in the ISD4004 Series ANA IN Modes, Figure 2. This capacitor value should be equal to the coupling capacitor used on the ANA IN+ pin. The input impedance at ANA IN- is nominally 56 K Ω . In the single-ended mode, ANA IN- should be capacitively coupled to V_{SSA} through a capacitor equal to that used on the ANA IN+ input.

AUDIO OUTPUT (AUD OUT)

This pin provides the audio output to the user. It is capable of driving a 5 K Ω impedance. It is recommended that this pin be AC coupled.

NOTE *The AUDOUT pin is always at 1.2 volts when the device is powered up. When in playback, the output buffer connected to this pin can drive a load as small as 5 K Ω . When in record, a resistor connects AUDOUT to the internal 1.2 volt analog ground supply. This resistor is approximately 850 K Ω , but will vary somewhat according to the sample rate of the device. This relatively high impedance allows this pin to be connected to an audio bus without loading it down.*

SLAVE SELECT (\overline{SS})

This input, when LOW, will select the ISD4004 device.

MASTER OUT SLAVE IN (MOSI)

This is the serial input to the ISD4004 device. The master microcontroller places data on the MOSI line one half-cycle before the rising clock edge to be clocked in by the ISD4004 device.

MASTER IN SLAVE OUT (MISO)

This is the serial output of the ISD4004 device. This output goes into a high-impedance state if the device is not selected.

SERIAL CLOCK (SCLK)

This is the clock input to the ISD4004. It is generated by the master device (microcontroller) and is used to synchronize data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD4004 on the rising edge of SCLK and shifted out of the device on the falling edge of SCLK.

INTERRUPT (\overline{INT})

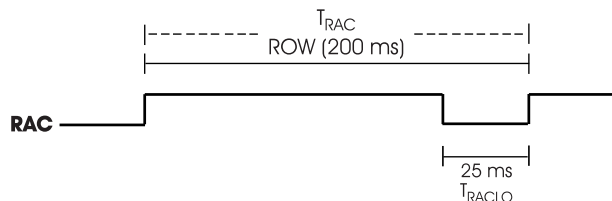
The ISD4004 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. This is an open drain output pin. Each operation that ends in an EOM or Overflow will generate an interrupt including the message cueing cycles. The interrupt will be cleared the next time an SPI cycle is initiated. The interrupt status can be read by an RINT instruction.

Overflow Flag (OVF)—The Overflow flag indicates that the end of the ISD4004's analog memory has been reached during a record or playback operation.

End of Message (EOM)—The End-of-Message flag is set only during playback operation when an EOM is found. There are eight EOM flag position options per row.

ROW ADDRESS CLOCK (RAC)

This is an open drain output pin that provides a signal with a 200 ms period at the 8 KHz sampling frequency. (This represents a single row of memory and there are 2400 rows of memory in the ISD4004 series devices.) This signal stays HIGH for 175 ms and stays LOW for 25 ms when it reaches the end of a row.



The RAC pin stays HIGH for 109.38 μ sec and stays LOW for 15.63 μ sec in Message Cueing mode (see page 5 for a more detailed description of Message Cueing). Refer to the AC Parameters table for RAC timing information on other sample rate products.

When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period. This is due to the need to load sample and hold circuits internal to the device. This pin can be used for message management techniques.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD4004 products has an internal pull-down device. These products are configured at the factory with an internal sampling clock frequency centered to ± 1 percent of specification. The frequency is then maintained to a variation over the entire commercial temperature and operating voltage ranges as defined by the minimum/maximum limits in the applicable AC Parameters table. The internal clock has a tolerance, over the extended temperature, industrial temperature and voltage ranges as defined by the minimum/maximum limits in the applicable AC Parameters table. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin in Table 1.

Table 1: External Clock Input Clocking Table

Part Number	Sample Rate	Required Clock
ISD4004-08M	8.0 KHz	1024 KHz
ISD4004-10M	6.4 KHz	819.2 KHz
ISD4004-12M	5.3 KHz	682.7 KHz
ISD4004-16M	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed. Thus, aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **If the XCLK is not used, this input should be connected to ground.**

AUTOMUTE™ FEATURE (AM CAP)

This pin is used in controlling the AutoMute feature. The AutoMute feature attenuates the signal when it drops below an internally set threshold. This helps to eliminate noise (with 6 dB of attenuation) when there is no signal (i.e., during periods of silence). A 1 μ F capacitor to ground should be connected to the AM CAP pin. This capacitor becomes a part of an internal peak detector which senses the signal amplitude (peak). This peak level is compared to an internally set threshold to determine the AutoMute trip point. For large signals the AutoMute attenuation is set to 0 dB while 6 dB of attenuation occurs for silence. The 1 μ F capacitor also affects the rate at which the AutoMute feature changes with the signal amplitude (or the attack time). The Automute feature can be disabled by connecting the AM CAP pin to V_{CCA} .

SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD4004 series operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD4004, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of \overline{SS} pin.
2. \overline{SS} is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and Record operations are initiated by enabling the device by asserting the \overline{SS} pin LOW, shifting in an opcode and an address field to the ISD4004 device (refer to the Opcode Summary on the page 6).
5. The opcodes and address fields are as follows: <8 control bits> and <16 address bits>.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is initiated.

7. As Interrupt data is shifted out of the ISD4004 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. An operation begins with the RUN bit set and ends with the RUN bit reset.
9. All operations begin with the rising edge of \overline{SS} .

MESSAGE CUEING

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 1600 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message.

Table 2: Opcode Summary

Instruction	Opcode <8 bits> Address <16 bits>	Operational Summary
POWERUP	00100XXX	Power-Up: Device will be ready for an operation after T_{PUD} .
SETPLAY	11100XXX <A15-A0>	Initiates Playback from address <A15-A0>.
PLAY	11110XXX	Playback from the current address (until EOM or OVF).
SETREC	10100XXX <A15-A0>	Initiates a Record operation from address <A15-A0>.
REC	10110XXX	Records from current address until OVF is reached.
SETMC	11101XXX <A15-A0>	Initiates Message Cueing (MC) from address <A15-A0>.
MC ¹	11111XXX	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if no more messages are present.
STOP	0X110XXX	Stops current operation.
STOPWRDN	0X01XXXX	Stops current Operation and enters stand-by (power-down) mode.
RINT ²	0X110XXX	Read Interrupt status bits: Overflow and EOM.

1. Message Cueing can be selected only at the beginning of a play operation.
2. As the Interrupt data is shifted out of the ISD4004, control and address data is being shifted in. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation at the same time. See Figure 5 through Figure 8 for Opcode format.

POWER-UP SEQUENCE

The ISD4004 will be ready for an operation after T_{PUD} (25 ms approximately for 8 KHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programming cycle should be used.

Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send SETPLAY command with address 00.
4. Send PLAY command.

The device will start playback at address 00 and it will generate an interrupt when an EOM is reached. It will then stop playback.

Record Mode

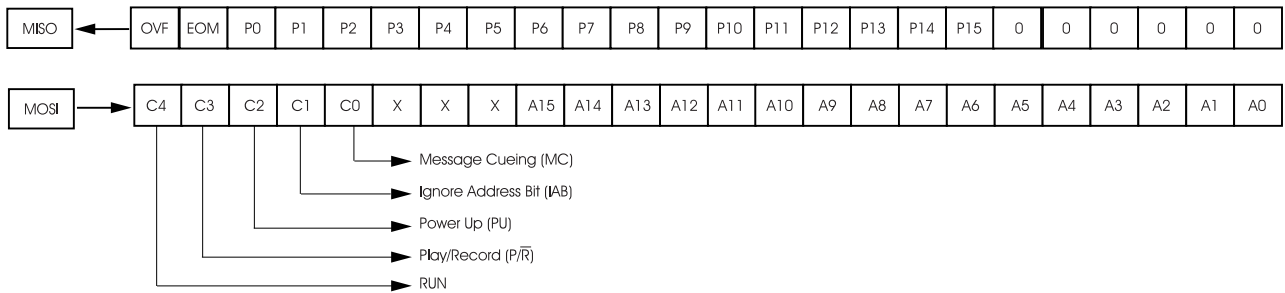
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send POWERUP command.
4. Send SETREC command with address 00.
5. Send REC command.

The device will start recording at address 00 and it will generate an interrupt when an overflow is reached (end of memory array). It will then stop recording.

SPI PORT

The following diagram describes the SPI port and the control bits associated with it.

Figure 3: SPI Port



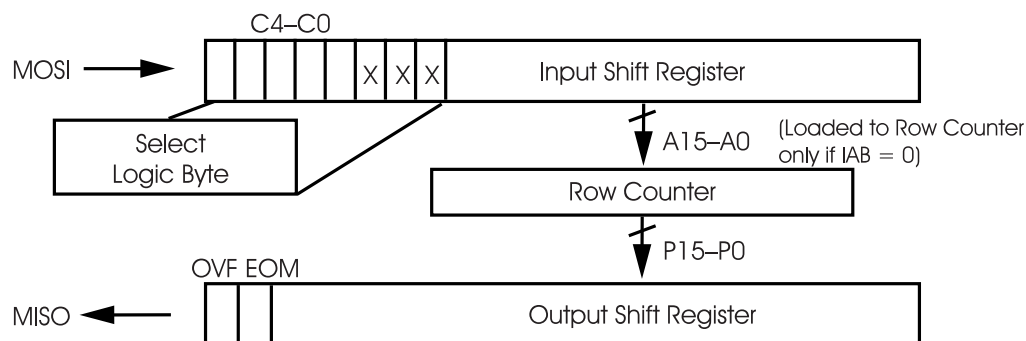
SPI CONTROL REGISTER

The SPI control register provides control of individual device functions such as Play, Record, Message Cueing, Power-Up and Power-Down, Start and Stop operations, and Ignore Address pointers.

Table 3: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN	= 1 = 0	Enable or Disable an operation Start Stop	PU	= 1 = 0	Master power control Power-Up Power-Down
P/R	= 1 = 0	Selects Play or Record operation Play Record	IAB	= 1 = 0	Ignore address control bit Ignore input address register (A15–A0) Use the input address register contents for an operation (A15–A0)
MC	= 1 = 0	Enable or Disable Message Cueing Enable Message Cueing Disable Message Cueing	P15–P0		Output of the row pointer register
			A15–A0		Input address register

Figure 4: SPI Interface Simplified Block Diagram

Table 4: Absolute Maximum Ratings (Packaged Parts)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V _{SS} - 0.3 V) to (V _{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V _{SS} - 1.0 V) to (V _{CC} + 1.0 V)
Lead temperature (soldering - 10 seconds)	300°C
V _{CC} - V _{SS}	-0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range ⁽¹⁾	0°C to +70°C
Extended operating temperature ⁽¹⁾	-20°C to +70°C
Industrial operating temperature ⁽¹⁾	-40°C to +85°C
Supply voltage (V _{CC}) ⁽²⁾	+2.7 V to +3.3 V
Ground voltage (V _{SS}) ⁽³⁾	0 V

1. Case temperature.
2. V_{CC} = V_{CCA} = V_{CCD}.
3. V_{SS} = V_{SSA} = V_{SSD}.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8			V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 10 μA
V _{OL1}	RAC, $\overline{\text{INT}}$ Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} - 0.4			V	I _{OH} = -10 μA
I _{CC}	V _{CC} Current (Operating) — Playback — Record		15 25	30 40	mA	R _{EXT} = ∞ ⁽³⁾ R _{EXT} = ∞ ⁽³⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	⁽³⁾ ⁽⁴⁾
I _{IL}	Input Leakage Current			±1	μA	
I _{HZ}	MISO Tristate Current		1	10	μA	
R _{EXT}	Output Load Impedance	5			KΩ	
R _{ANA IN+}	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
R _{ANA IN-}	ANA IN- Input Resistance	40	56	71	KΩ	
A _{ARP}	ANA IN+ or ANA IN- to AUD OUT Gain		25		dB	⁽⁵⁾

1. Typical values: T_A = 25°C and 3.0 V.

2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.

3. V_{CCA} and V_{CCD} connected together.

4. $\overline{\text{SS}} = \text{VCCA} = \text{VCCD}$, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.

5. Measured with AutoMute feature disabled.

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD4004-08M	8.0		KHz	⁽⁵⁾
		ISD4004-10M	6.4		KHz	⁽⁵⁾
		ISD4004-12M	5.3		KHz	⁽⁵⁾
		ISD4004-16M	4.0		KHz	⁽⁵⁾
F _{CF}	Filter Pass Band	ISD4004-08M	3.4		KHz	3-dB Roll-Off Point ⁽³⁾ ⁽⁷⁾
		ISD4004-10M	2.7		KHz	3-dB Roll-Off Point ⁽³⁾ ⁽⁷⁾
		ISD4004-12M	2.3		KHz	3-dB Roll-Off Point ⁽³⁾ ⁽⁷⁾
		ISD4004-16M	1.7		KHz	3-dB Roll-Off Point ⁽³⁾ ⁽⁷⁾
T _{REC}	Record Duration	ISD4004-08M	8		min	⁽⁶⁾
		ISD4004-10M	10		min	⁽⁶⁾
		ISD4004-12M	12		min	⁽⁶⁾
		ISD4004-16M	16		min	⁽⁶⁾

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
T _{PLAY}	Playback Duration	ISD4004-08M		8		min	
		ISD4004-10M		10		min	
		ISD4004-12M		12		min	
		ISD4004-16M		16		min	
T _{PUD}	Power-Up Delay	ISD4004-08M		25		msec	
		ISD4004-10M		31.25		msec	
		ISD4004-12M		37.5		msec	
		ISD4004-16M		50		msec	
T _{STOP} or T _{PAUSE}	Stop or Pause in Record or Play	ISD4004-08M		50		msec	
		ISD4004-10M		62.5		msec	
		ISD4004-12M		75		msec	
		ISD4004-16M		100		msec	
T _{RAC}	RAC Clock Period	ISD4004-08M		200		msec	⁽⁹⁾
		ISD4004-10M		250		msec	⁽⁹⁾
		ISD4004-12M		300		msec	⁽⁹⁾
		ISD4004-16M		400		msec	⁽⁹⁾
T _{RACLO}	RAC Clock Low Time	ISD4004-08M		25		msec	
		ISD4004-10M		31.25		msec	
		ISD4004-12M		37.5		msec	
		ISD4004-16M		50		msec	
T _{RACM}	RAC Clock Period in Message Cueing Mode	ISD4004-08M		125		μsec	
		ISD4004-10M		156.3		μsec	
		ISD4004-12M		187.5		μsec	
		ISD4004-16M		250		μsec	
T _{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD4004-08M		15.63		μsec	
		ISD4004-10M		19.53		μsec	
		ISD4004-12M		23.44		μsec	
		ISD4004-16M		31.25		μsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V _{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak ⁽⁴⁾ ⁽⁷⁾ ⁽⁸⁾

1. Typical values: $T_A = 25^\circ\text{C}$ and 3.0 V.
2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).
4. Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN- is 16mVp-p.
5. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6dB drop by nature of passing through both filters.
7. The typical output voltage will be approximately 570mVp-p with V_{IN} at 32mVp-p.
8. For optimal signal quality, this maximum limit is recommended.
9. When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.

Table 8: Absolute Maximum Ratings (Die)⁽¹⁾

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V _{SS} - 0.3 V) to (V _{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V _{SS} - 1.0 V) to (V _{CC} + 1.0 V)
V _{CC} - V _{SS}	-0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V _{CC}) ⁽¹⁾	+2.7 V to +3.3 V
Ground voltage (V _{SS}) ⁽²⁾	0 V

1. V_{CC} = V_{CCA} = V_{CCD}

2. V_{SS} = V_{SSA} = V_{SSD}.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
V _{IL}	Input Low Voltage			V _{CC} × 0.2	V	
V _{IH}	Input High Voltage	V _{CC} × 0.8			V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 10 μA
V _{OL1}	RAC, INT Output Low Voltage			0.4	V	I _{OL} = 1 mA
V _{OH}	Output High Voltage	V _{CC} - 0.4			V	I _{OH} = -10 μA
I _{CC}	V _{CC} Current (Operating) — Playback — Record		15 25	30 40	mA	R _{EXT} = ∞ ⁽³⁾ R _{EXT} = ∞ ⁽³⁾
I _{SB}	V _{CC} Current (Standby)		1	10	μA	⁽³⁾ ⁽⁴⁾
I _{IL}	Input Leakage Current			±1	μA	
I _{HZ}	MISO Tristate Current		1	10	μA	
R _{EXT}	Output Load Impedance	5			KΩ	
R _{ANA IN+}	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
R _{ANA IN-}	ANA IN- Input Resistance	40	56	71	KΩ	
A _{ARP}	ANA IN+ or ANA IN- to AUDOUT Gain		25		dB	⁽⁵⁾

1. Typical values: T_A = 25°C and 3.0 V.

2. All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.

3. V_{CCA} and V_{CCD} connected together.

4. SS = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.

5. Measured with AutoMute feature disabled.

Table 11: AC Parameters (Die)

Symbol	Characteristic	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units	Conditions
F _S	Sampling Frequency	ISD4004-08M	8.0		KHz	(5)
		ISD4004-10M	6.4		KHz	(5)
		ISD4004-12M	5.3		KHz	(5)
		ISD4004-16M	4.0		KHz	(5)
F _{CF}	Filter Pass Band	ISD4004-08M	3.4		KHz	3dB Roll-Off Point ⁽³⁾ (⁶)
		ISD4004-10M	2.7		KHz	3dB Roll-Off Point ⁽³⁾ (⁶)
		ISD4004-12M	2.3		KHz	3dB Roll-Off Point ⁽³⁾ (⁶)
		ISD4004-16M	1.7		KHz	3dB Roll-Off Point ⁽³⁾ (⁶)
T _{REC}	Record Duration	ISD4004-08M	8		min	(5)
		ISD4004-10M	10		min	(5)
		ISD4004-12M	12		min	(5)
		ISD4004-16M	16		min	(5)
T _{PLAY}	Playback Duration	ISD4004-08M	8		min	(5)
		ISD4004-10M	10		min	(5)
		ISD4004-12M	12		min	(5)
		ISD4004-16M	16		min	(5)
T _{PUD}	Power-Up Delay	ISD4004-08M	25		msec	
		ISD4004-10M	31.25		msec	
		ISD4004-12M	37.5		msec	
		ISD4004-16M	50		msec	
T _{STOP} or T _{PAUSE}	Stop or Pause in Record or Play	ISD4004-08M	50		msec	
		ISD4004-10M	62.5		msec	
		ISD4004-12M	75		msec	
		ISD4004-16M	100		msec	
T _{RAC}	RAC Clock Period	ISD4004-08M	200		msec	(9)
		ISD4004-10M	250		msec	(9)
		ISD4004-12M	300		msec	(9)
		ISD4004-16M	400		msec	(9)
T _{RACLO}	RAC Clock Low Time	ISD4004-08M	25		msec	
		ISD4004-10M	31.25		msec	
		ISD4004-12M	37.5		msec	
		ISD4004-16M	50		msec	
T _{RACM}	RAC Clock Period in Message Cueing Mode	ISD4004-08M	125		μsec	
		ISD4004-10M	156.3		μsec	
		ISD4004-12M	187.5		μsec	
		ISD4004-16M	250		μsec	
T _{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD4004-08M	15.63		μsec	
		ISD4004-10M	19.53		μsec	
		ISD4004-12M	23.44		μsec	
		ISD4004-16M	31.25		μsec	

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