OKI

MSM9562/63/66/67

User's Manual

IC for FM Multiplex Demodulation

Preliminary

[Control Flow]

Oki Electric Industry Co., Ltd.

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CONTENTS

MSM9562/63/66/67 Control Flow

1. Modes

1.1 Operating Modes

This IC has three reception modes.

(1) A main channel mode (conventional method) that continuously receives data from a single broadcast station and outputs the received data in units of packets and frames

(2) A sub-channel mode that receives data by switching a tuner at high-speed between one broadcast station (main station) and another broadcast station (sub-station), and outputs the sub-station receive data in packet units
(During sub-station reception, missing main station packets can be regenerated by error correction. Therefore, by watching for missing packets, simultaneous reception of the main station and sub-station is possible.)

(3) A page mode that writes the 1st horizontal receive data to frame memory and outputs the collective packets receive during a specific time interval

Figures 1.1 to 1.3 show the receive operation of each receive mode.

Applications of the sub-channel mode include simultaneous reception an FM multiplexed broadcast program on one channel and packet data on another channel.
The page mode can be applied to pager or high-speed broadcast program verification.

Each mode can be switched to another mode.

1.2 Frame Format

This IC fully supports international standard frame formats A0, A1, B (Japan) and C. High-speed switching of each frame format is also possible.

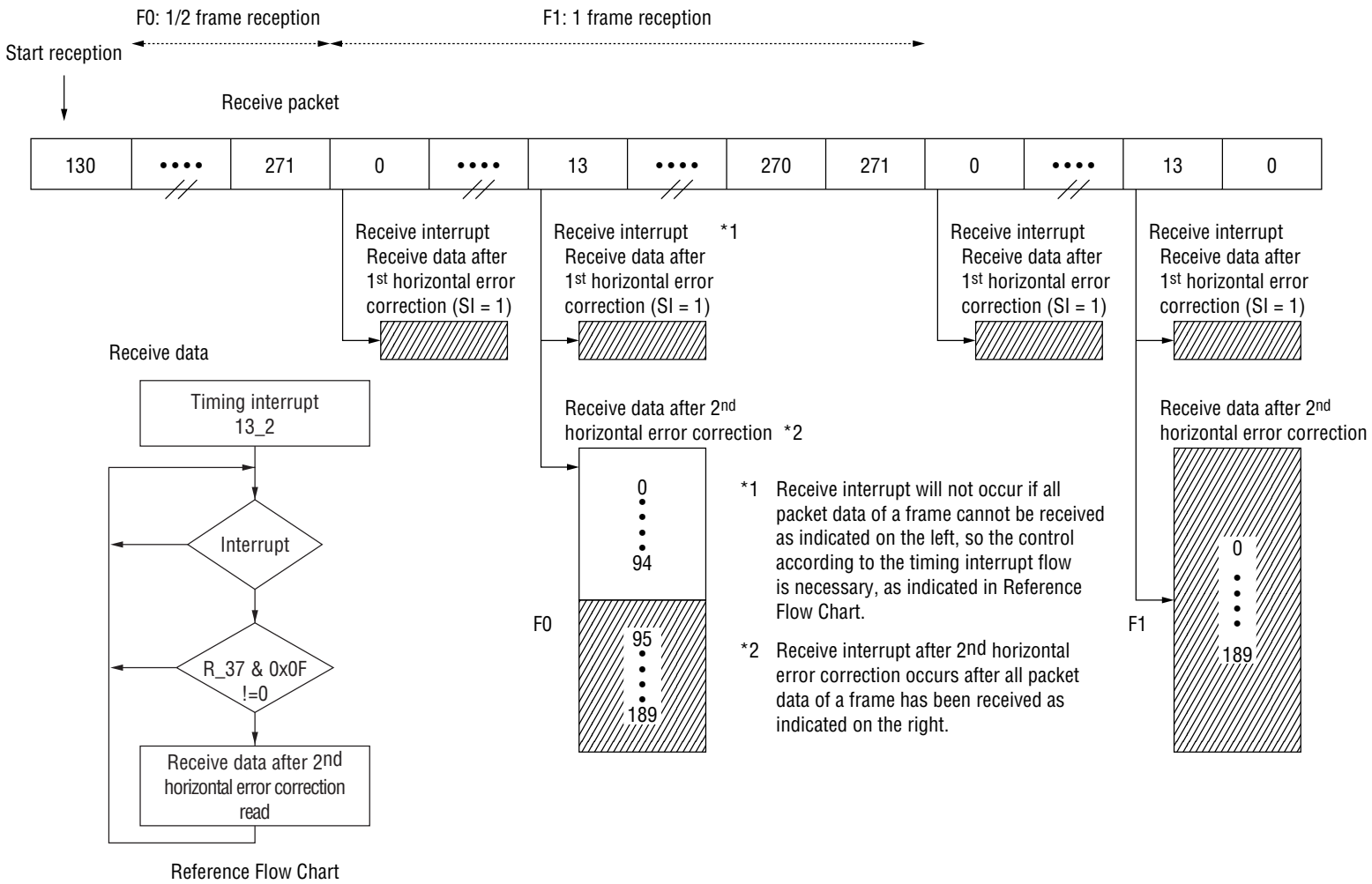


Figure 1.1 Main Channel Mode Reception
(Case where only SI = 1 at reception after the first horizontal error correction)

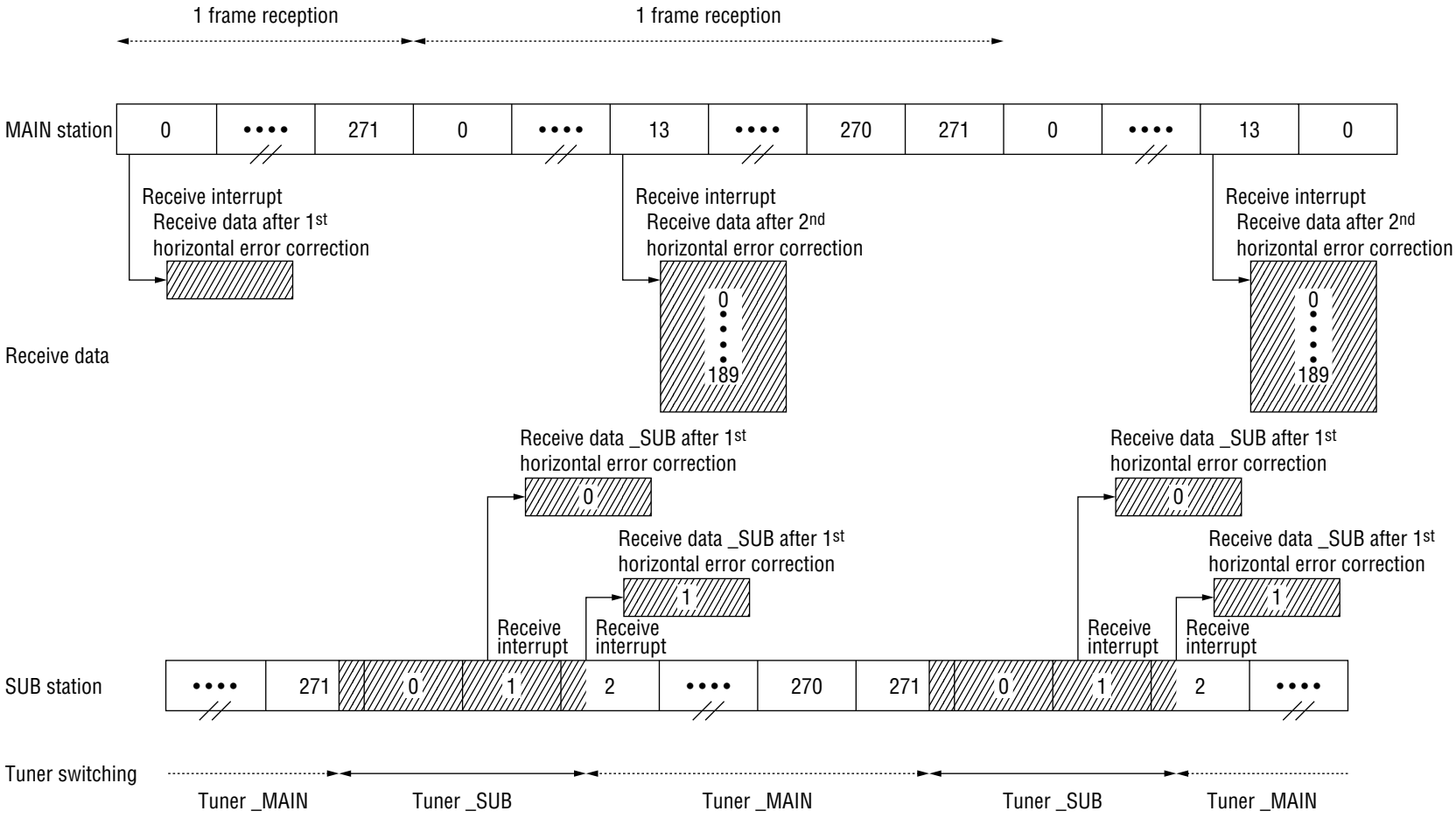


Figure 1.2 Switched Reception Between Main Channel Mode and Sub-Channel Mode

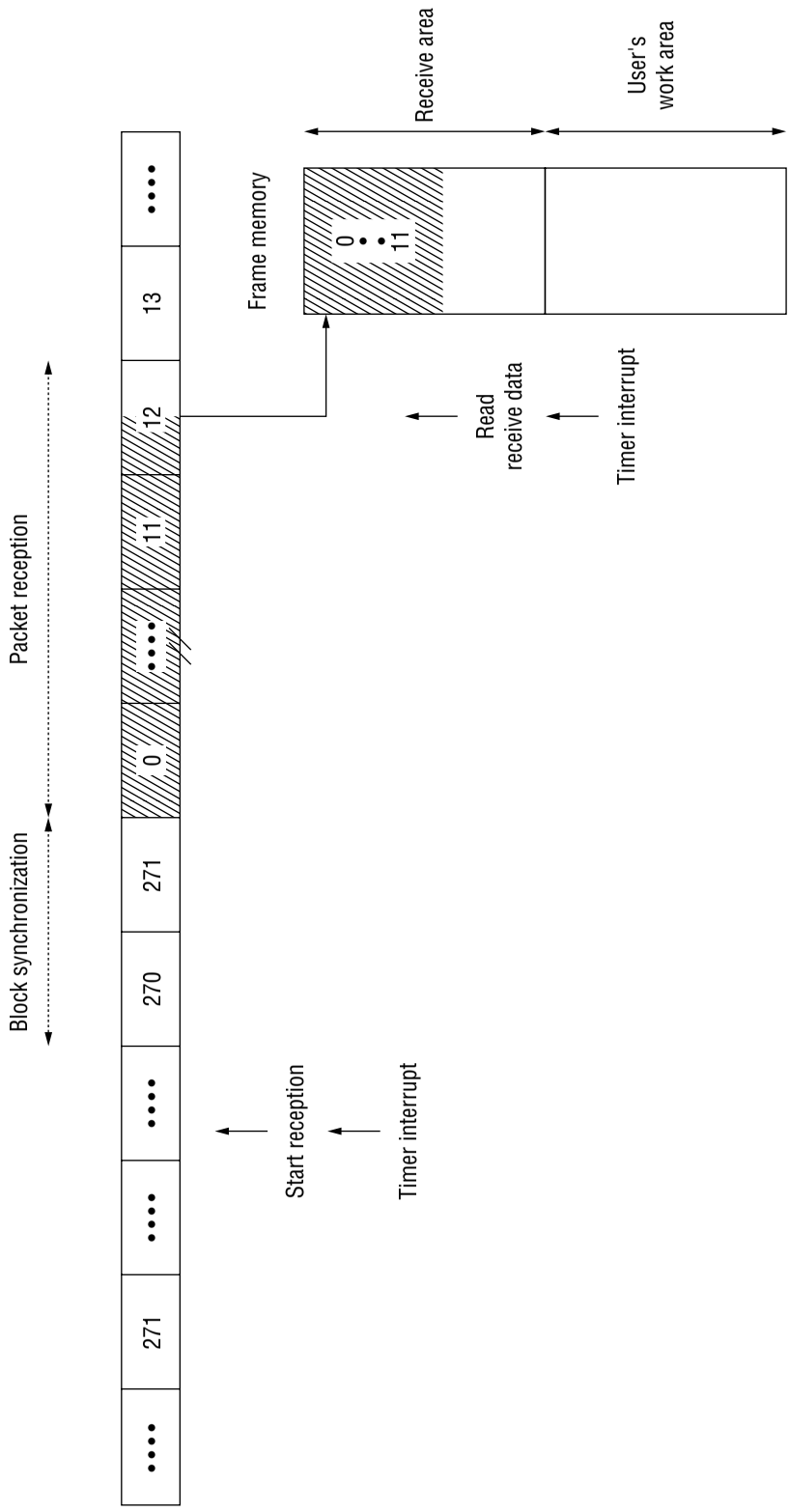


Figure 1.3 Page Mode Reception

2. Control Flow Examples

2.1 Normal Reception

This flow example indicates the control flow of receive _MAIN after the 1st horizontal error correction, and of reception after the 2nd horizontal error correction.

2.1.1 Total Flow

Figure 2.1.1 shows the total flow.
The total flow can be changed by the following three controls.
• Power-on/receive start (power-on 2/receive start 3)
• Switching the MAIN channel
• Halting operation

2.1.2 Total Configuration

Figure 2.1.2 shows the total configuration.
This figure shows the total flow control and the function of interrupts.

Controls that manage the total flow such as MAIN reception or halting operation are executed from the main program. It is not necessary to synchronize these controls with the IC.

The transfer of receive data (layer 3 data) after the 2nd horizontal error correction or receive _MAIN data after the 1st horizontal error correction to the USR_RAM, modification and display of this receive data, display of the synchronous state of the FM multiplexing IC, etc. are performed by interrupt control. This control must be synchronized with an IC interrupt.

2.1.3 Interrupts

Figure 2.1.3 shows the flow of interrupt processing.

2.1.4 User RAM Configuration

Figure 2.1.4 shows the configuration of user RAM and table 2.1.4 shows the contents of user RAM utilized in this flow.

Table 2.1.4 User RAM Contents

1	(R_00)	Content of interrupt register R_00 that was read
2	(R_01)	Content of interrupt mask register R_01 that was written
3	(R_04)	Content of channel connection register R_04 that was written
4	(R_05)	Content of timing interrupt register R_05 that was written
5	(R_1A)	Display of frame sync monitor R_1A that was read (4 times/1 frame)
6	(R_34)	Content of interrupt condition register R_34 that was written
7	(R_37)	Display of receive status register R_37 (1 time/1 frame at receive interrupt after 2nd horizontal error correction)
8	PacketNo_MAIN	Packet number of main channel when an interrupt (main channel) is generated
9	2nd horizontal data update flag	Display at completion of receive data read after 2nd horizontal error correction
10	N	Number of block transfers 1 to 5: Receive data exists after 2nd horizontal error correction 0: No receive data after 2nd horizontal error correction
11	i	2nd horizontal error correction USR_RAM pointer To simplify explanation, cleared to "0" at reset
12	2nd horizontal USR_RAM	Buffer area for receive data that was read after 2nd horizontal error correction
13	j	1st horizontal error correction USR_RAM_SUB pointer To simplify explanation, cleared to "0" at reset
14	1st horizontal USR_RAM	Buffer area for receive data that was read after 1st horizontal error correction

2.1.5 Description of Each Flow

Control of the total flow is indicated in items (1) to (5).

(1) Power-on control flow
Shown in figure 2.1.5.1.

(2) Initial parameter setting
Table 2.1 lists recommended parameter setting values and table 2.2 lists registers in which parameter setting is unnecessary. Figure 2.1.5.2 shows the parameter setting flow.

(3) MAIN channel activation
Shown in figure 2.1.5.3.

(4) MAIN channel switching
Shown in figure 2.1.5.4.

(5) MAIN channel halting
Shown in figure 2.1.5.5.

Interrupt control of the MAIN channel is indicated in items (6) to (9).

(6) Interrupt control
Shown in figure 2.1.5.6.

(7) Receive _MAIN after 1st horizontal error correction
Shown in figure 2.1.5.7.

(8) Reception after 2nd horizontal error correction
Shown in figure 2.1.5.8.
If there is a receive interrupt after the 2nd horizontal error correction, set the receive port (R_38) pointer to "0." Because the quantity of data is large, if the data cannot all be read at once (approx. 10 ms), divide it into several packets and then read the data.
In this example, data is divided into N = 5 packets and is read five times. Interrupts are set at each packet timing. When N = 0 and the read is completed, interrupts are released at each packet timing, and after the 2nd horizontal error correction, update and display data is written.

(9) Status monitor
Shown in figure 2.1.5.9.

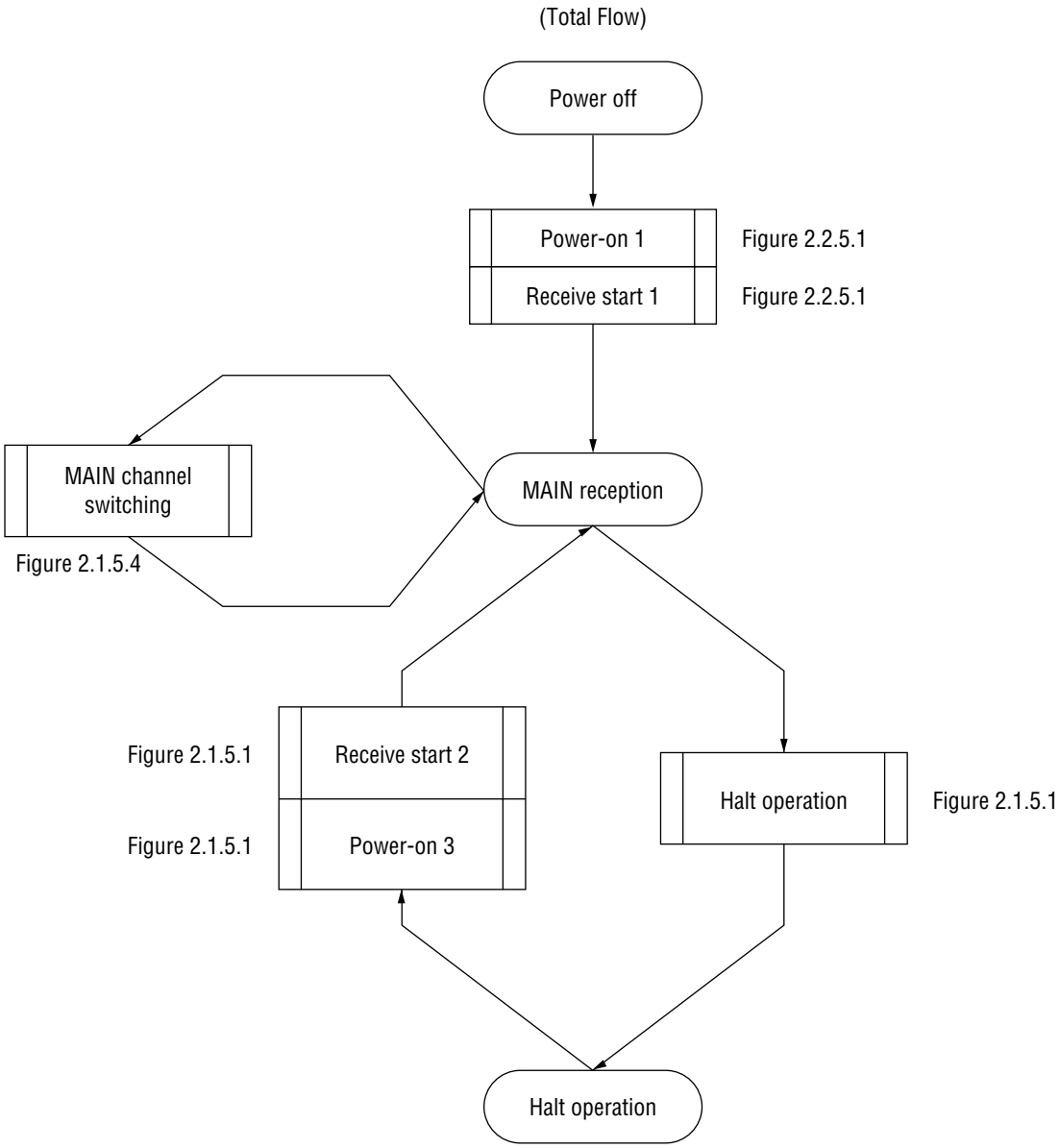


Figure 2.1.1 Total Flow

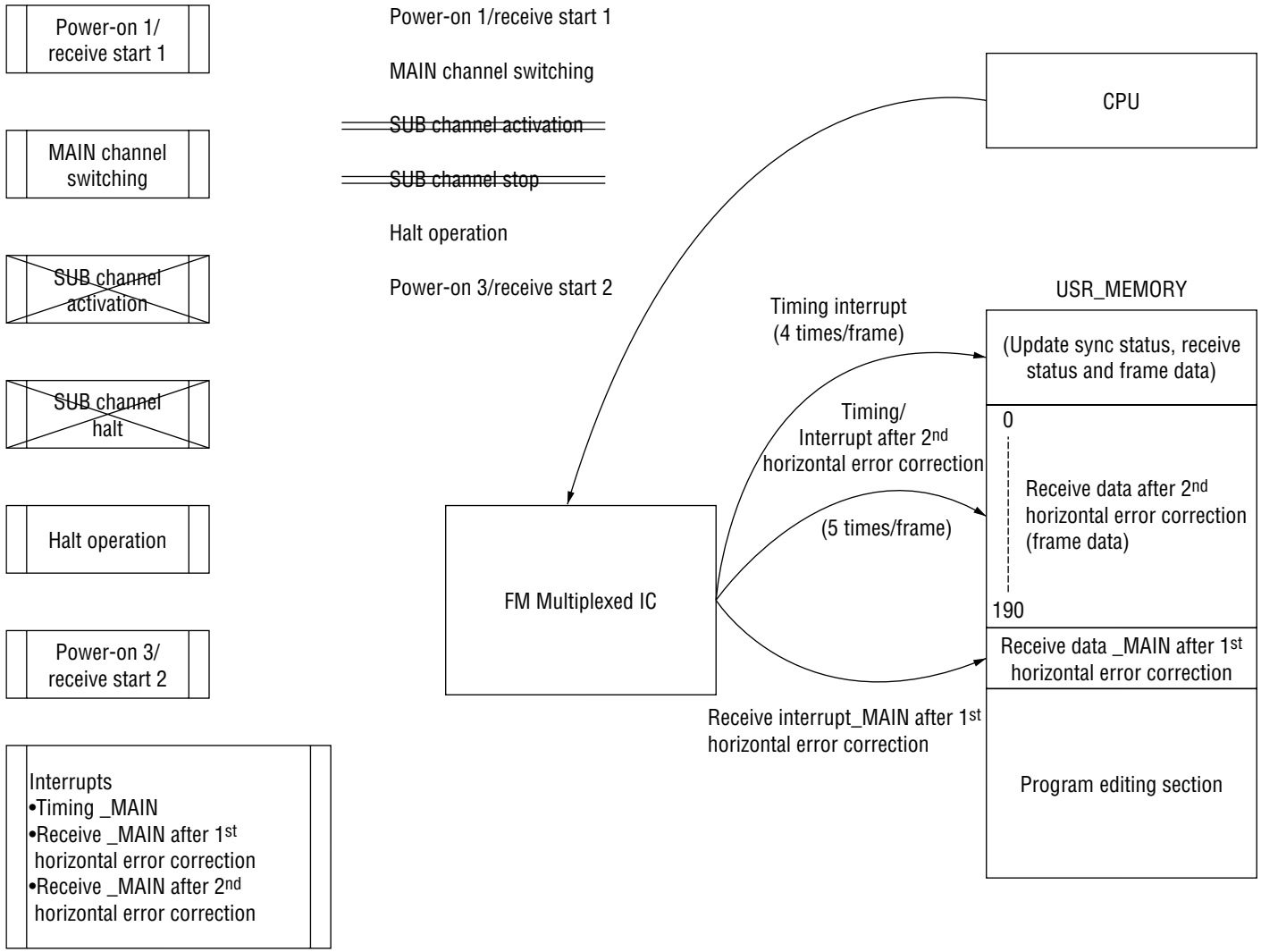


Figure 2.1.2 Total Configuration

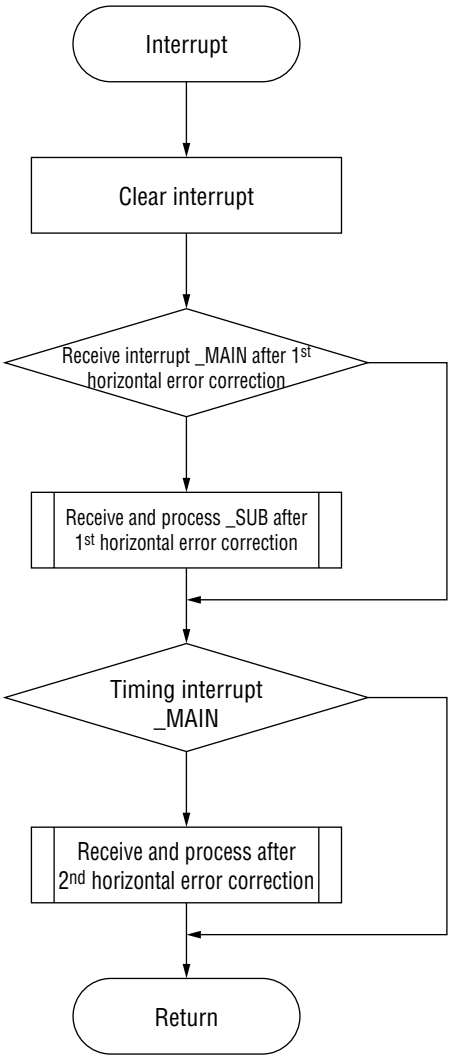
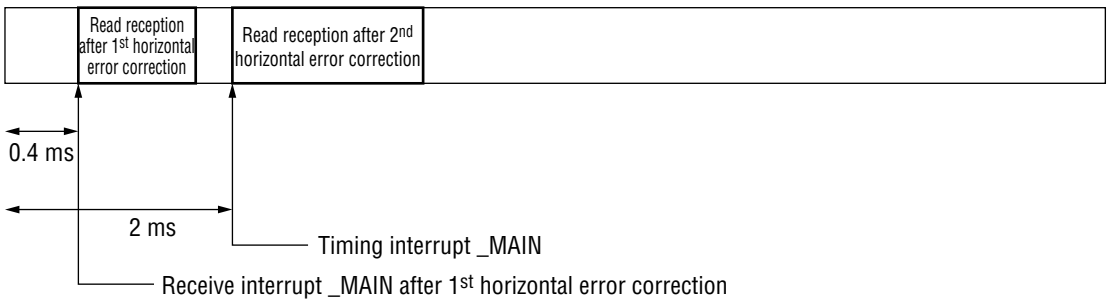


Figure 2.1.3 Simplified Interrupt Flow

Case where receive _MAIN after 1st horizontal error correction and timing interrupt _MAIN occur in the same packet



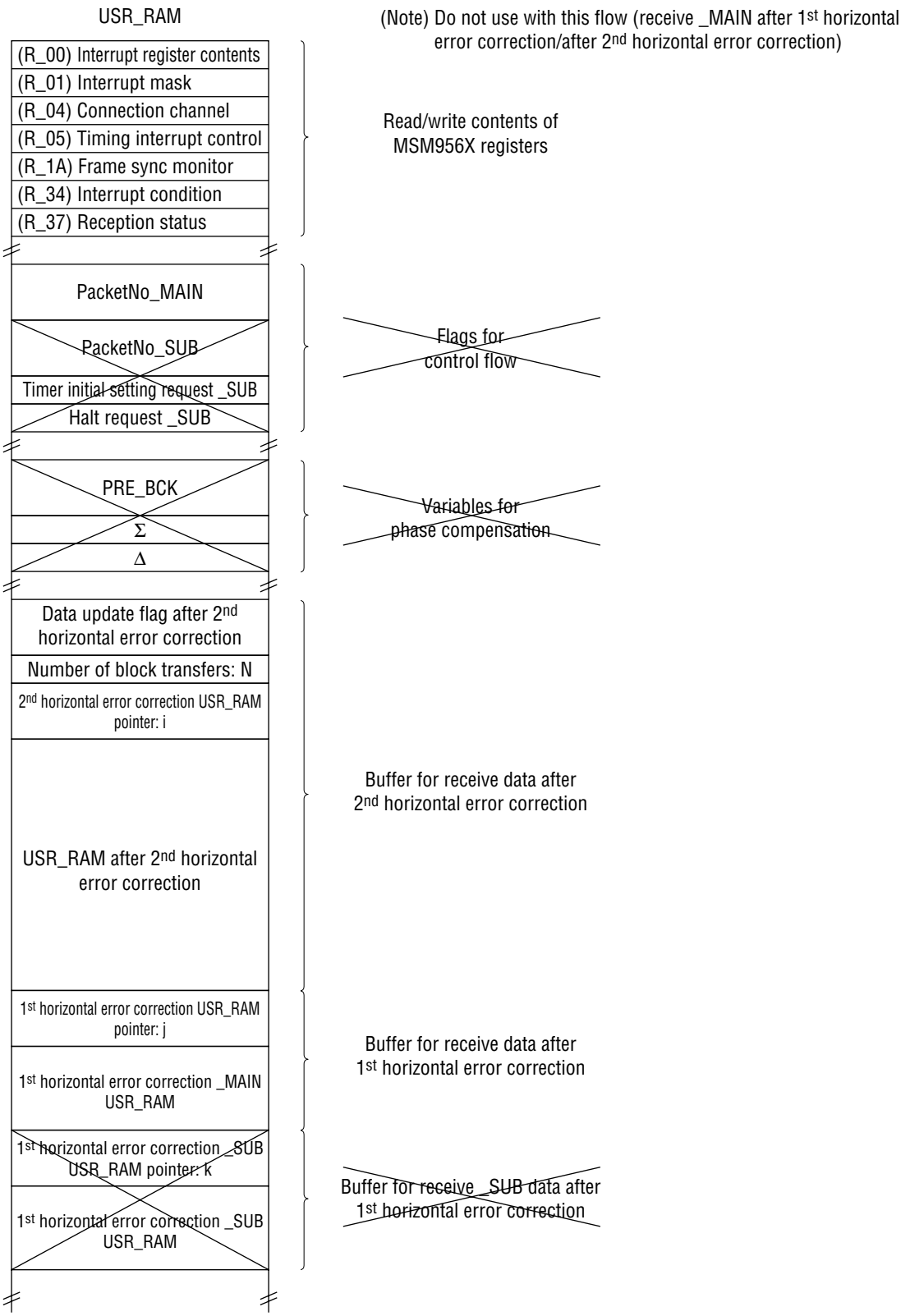


Figure 2.1.4 USR_RAM Configuration

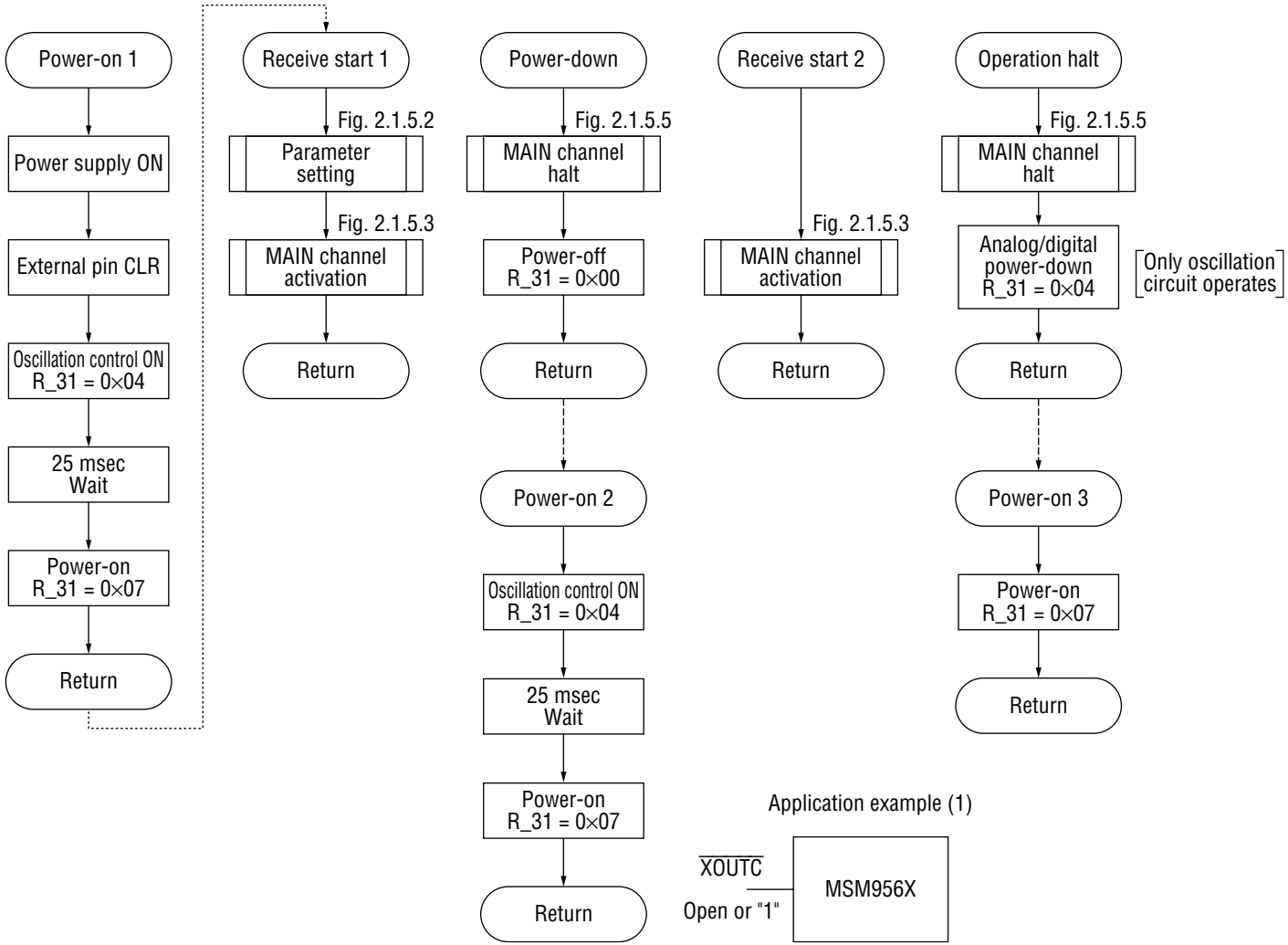


Figure 2.1.5.1 Power-On Control Flow

Table 2.1 Recommended Parameter Setting Values

Register	Address	Setting value	Description
Interrupt mask	0×01	0×36	Receive _MAIN after 1st horizontal error correction = timing _MAIN = "1" After 2nd horizontal error correction, setting is unnecessary since receive _MAIN and sync displacement are determined at time of R_00 read.
Integration constant before block synchronization	0×0C	0×06	6
Integration constant after block synchronization	0×0D	0×10	16
Phase correction step	0×0E	0×33	4/4MHz
Allowable Number of BIC Error Bits	0×10	0×09	Before synchronization: 1 After synchronization: 2
No. of Block Sync Backward Protection Steps	0×11	0×12	SUB = 1 MAIN = 2
No. of Block Sync Forward Protection Steps	0×12	0×4F	SUB = 4 MAIN = 15
No. of Frame Sync Backward Protection Steps	0×18	0×00	1
No. of Frame Sync Forward Protection Steps	0×19	0×04	4
DDJ mode *	0×28	0×A0	1st horizontal error correction/2nd horizontal error correction mode
Analog	0×30	0×06	DETO_DTST: invalid, ADETIN: invalid Amp gain: ×3, DETTC: invalid
TST1	0×33	0×04	PN decoding: on, Differential decoding: off, Monitor: off

* For MSM9566/67 only

Table 2.2 Registers That Do Not Require Parameter Setting

Register	Address	Initial value	Description
Receive port switching after 1st horizontal error correction	0×02	0×00	Use initial value of receive _MAIN after 1st horizontal error correction
Main/sub channel switching	0×04	0×01	Use initial value of main channel (no switching)
Fixed phase adjustment	0×0B	0×00	Setting unnecessary
Clear/set block sync	0×14	0×00	Setting unnecessary
Clear sync	0×1B	0×00	Setting unnecessary
Set sync	0×1C	0×00	Setting unnecessary
Frame format	0×1F	0×02	B format
Error correction	0×20 to 0×22	0×00	Not used
Number of error corrections	0×23	0×FB	Use initial value
Number of error corrections/threshold value	0×25	0×EE	Use initial value
Operating mode	0×3E	0×00	Use initial value

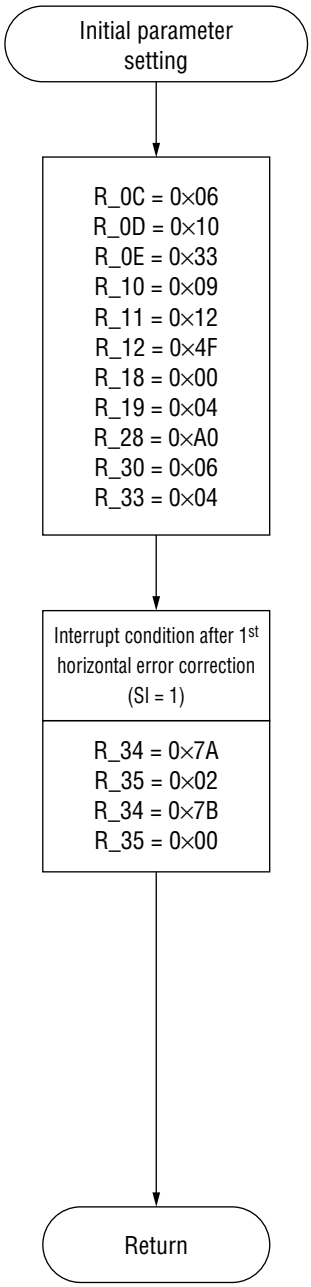


Figure 2.1.5.2
Initial Parameter Setting

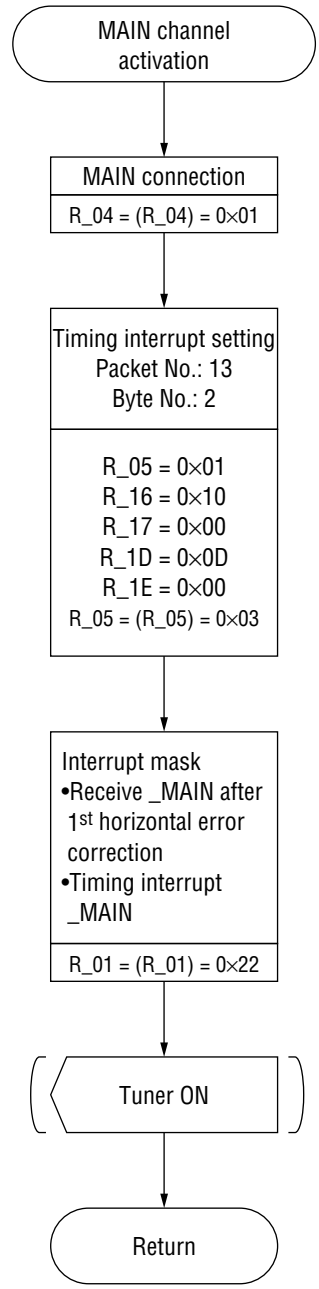


Figure 2.1.5.3
Main Channel Activation

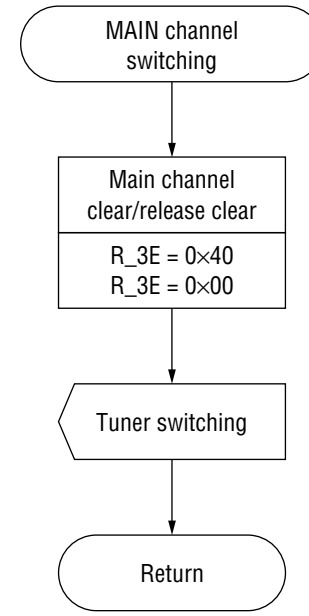


Figure 2.1.5.4
Main Channel Switched Reception

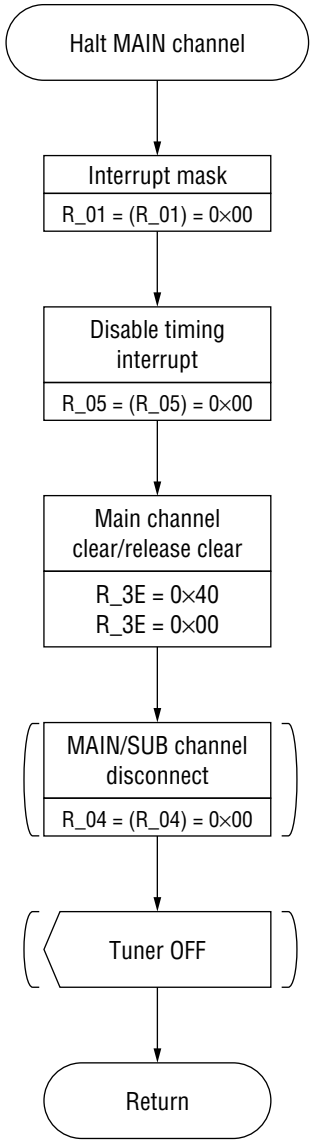


Figure 2.1.5.5 Main Channel Halt

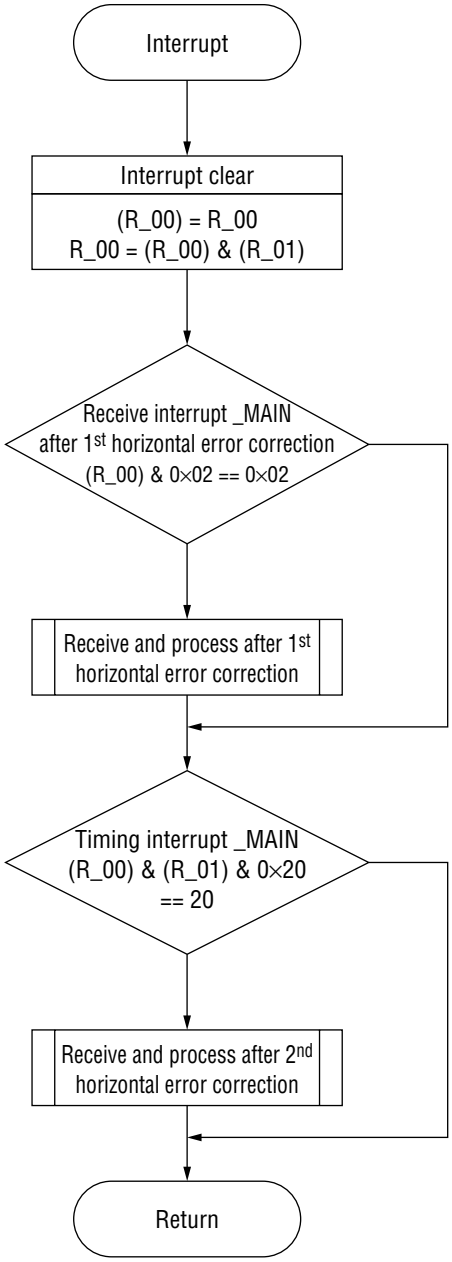


Fig. 2.1.5.7

Fig. 2.1.5.8

Figure 2.1.5.6 Interrupt Control

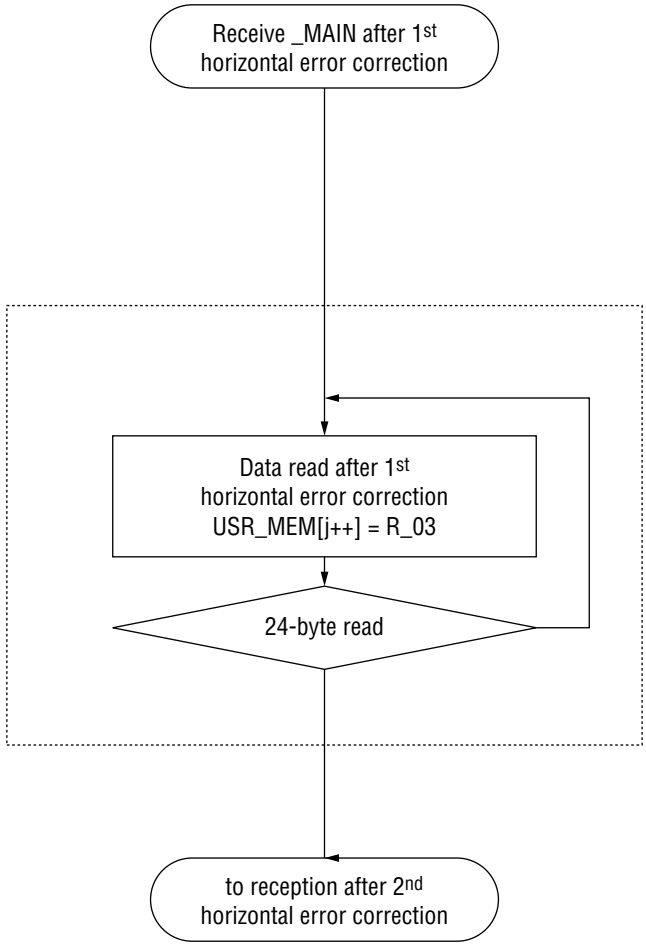


Figure 2.1.5.7 Receive _MAIN After 1st Horizontal Error Correction

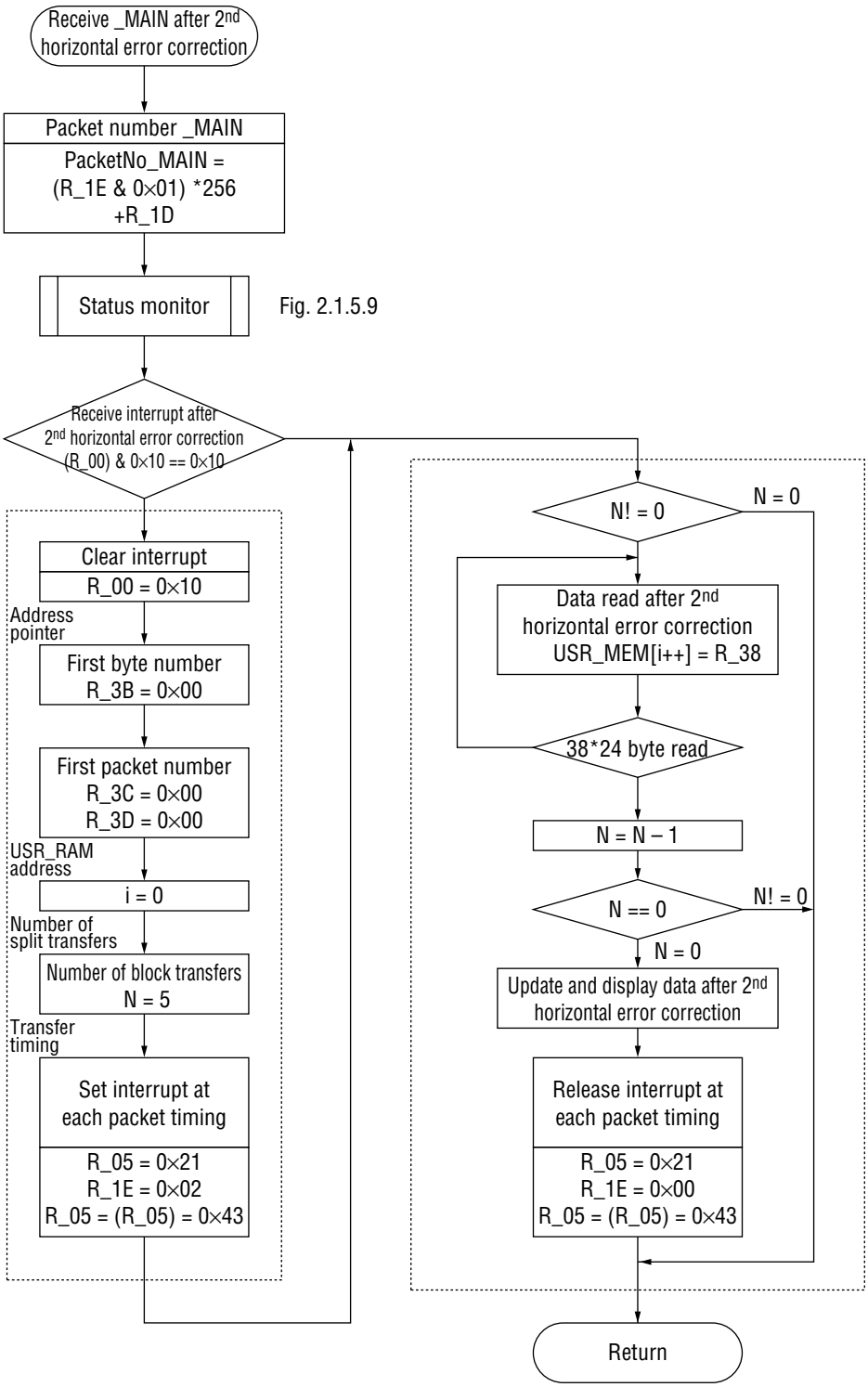


Figure 2.1.5.8 Reception After 2nd Horizontal Error Correction

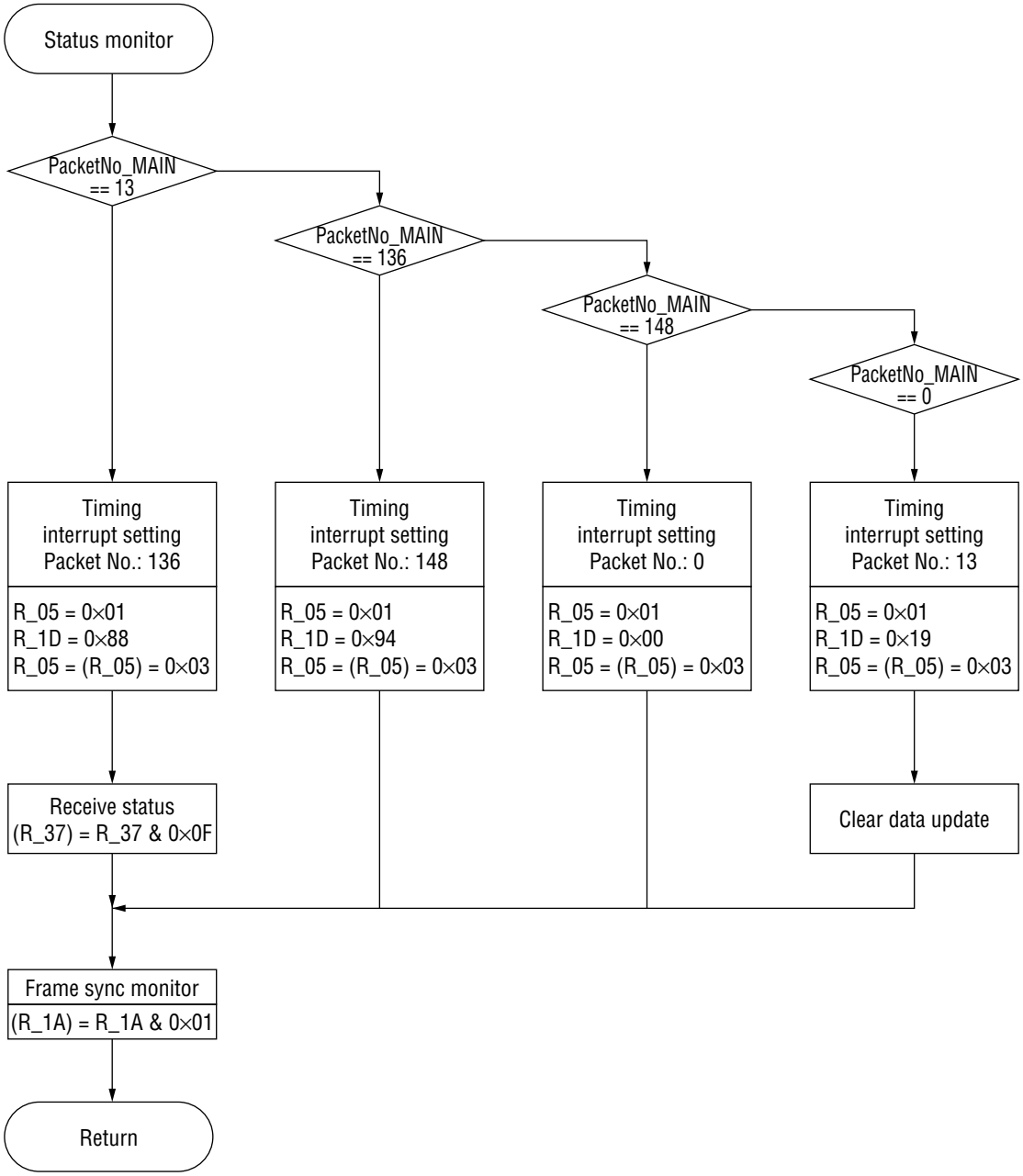


Figure 2.1.5.9 Status Monitor

2.2 Main/Sub Switched Reception

An example of the control flow of main/sub switched reception is listed below.

(1) This example indicates the control flow of the receive _MAIN after the 2nd horizontal error correction and the receive _SUB after the 1st horizontal error correction. The receive _MAIN after the 1st horizontal error correction is omitted.

(2) This example assumes that the sub-channel reception time includes: tuner switching time of 1×2 packets, clock capture time of 1/3 packet, and block synchronization time of 1 packet. In this case, 5.5 packets (including receive packet 2) disappear from the main channel.

2.2.1 Total Flow

(1) Figure 2.2.1.1 shows the block diagram.

(2) Figure 2.2.1.2 shows the total flow.
The total flow can be changed by the following five controls
- Power-on/receive start (power-on 2/receive start 3)
- Switching the MAIN channel
- Activating the SUB channel
- Halting the SUB channel
- Halting operation

(3) Figure 2.2.1.3-1/2 and figure 2.2.1.3-2/2 show the main/sub switching timing. Main channel packets are shown on the left and sub-channel packets on the right. To simplify this example, the packets have matching starting positions. In an actual application these positions are displaced, however details of the explanation do not change.

2.2.2 Total Configuration

Figure 2.2.2 shows the total configuration.
This figure shows the total flow control and the function of interrupts.

Controls that manage the total flow such as MAIN reception, MAIN/SUB switched reception, halting operation, etc. are executed from the main program. It is not necessary to synchronize these controls to the IC.

The transfer of receive data (Layer 3 data) after the 2nd horizontal error correction or of receive _SUB data after the 1st horizontal error correction to the USR_RAM, modification and display of this receive data, display of the synchronous state of the FM multiplexing IC, etc. are performed by interrupt control. This control must be synchronized with an IC interrupt.

2.2.3 Interrupts

Figure 2.2.3 shows a simplified flow of interrupt processing.

2.2.4 User RAM Configuration

Figure 2.2.4 shows the configuration of user RAM and table 2.2.4 shows the contents of user RAM utilized in this flow.

Table 2.2.4 User RAM Contents

1	(R_00)	Content of interrupt register R_00 that was read
2	(R_01)	Content of interrupt mask register R_01 that was written
3	(R_04)	Content of channel connection register R_04 that was written
4	(R_05)	Content of timing interrupt register R_05 that was written
5	(R_1A)	Display of frame sync monitor R_1A that was read (4 times/1 frame)
6	(R_34)	Content of interrupt condition register R_34 that was written
7	(R_37)	Display of receive status register R_37 (1 time/1 frame at receive interrupt after 2nd horizontal error correction)
8	PacketNo_MAIN	Packet number of main channel when an interrupt (main channel) is generated
9	PacketNo_SUB	Packet number of sub channel when an interrupt (sub-channel) is generated
10	Halt request _SUB	Halt request flag for sub-channel reception
11	PRE_BCK	Stores the bit number immediately prior to block synchronization of the sub-channel If there is no bit displacement, the value is 16.
12	Δ	Stores the bit displacement Δ = PRE_BCK-16
13	Σ	Stores the bit displacement compensation value ($\Sigma = \Sigma + \Delta$)
14	2nd horizontal data update flag	Displayed at completion of receive data read after 2nd horizontal error correction
15	N	Number of block transfers when reading data after the 2nd horizontal error correction. In this example, transfers are divided into N = 5 times. 1 to 5: Receive data exists after 2nd horizontal error correction 0: No receive data after 2nd horizontal error correction
16	i	2nd horizontal error correction USR_RAM pointer To simplify explanation, cleared to "0" at reset
17	2nd horizontal USR_RAM	Buffer area for receive data after 2nd horizontal error correction that was read
18	j	USR_RAM_SUB pointer after 1st horizontal error correction To simplify explanation, cleared to "0" at reset
19	1st horizontal USR_RAM_SUB	Buffer area for receive data SUB after 1st horizontal error correction that was read

2.2.5 Description of Each Flow

Control of the total flow is indicated in items (1) to (7).

(1) Power-on control flow
Shown in figure 2.2.5.1.

(2) Initial parameter setting
Table 2.3 lists recommended parameter setting values and table 2.4 lists registers in which parameter setting is unnecessary. Figure 2.2.5.2 shows the parameter setting flow.

(3) MAIN channel activation
Shown in figure 2.2.5.3.

(4) MAIN channel switching
Shown in figure 2.2.5.4.

(5) SUB channel activation
Shown in figure 2.2.5.5.

(6) SUB channel halting
Shown in figure 2.2.5.6.

(7) MAIN channel halting
Shown in figure 2.2.5.7.

Interrupt control
(8) Interrupt control
Shown in figure 2.2.5.8.

Interrupt control of the MAIN channel is indicated in items (9) to (11).

(9) Frame timing setup _SUB
Shown in figure 2.2.5.9.
If (R_01) = 0×11(MAIN/SUB), since synchronization will be established for the first time with the SUB station, frame timing setup _SUB control is performed.
The control flow initializes settings of the timer _SUB to the packet number of the synchronous SUB station.
The packet number of the MAIN channel is set to the packet number counter (R_08, R_09) of the sub-channel so that the packet numbers are equal. Thereafter, use of timing interrupt _SUB is possible.
Next, the timing is set to switch the tuner to the SUB station (packet number _SUB = 269, byte number = 22).

Since frame timing setup _SUB is completed via the MAIN channel, reception with the MAIN channel is possible. After the 1st horizontal error correction, original receive conditions (R_34) are restored and the receive state of the SUB station is cleared (R_3E). The tuner switches to the MAIN channel and, continuing from step (8), processing of this interrupt is completed.

(10) Reception after 2nd horizontal error correction
Shown in figure 2.2.5.10.
If there is a receive interrupt after the 2nd horizontal error correction, set the receive port (R_38) pointer to "0". Since the quantity of data is large, if the data cannot be read at once (approx. 10 ms), divide it into several packets and then read the data.
In this example, data is divided into N = 5 packets and is read. Interrupts are set at each packet timing. When N = 0 and the read is completed, interrupts are released at each packet timing, and after the 2nd horizontal error correction, update and display data is written.

(11) Status monitor
Shown in figure 2.2.5.11.

Interrupt control of the SUB channel is indicated in items (12) to (16).

(12) SUB control
Shown in figure 2.2.5.12.
Interrupt control of the SUB channel is activated by timer interrupt _SUB.
Depending upon the packet number _SUB of the internal counter that is read, control switches to SUB connection, receive _SUB after 1st horizontal error correction, or main connection.

(13) SUB connection
Shown in figure 2.2.5.13.
When the SUB station's packet number equals 269, control transfers to this flow.
The channel is set to SUB connection and the tuner is switched from the MAIN station to the SUB station.
Next, the receive timing of the 1st packet _SUB is set (packet number _SUB = 1, byte number = 2). The time until reception of the first packet _SUB consists of the following: tuner switch time, clock capture time, block sync time, and time required for reception of the first packet _SUB.

(14) Receive _SUB after 1st horizontal error correction
Shown in figure 2.2.5.14.
When packet number of the SUB station equals 1 or 2, control transfers to this flow.
When the receive interrupt is 1 after the 1st horizontal error correction, read 24 bytes of receive data.
When the packet number of the SUB station equals 2, since the packets of the SUB channel are completed, execute various controls (synchronous clear _SUB, SUB disconnect, switch the tuner from the SUB station to the MAIN station) to complete processing of this interrupt.

(15) MAIN channel connection
Shown in figure 2.2.5.15.
When the packet number of the SUB station equals 3, control transfers to this flow and connects the MAIN channel. When packet number _SUB equals 2, the switched tuner is stabilized and main channel reception can be resumed while maintaining the synchronous status when disconnected with a packet number of 269.

(16) Bit displacement compensation

Shown in figure 2.2.5.16.

After several consecutive frames, even if the packet number of the SUB station cannot be received, bit displacement compensation is performed to enable SUB connection with accurate timing.

7 bits can be compensated with 1 instruction. Bit compensation of up to 7 bits is implemented during the second packet reception of step (6). In the case of compensation of 8 bits or more, compensation of the remainder is implemented when MAIN channel connection of step (7) is 3.

Σ is the previous bit compensation number and Δ is the bit displacement detected this time.

Control of bit displacement compensation is required regardless of whether or not there is a receive packet.

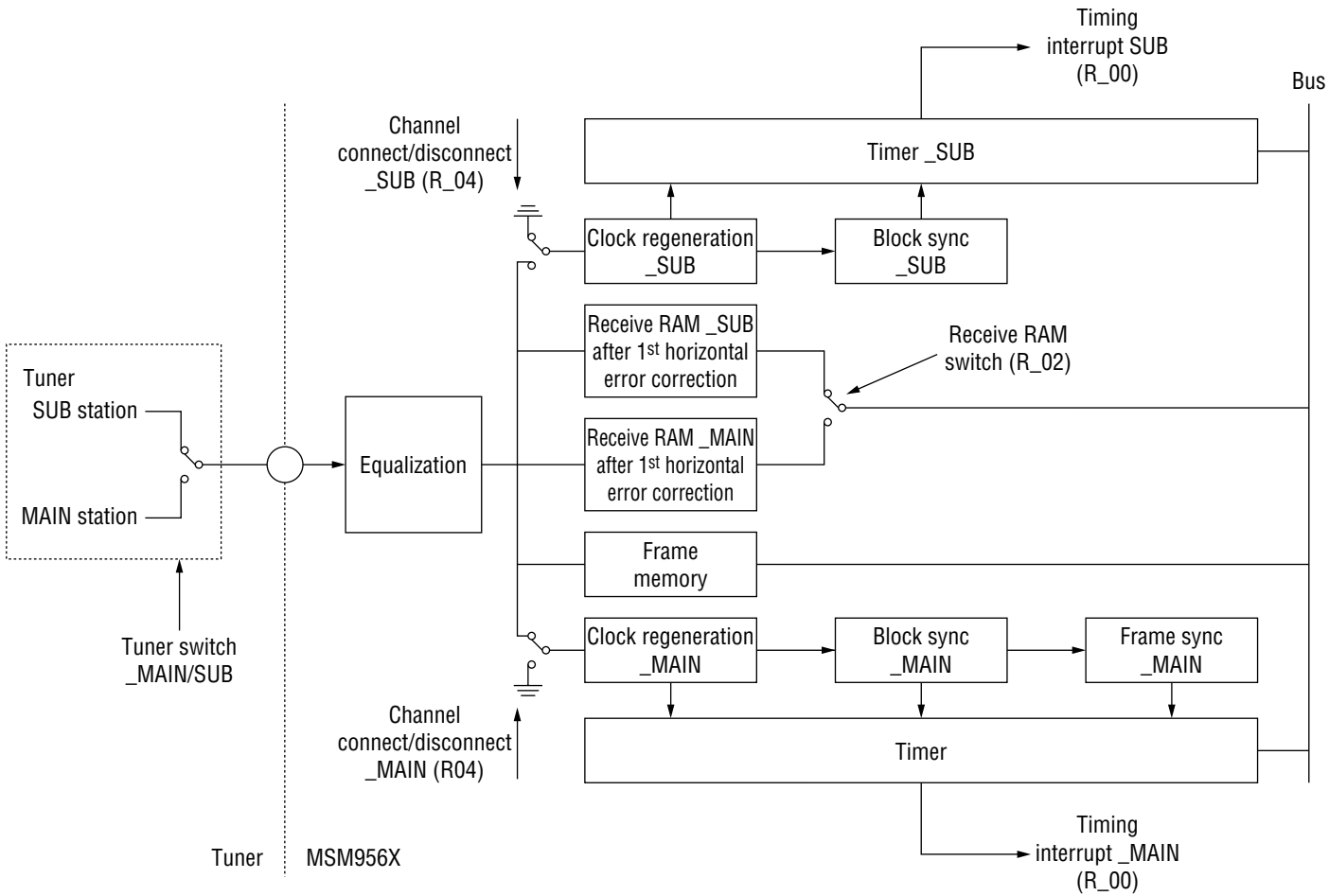


Figure 2.2.1.1 Main/Sub Switched Reception Block Diagram

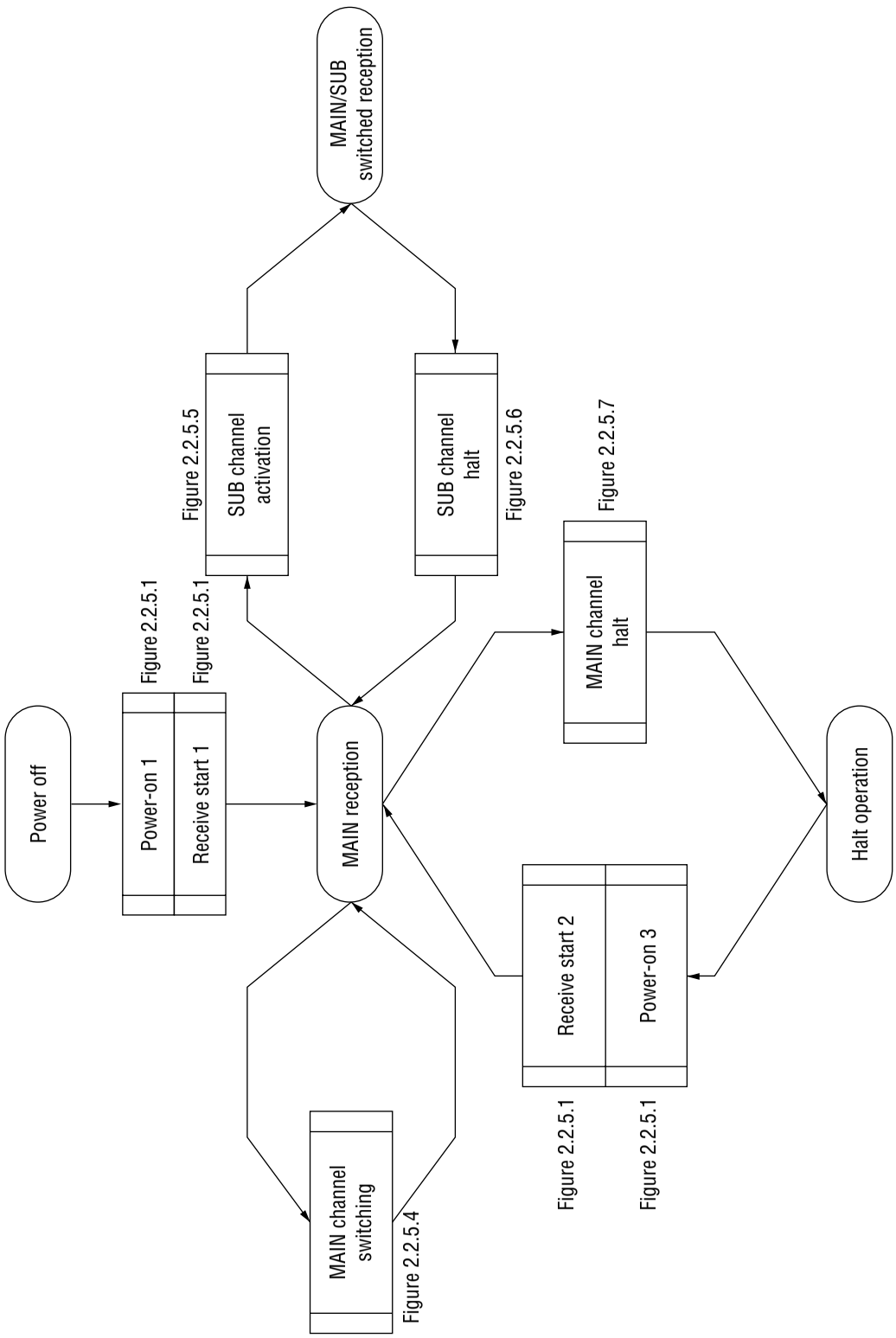


Figure 2.2.1.2 Total Flow

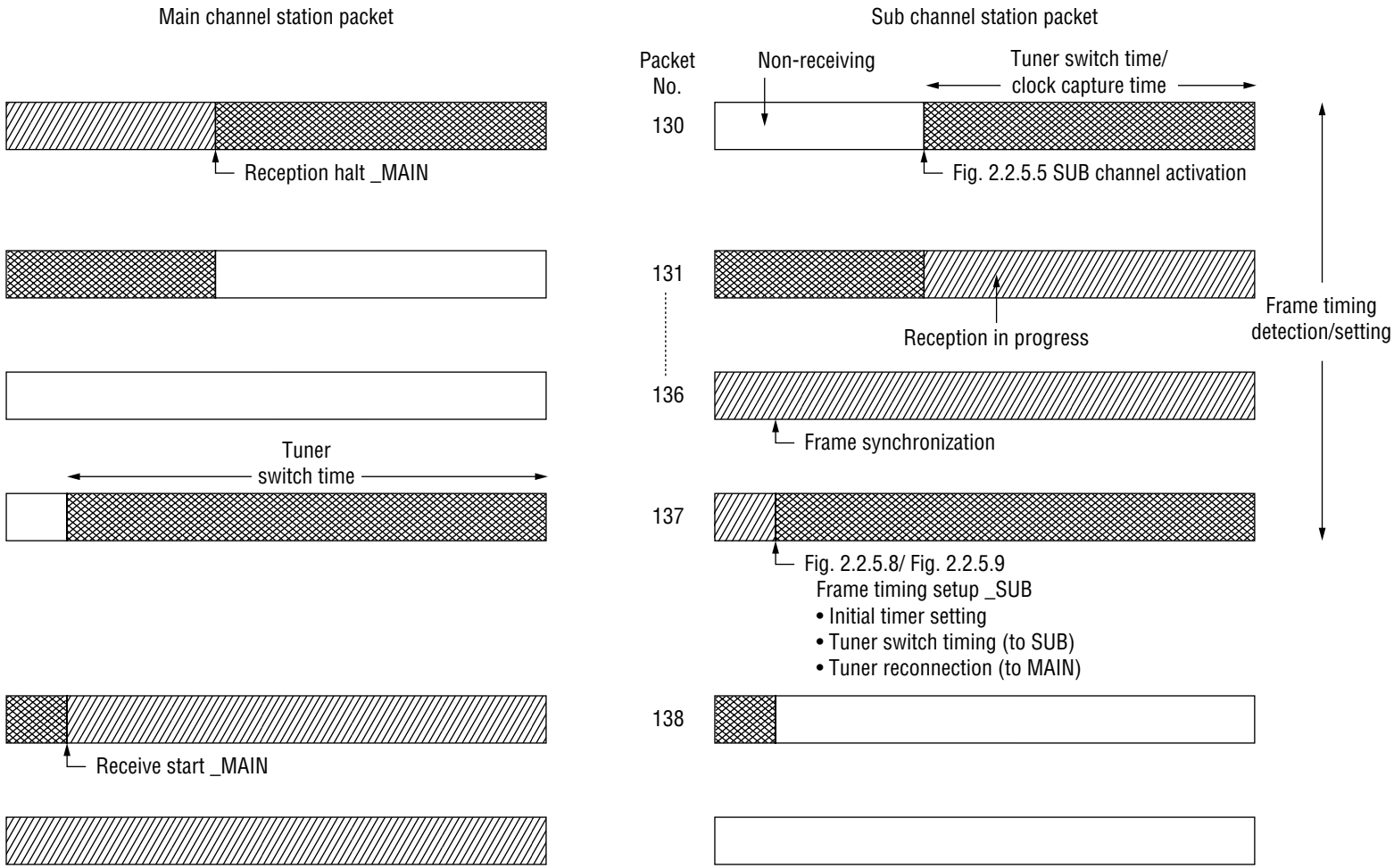


Figure 2.2.1.3-1/2 Main/Sub Switched Reception Timing

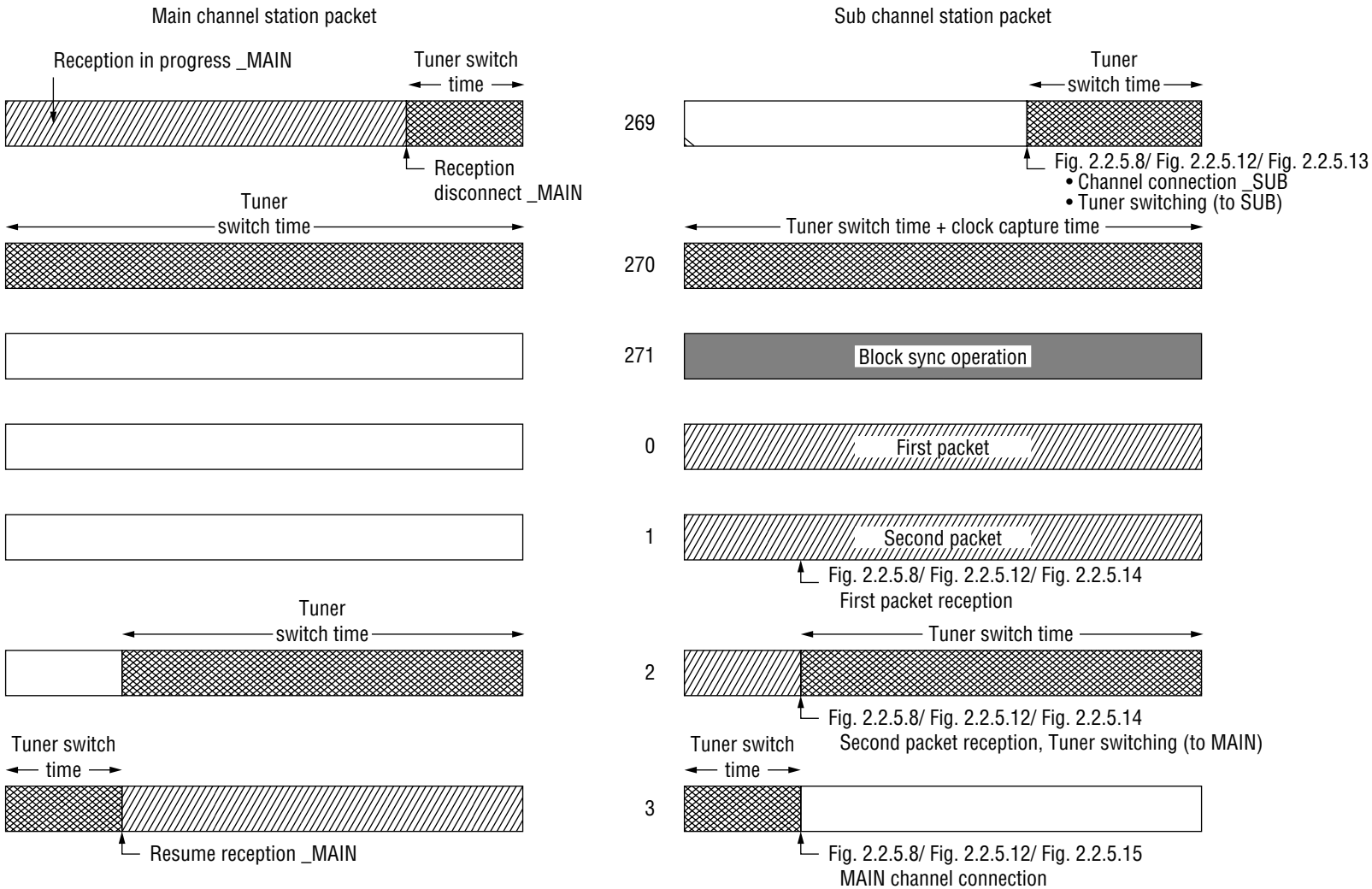


Figure 2.2.1.3-2/2 Main/Sub Switched Reception Timing

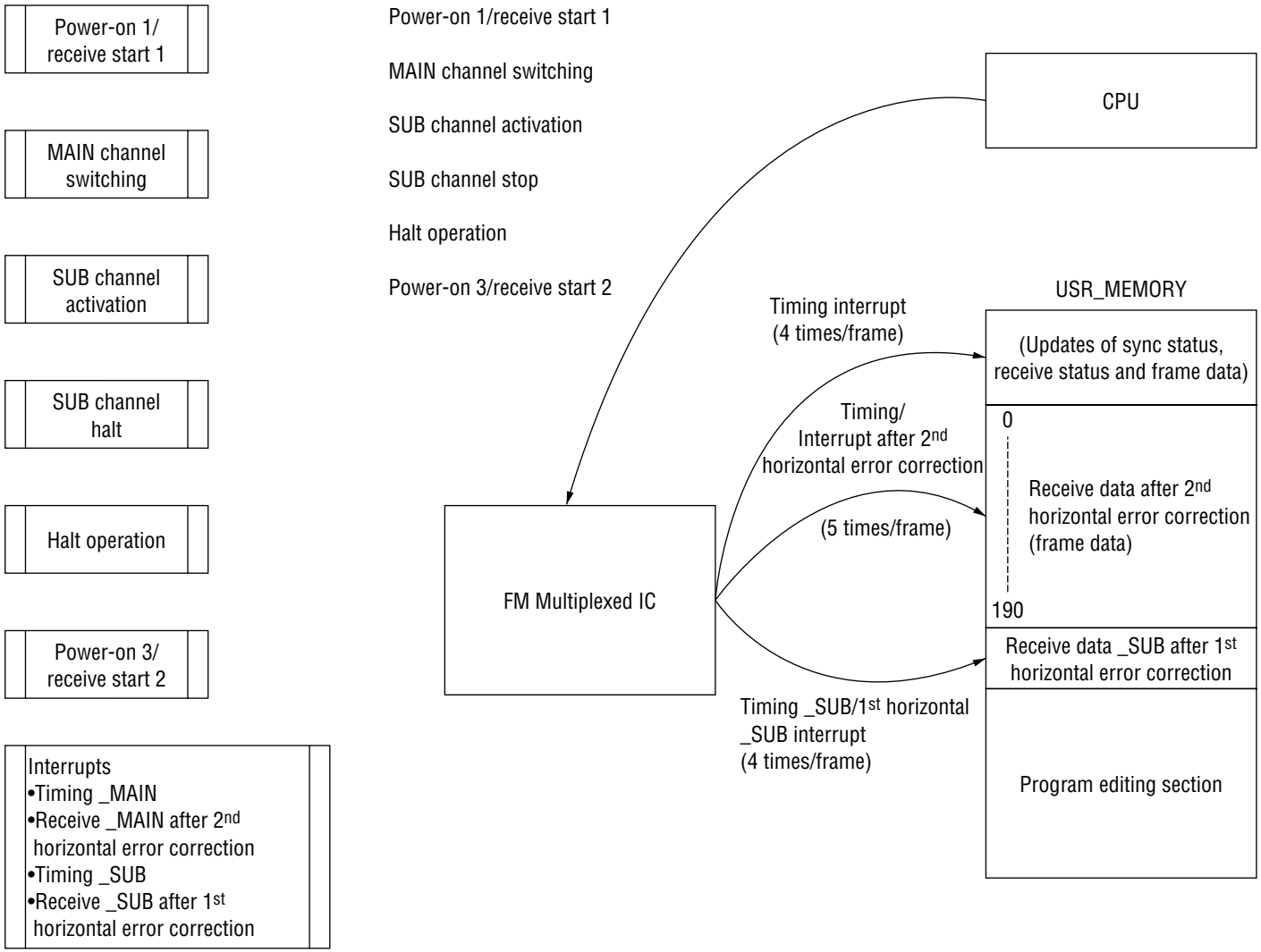


Figure 2.2.2 Total Configuration

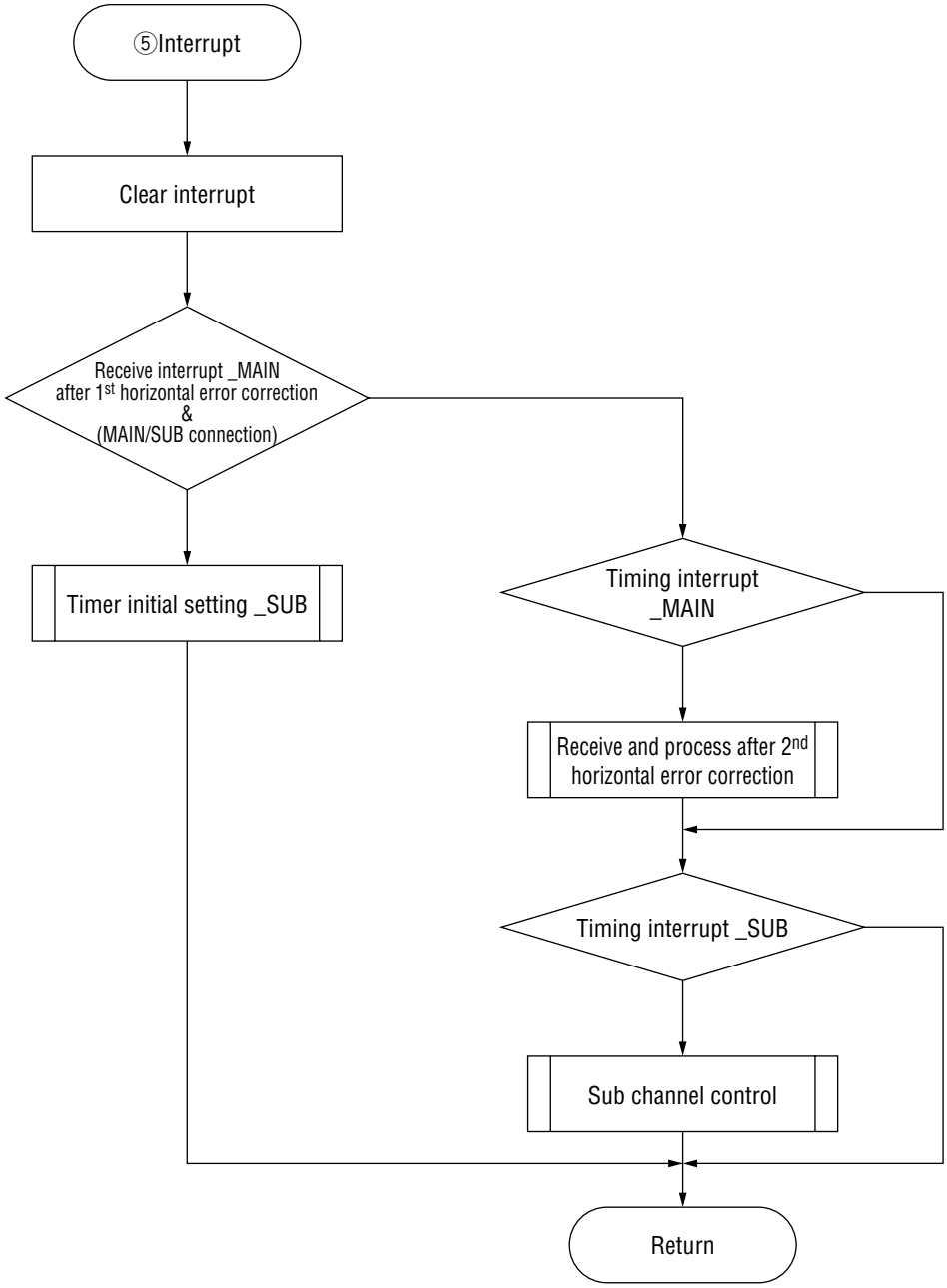


Figure 2.2.3 Simplified Interrupt Flow

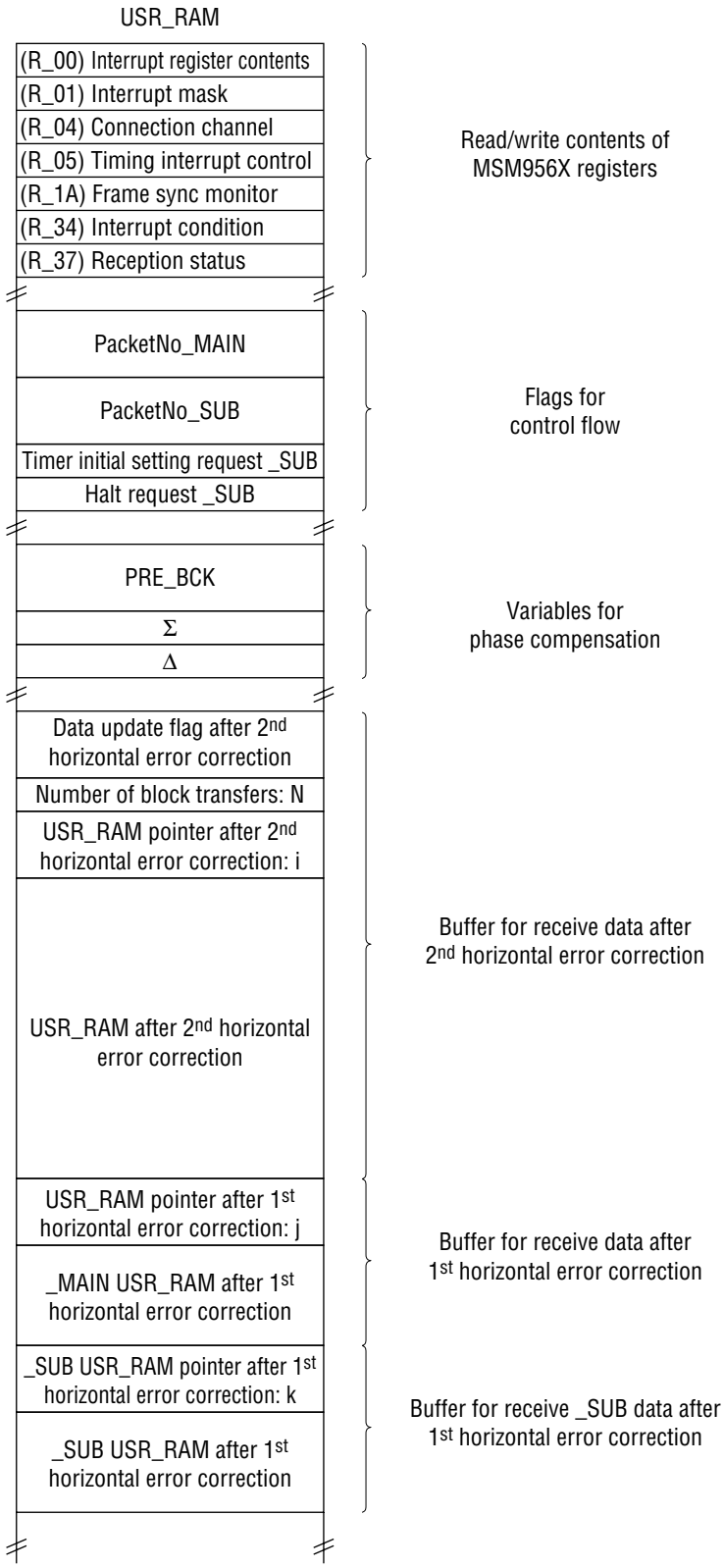


Figure 2.2.4 USR_RAM Configuration

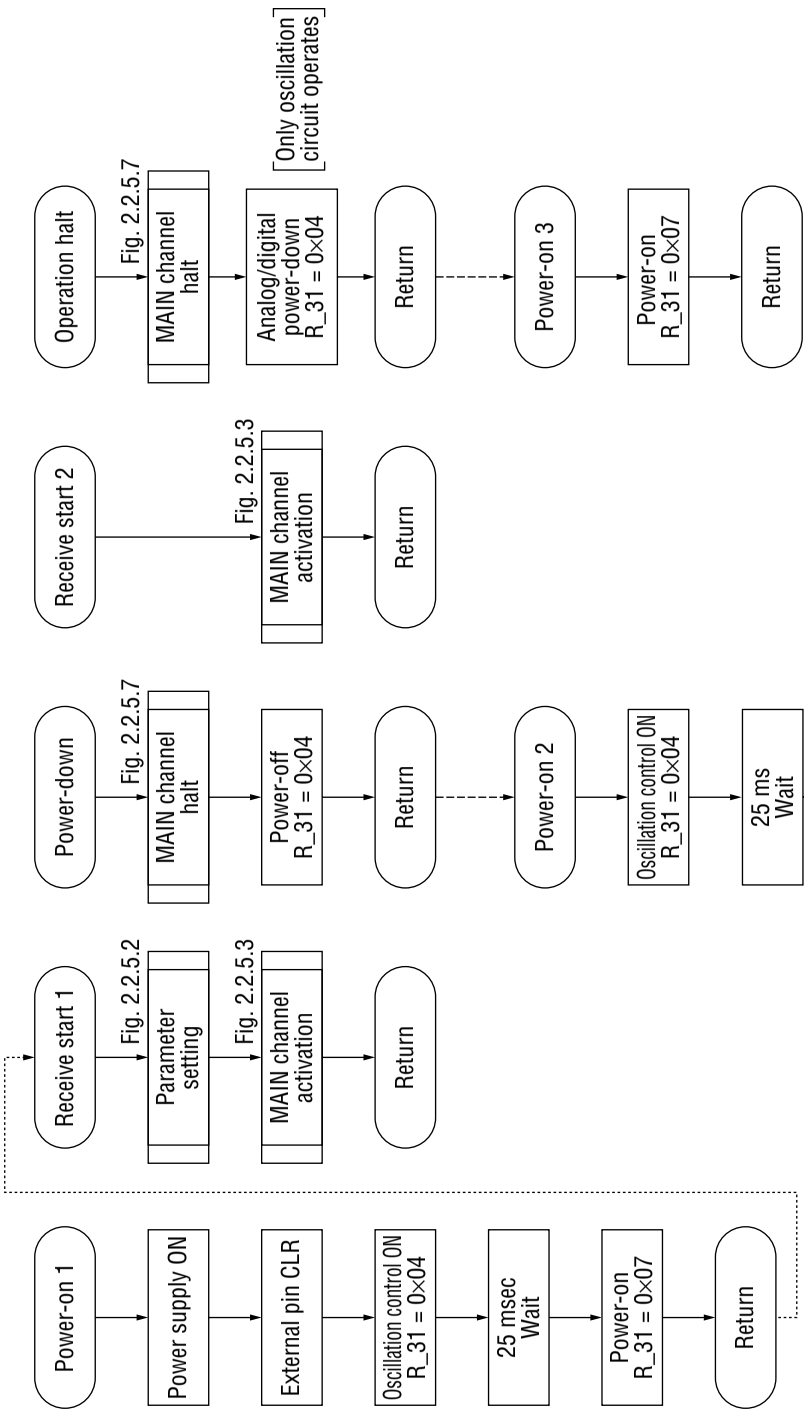


Figure 2.2.5.1 Power-On Control Flow

Table 2.3 Recommended Parameter Setting Values

Register	Address	Setting value	Description
Interrupt mask	0×01	0×36	Receive _MAIN after 1st horizontal error correction = timing _MAIN = "1" After 2nd horizontal error correction, setting is unnecessary since receive _MAIN and sync displacement are determined at time of R_00 read.
Integration constant before block synchronization	0×0C	0×06	6
Integration constant after block synchronization	0×0D	0×10	16
Phase correction step	0×0E	0×33	4/4MHz
No. of tolerable BIC errors	0×10	0×09	Before synchronization: 1 After synchronization: 2
No. of protective steps at rear of block synchronization	0×11	0×12	SUB = 1 MAIN = 2
No. of protective steps at front of block synchronization	0×12	0×4F	SUB = 4 MAIN = 15
No. of protective steps at rear of frame synchronization	0×18	0×00	1
No. of protective steps at front of frame synchronization	0×19	0×04	4
DDJ mode *	0×28	0×A0	1st horizontal error correction/2nd horizontal error correction mode
Analog	0×30	0×06	DETO_DTST: invalid, ADETIN: invalid Amp gain: ×3, DETTC: invalid
TST1	0×33	0×04	PN decoding: on, Differential decoding: off, Monitor: off

* For MSM9566/67 only

Table 2.4 Registers That Do Not Require Parameter Setting

Register	Address	Initial value	Description
Receive port switching after 1st horizontal error correction	0×02	0×00	Use initial value of receive _MAIN after 1st horizontal error correction
Main/sub channel switching	0×04	0×01	Use initial value of main channel (no switching)
Fixed phase adjustment	0×0B	0×00	Setting unnecessary
Clear/set block sync	0×14	0×00	Setting unnecessary
Clear sync	0×1B	0×00	Setting unnecessary
Set sync	0×1C	0×00	Setting unnecessary
Frame format	0×1F	0×02	B format
Error correction	0×20 to 0×22	0×00	Not used
Number of error corrections	0×23	0×FB	Use initial value
Number of error corrections/threshold value	0×25	0×EE	Use initial value
Operating mode	0×3E	0×00	Use initial value

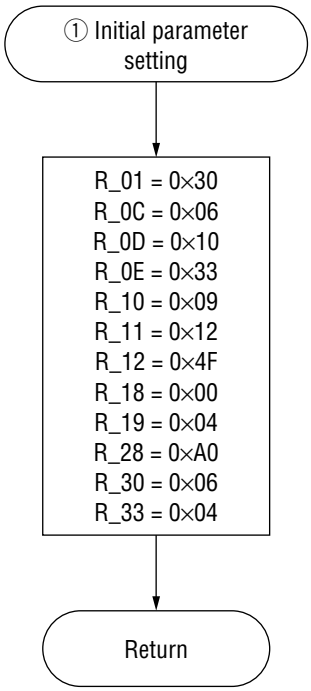


Figure 2.2.5.2
Initial Parameter Setting

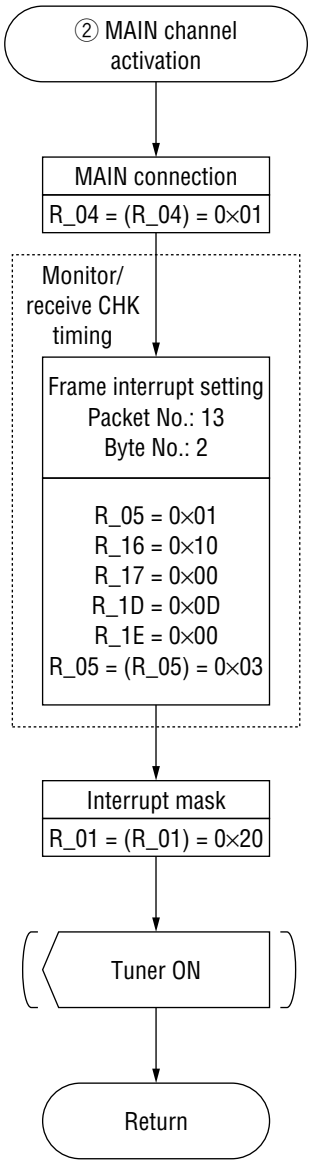


Figure 2.2.5.3
Main Channel Activation

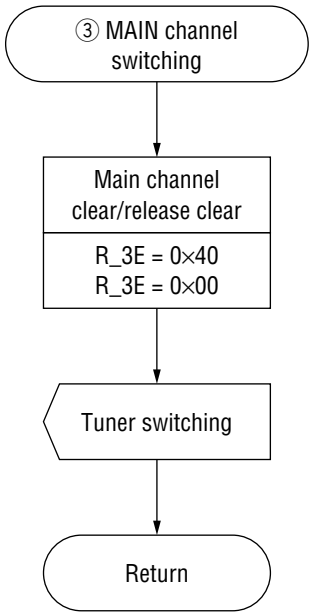


Figure 2.2.5.4
Main Channel Switched Reception

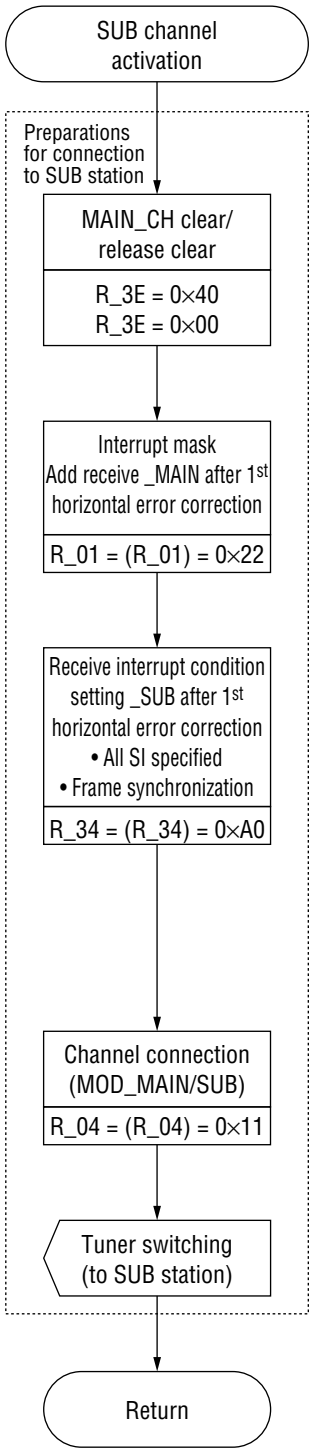


Figure 2.2.5.5 Sub Channel Activation

Activation of SUB Channel Halt

SUB channel reception is halted while maintaining the receive state of the MAIN channel.

(1) In the state where "PacketNo = 269 or 1 or 2", the tuner is connected to the SUB station. Control is performed as follows: ① the MAIN/SUB channel is disconnected, ② the tuner is switched to the MAIN station, and ③ after the tuner switch time elapses, the MAIN channel is reconnected.
Processes ① and ② are executed with the flow shown below on the left. Process ③ is executed within the "figure 2.2.5.15 Main Connection" interrupt routine.
After executing the interrupt of process ③, SUB channel reception is halted.

(2) In the state where "PacketNo ! = 269 or 1 or 2", the tuner is not connected to the SUB station. Therefore, after the timing interrupt _SUB is halted and the SUB channel is disconnected, SUB channel reception is halted.

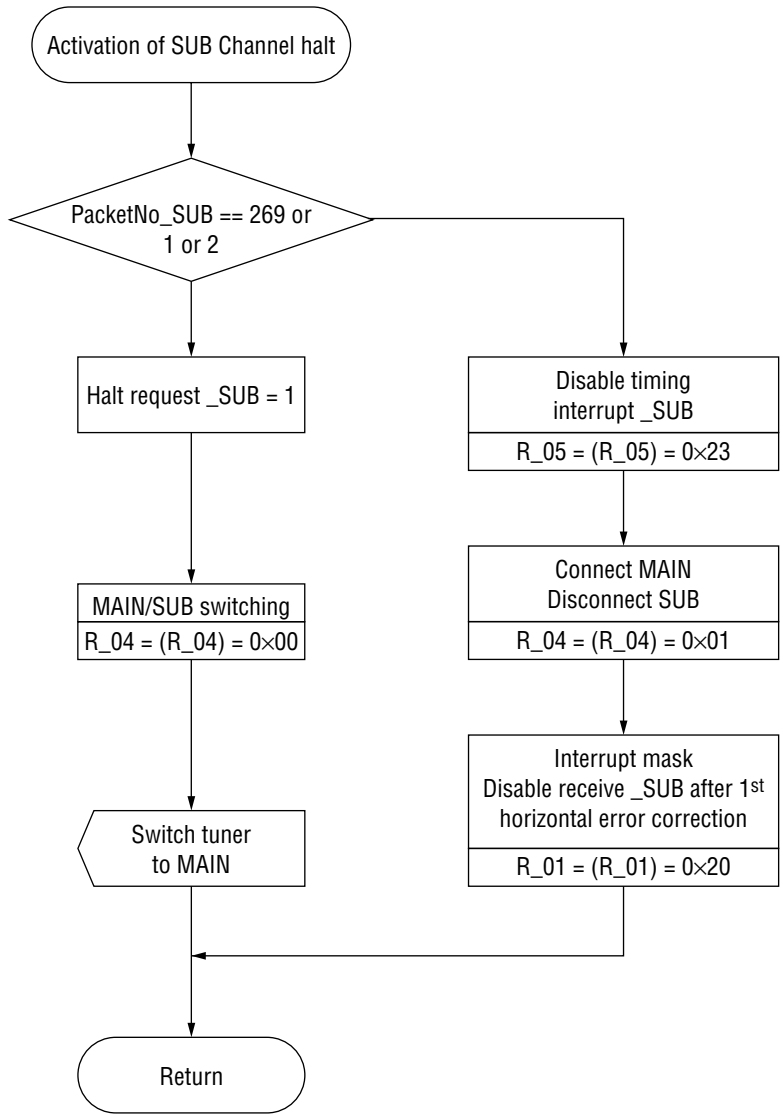


Figure 2.2.5.6 Halting the SUB Channel

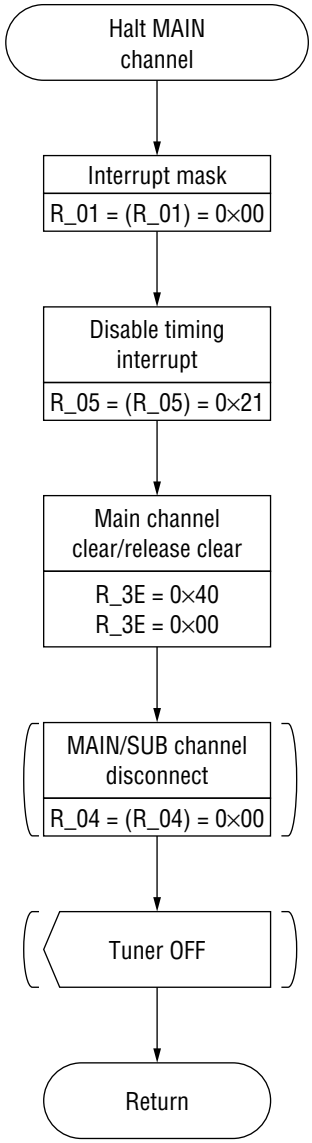


Figure 2.2.5.7 Halting the Main Channel

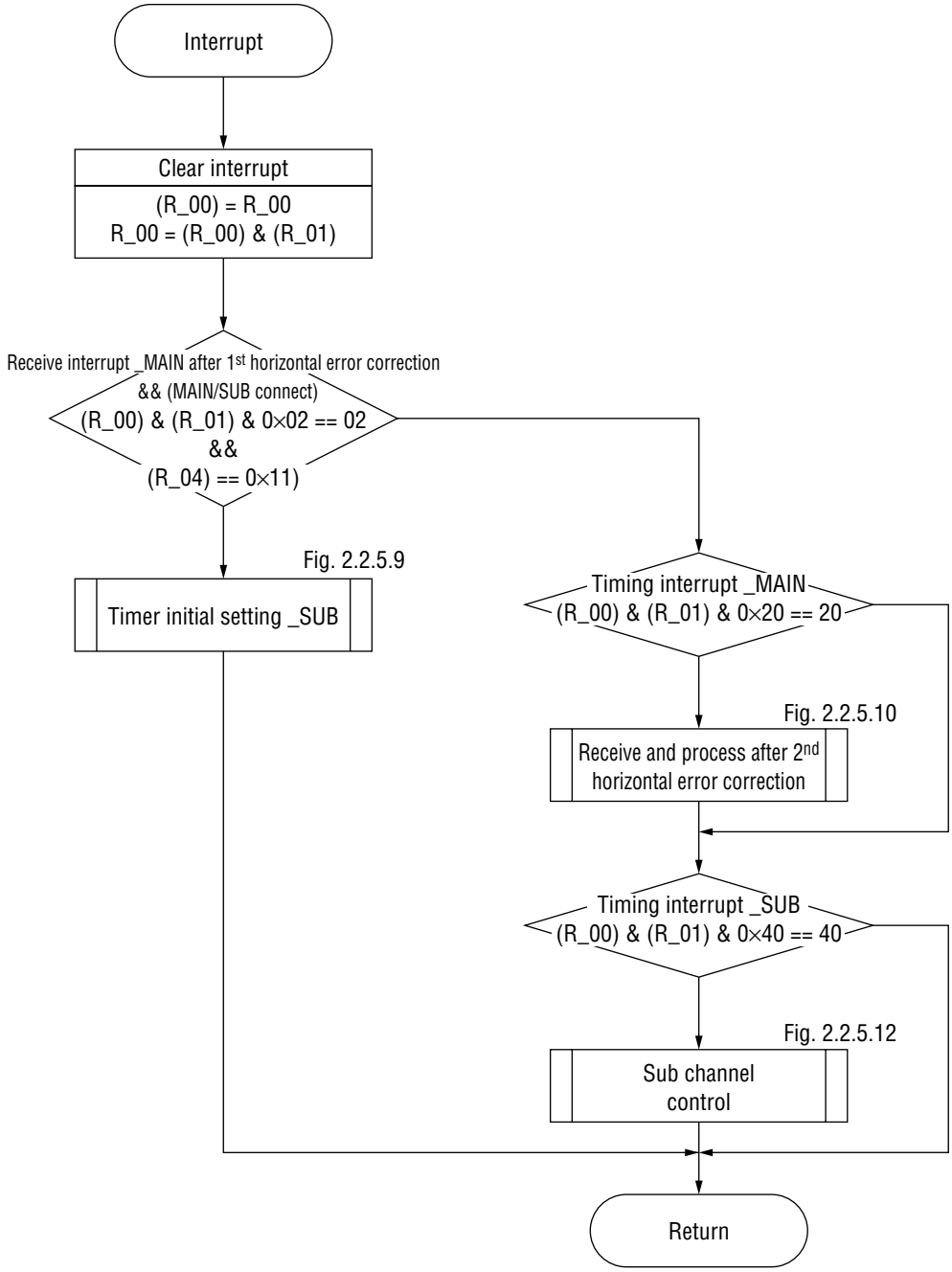


Figure 2.2.5.8 Interrupt Control

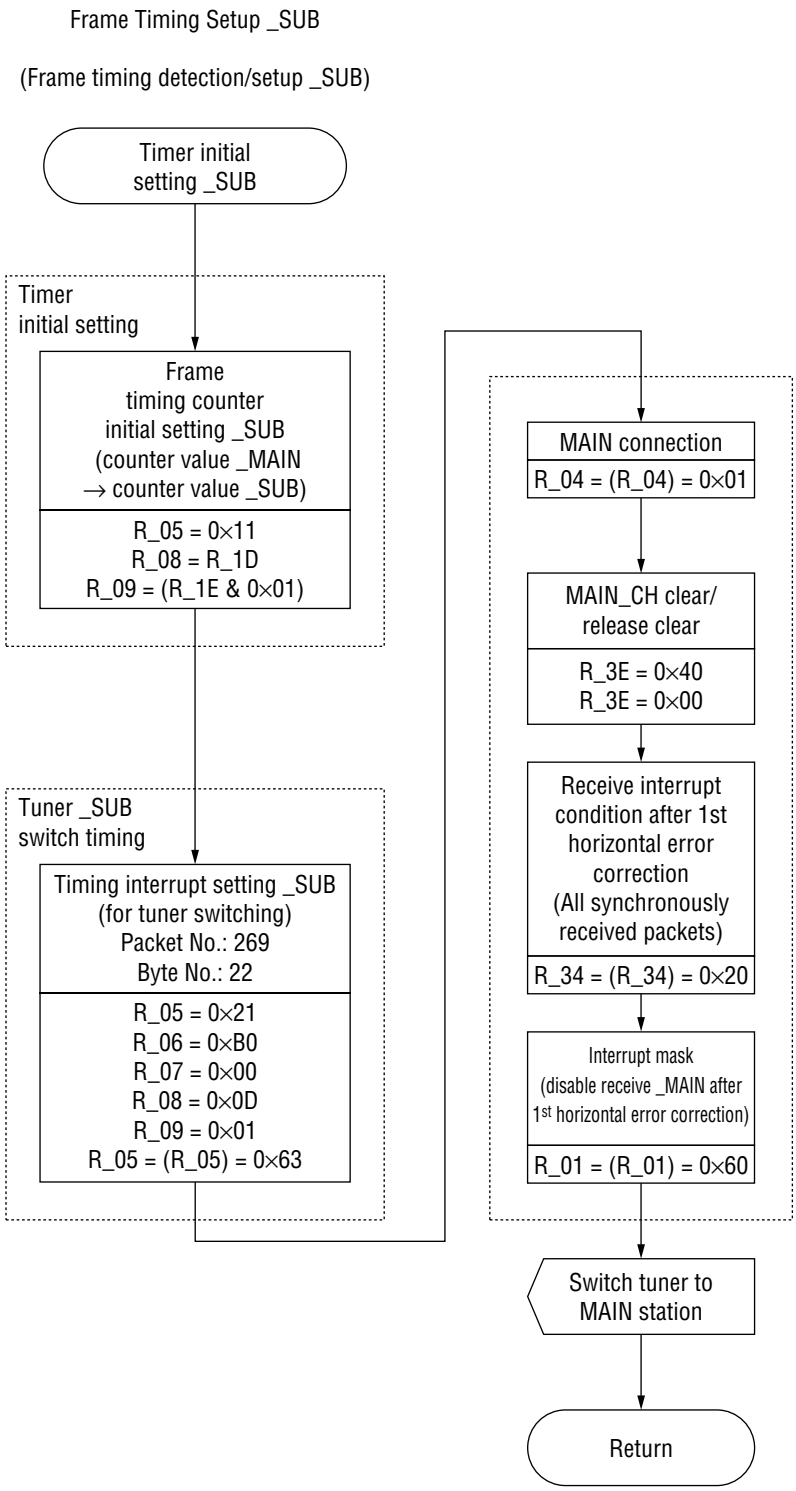


Figure 2.2.5.9 Frame Timing Setup _SUB

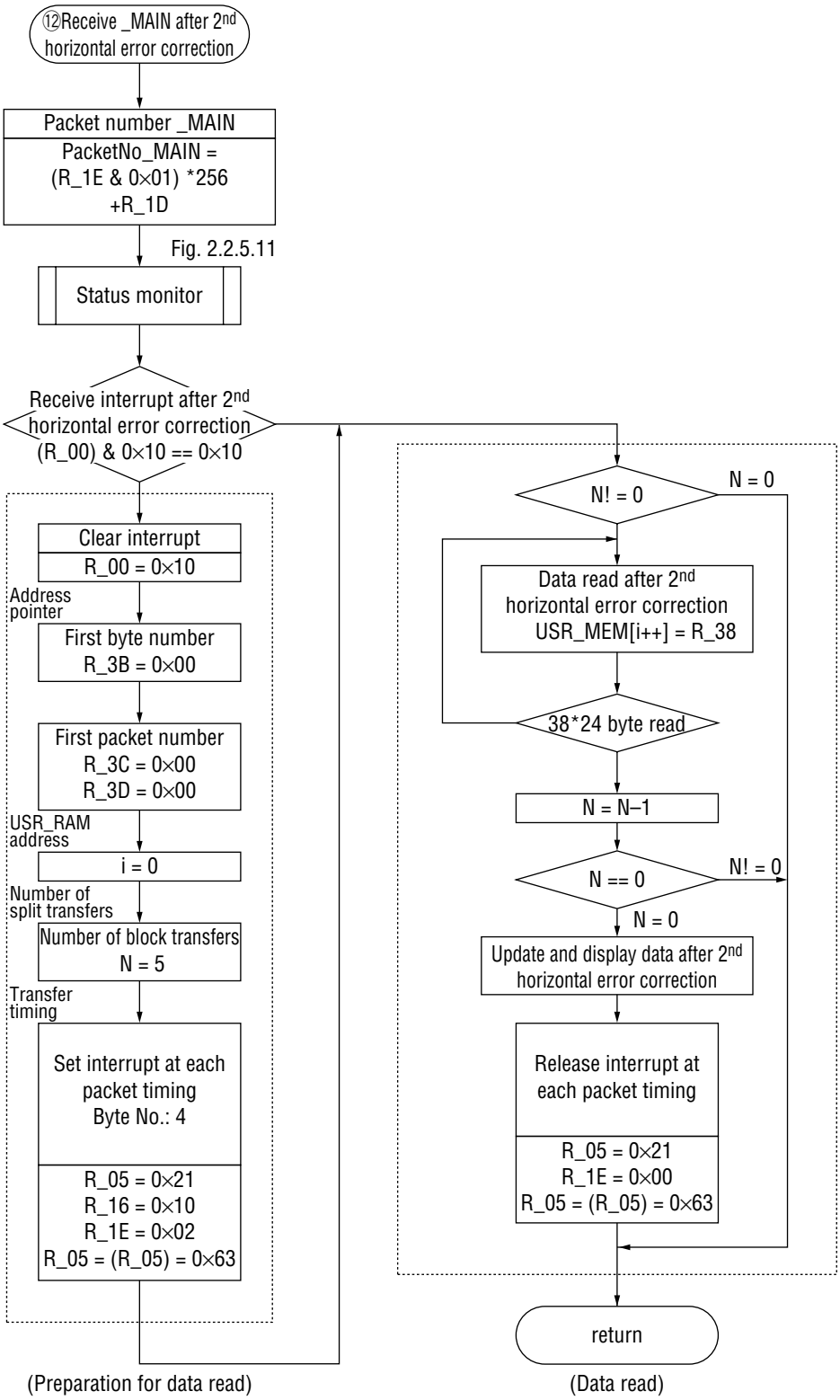


Figure 2.2.5.10 Reception After 2nd Horizontal Error Correction

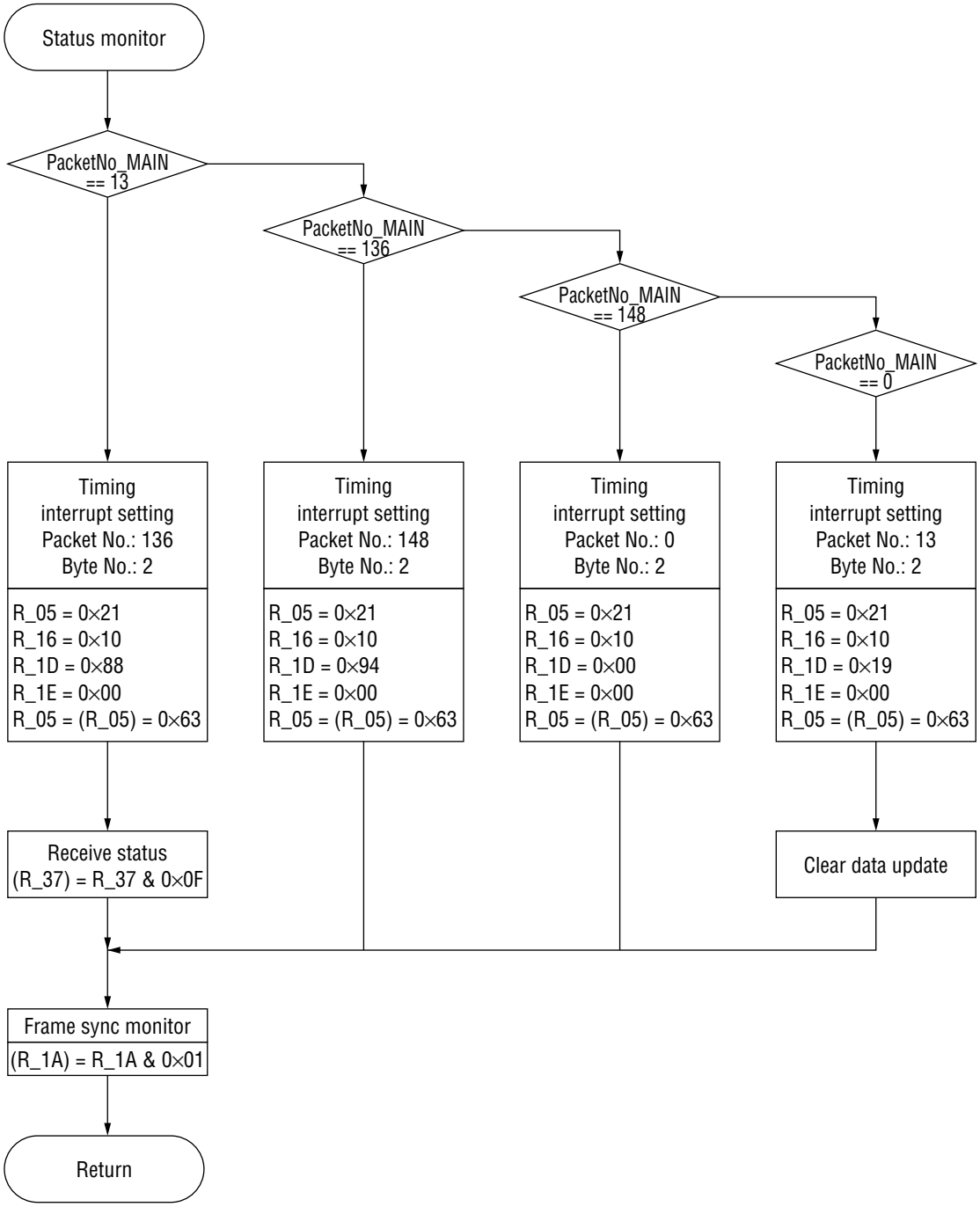


Figure 2.2.5.11 Status Monitor

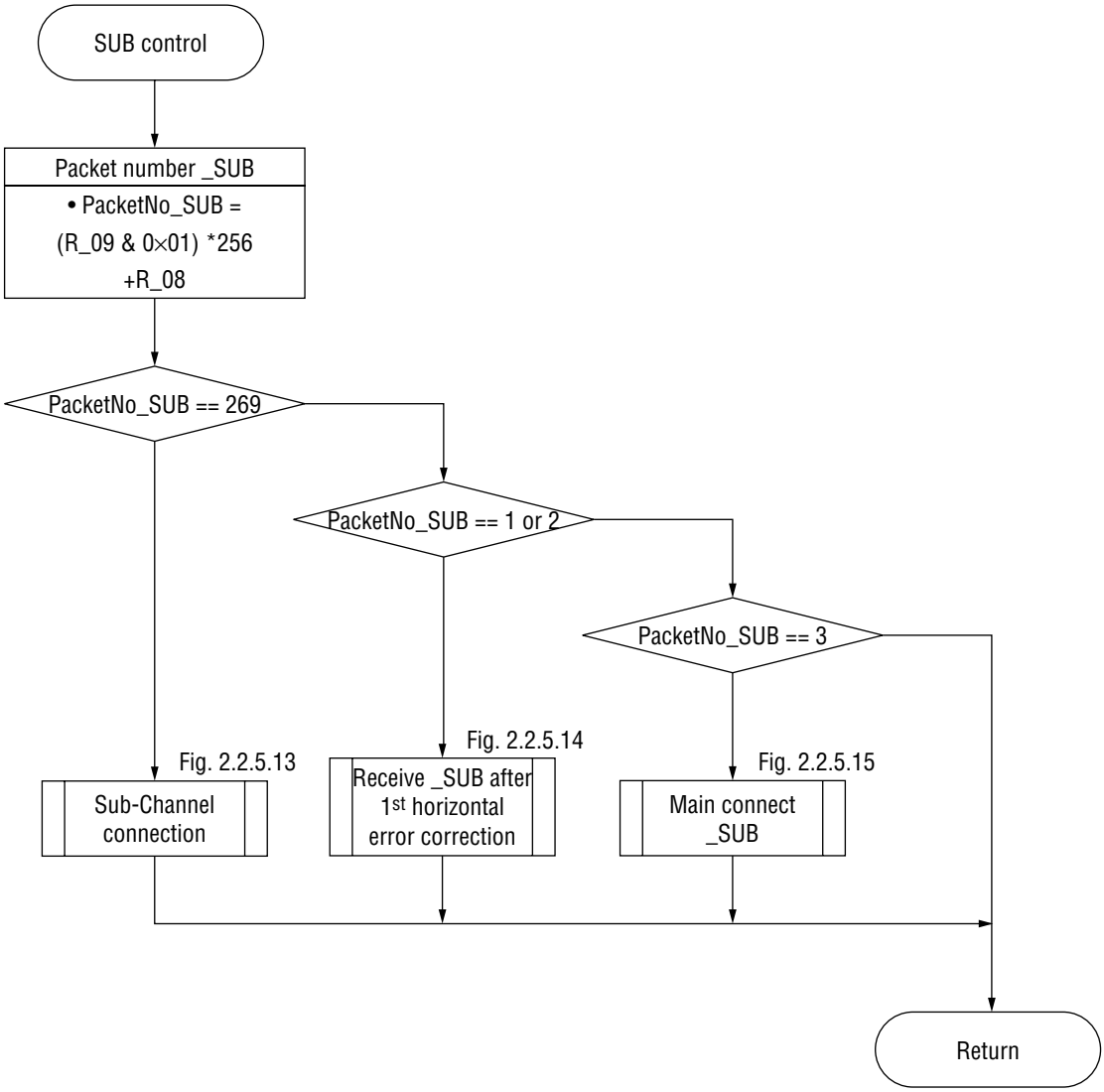


Figure 2.2.5.12 SUB Control

(Notes)

Subchannel synchronization error

In the early M956x series products, block synchronization error may occur depending on the subchannel receive timing.

- Synchronization error occurrence timing
  This error may occur when the main channel is switched to the subchannel and a synchronization signal matches with the switching timing.
- Countermeasure against error
  Set the number of allowable BIC errors to zero.
  Before SUB connection, insert 5 or more dummy bits (fixed patterns) of "1" after switching from the AIN pin to the ADETIN pin so as to have no BIC detection.
  Return the number of allowable BIC errors to the previous one.
  Fig. 2.4.5.13 shows a countermeasure flowchart.
  This flowchart can be used for an improved LSI.

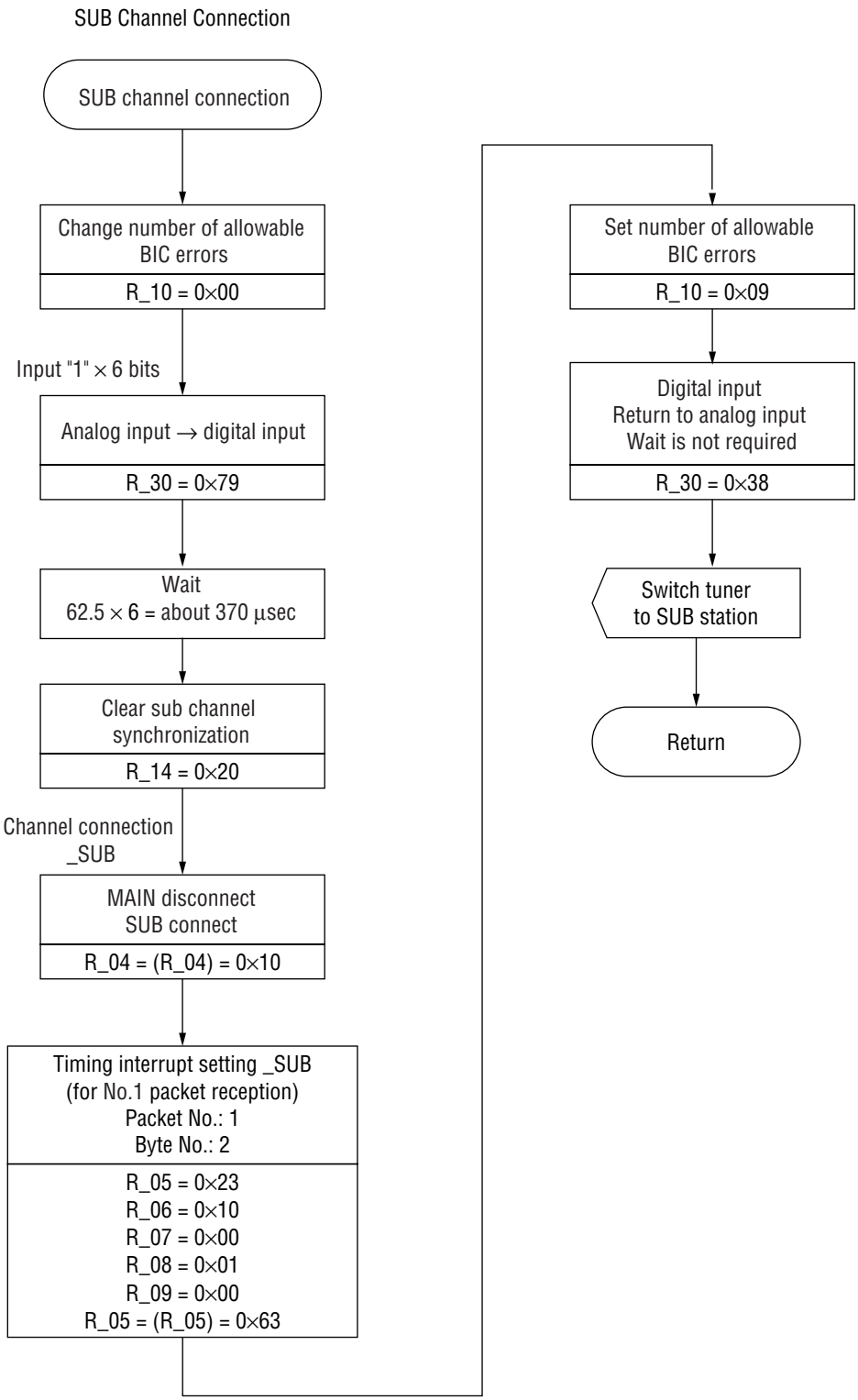


Figure 2.2.5.13 Sub Channel Connection

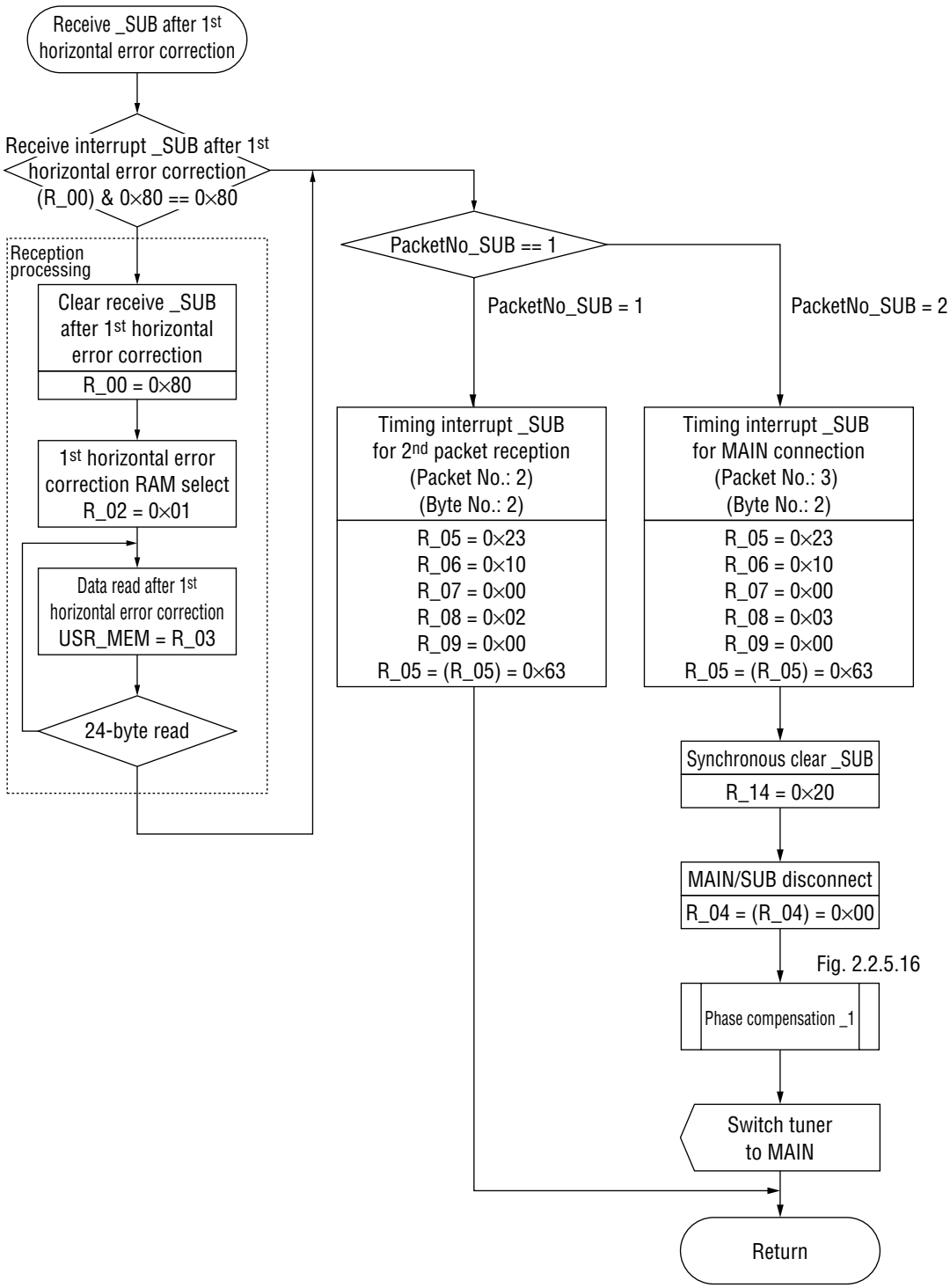


Figure 2.2.5.14 Receive _SUB After 1st Horizontal Error Correction

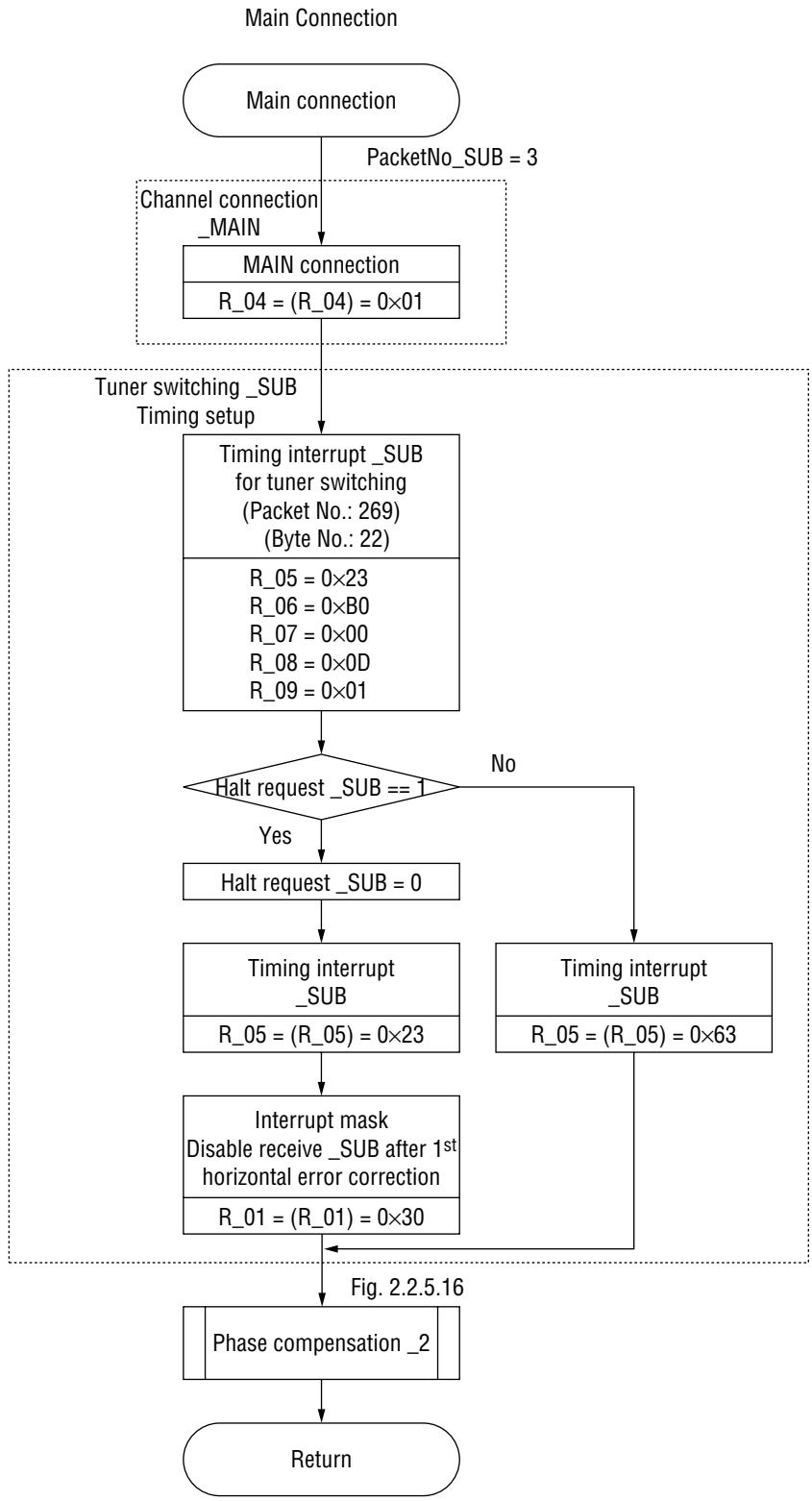


Figure 2.2.5.15 Main Channel Connection

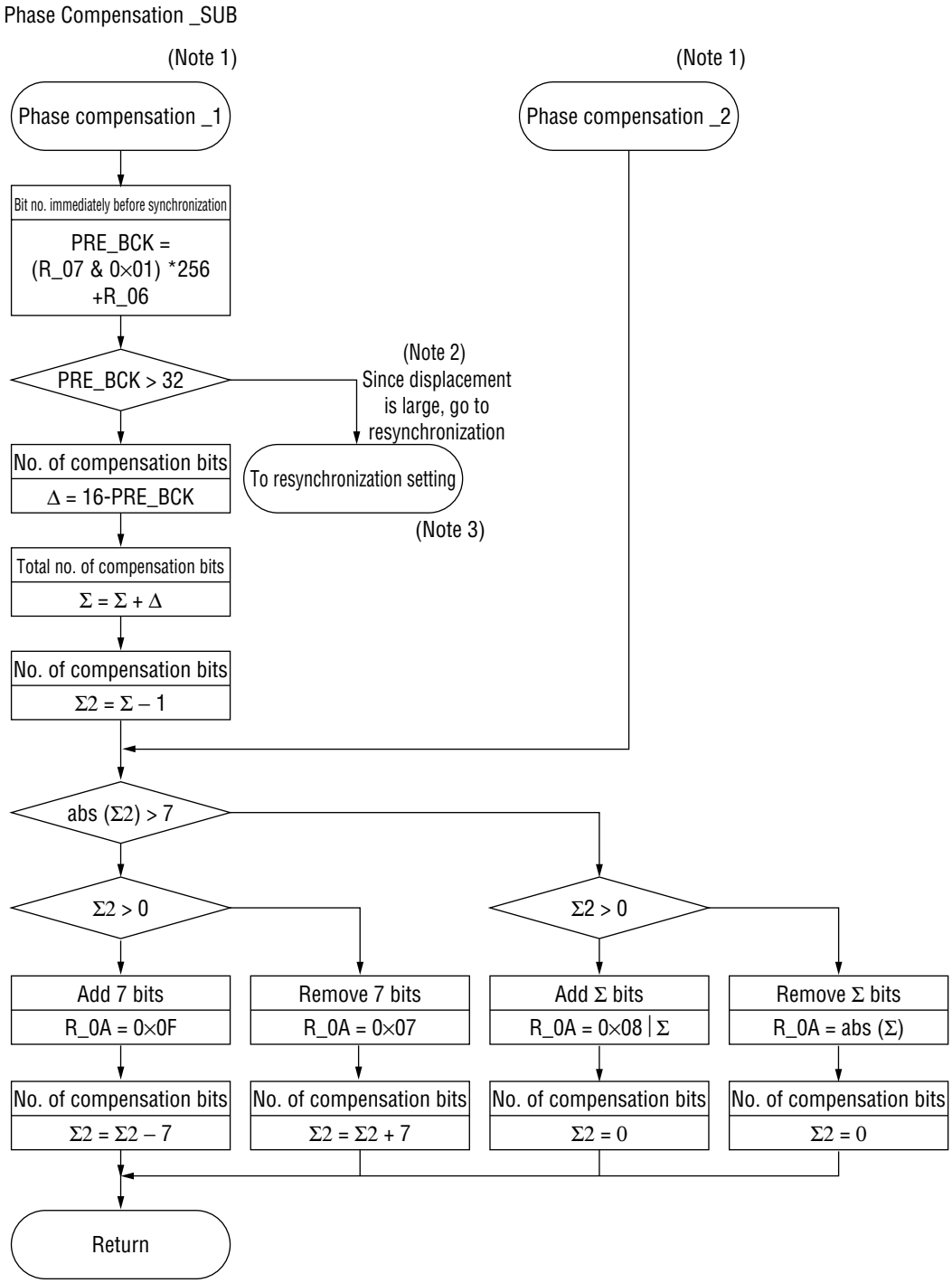


Figure 2.2.5.16 Bit Displacement Compensation

(Note 1) In this flow, since bit correction of the sub channel is divided and performed in 2 operations, correction of up to ±14 bits (max.) is possible.

(Note 2) Correction is necessary 2 or more times.
Alternatively, the packet number may be displaced.

(Note 3) Implement sub channel activation processing after the sub channel is haltted.

2.3 Layer4CRC Processing

This section shows the control flow of layer4CRC.

2.3.1 Control Flow

The control flow of layer4CRC is subject to change depending on layer4CRC/VICS and layer4CRC/DDJ modes or other modes.
Layer4CRC/VICS mode: For the MSM9564/65 only
Layer4CRC/DDJ mode: For the MSM9566/67 only

2.3.2 Description of Each Flow

- Control flow in other modes than layer4CRC and layer4CRC/DDJ modes
  This control flow is shown in Figure 2.3.1.
  Prepare a data group including data packets.

- Control flow in layer4CRC/VICS and layer4CRC/DDJ modes
  This control flow is shown in Figure 2.3.2.
  Prepare a data group and a prifix for the last packet.

2.3.3 User RAM

The contents of user RAM used in this flow are shown in Table 2.3.3.

Table 2.3.3 Contents of User RAM

1	L4Data	Layer4 data group read/write address
2	Prifix_0 Prifix_1 Prifix_2 Prifix_3	Data packet last data packet prifix for layer4CRC/VICS and layer4CRC/DDJ modes
3	i	Layer4CRC data group pointer

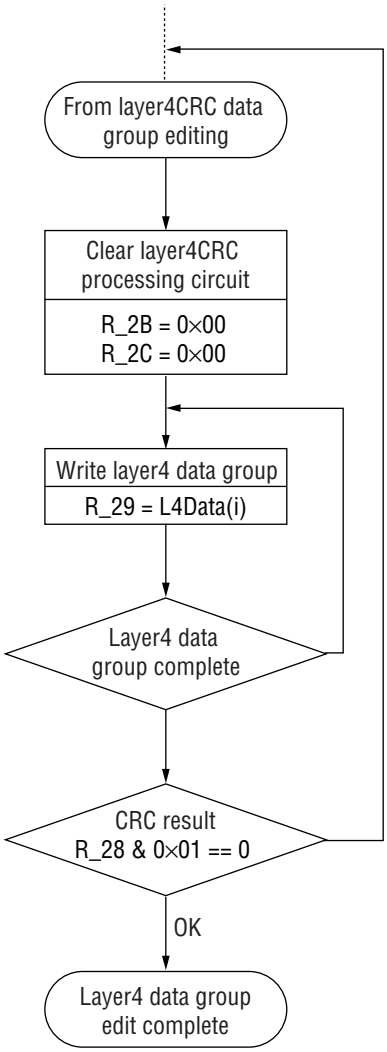
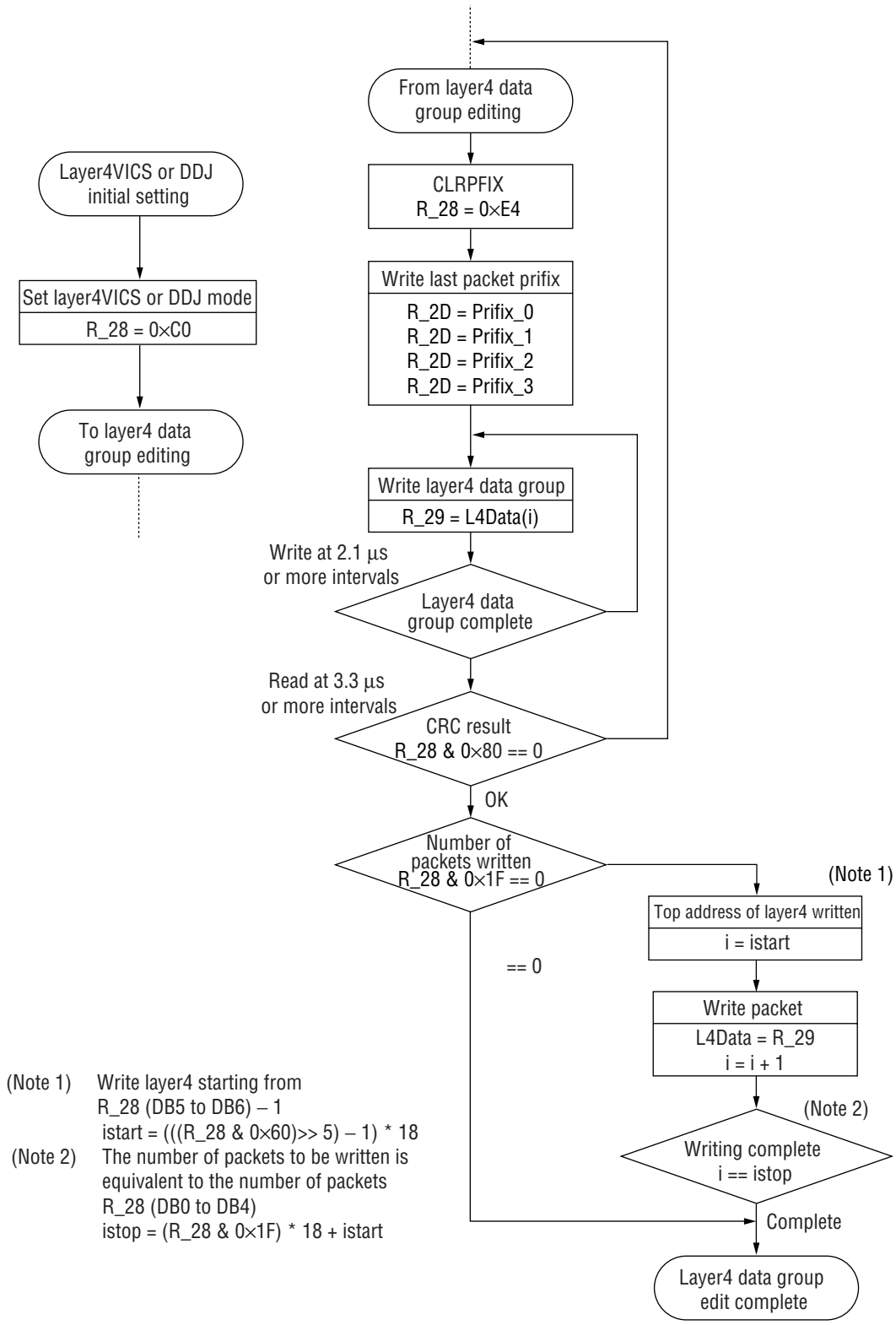


Figure 2.3.1 Modes other than Layer4CRC/VICS and Layer4CRC/DDJ Modes



(Note 1) Write layer4 starting from
R_28 (DB5 to DB6) – 1
istart = (((R_28 & 0×60)>> 5) – 1) * 18

(Note 2) The number of packets to be written is equivalent to the number of packets
R_28 (DB0 to DB4)
istop = (R_28 & 0×1F) * 18 + istart

Figure 2.3.2 Layer4CRC/VICS and Layer4CRC/DDJ Modes

MSM9562/63/66/67

User's Manual [Control Flow]

Version 0.9: January 1999
Version 1.0: December 2000

PEXL9562-67FLOW-10