OKI Semiconductor

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Previous version: Aug. 1998

MSM7620

Echo Canceler

GENERAL DESCRIPTION

The MSM7620 is an improved version of the MSM7520 with the same basic configuration. The MSM7620 includes following improvements: a modified through mode, timing control of the control pin input, and a thinner package. The MSM7620 also provides a pin-for-pin replacement with the MSM7520.
The MSM7620 is a low-power CMOS IC device for canceling echo (in an acoustic system or telephone line) generated in a speech path.
Echo is canceled (in digital signal processing) by estimating the echo path and generating a pseudo-echo signal.
Used as an acoustic echo canceler, the MSM7620 cancels the acoustic echo between the loud speaker and the microphone which occurs during hands free communication, such as on a car phone or a conference system phone.
Used as a line echo canceler, the device cancels the line echo impedance mismatching in a hybrid. In addition, a quality conversation is made possible by controlling the level and preventing howling with a howling detector, double talk detector, attenuation function and a gain control function, and by controlling the low level noise with a center clipping function.
The MSM7620 I/O interface supports μ-law PCM. The use of a single chip CODEC, such as the MSM7543, allows the configuration an economic and efficient echo canceler to be configured.

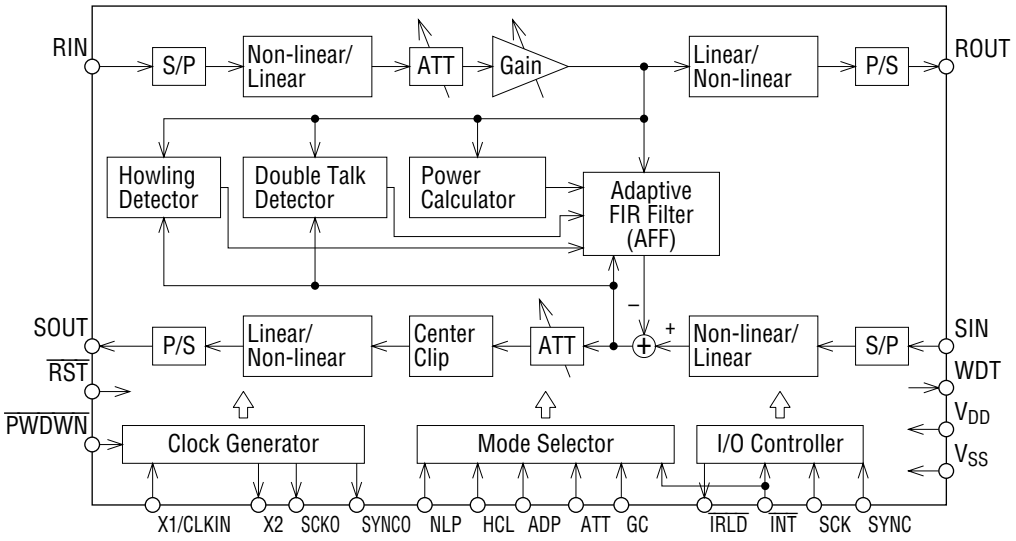
Note: If the object is to cancel line echo, the use of the MSM7602 is recommended, for the MSM7602 is provided with a howling detect control pin. In addition, the MSM7602, while having characteristics equivalent to the MSM7620, is packaged small.

FEATURES

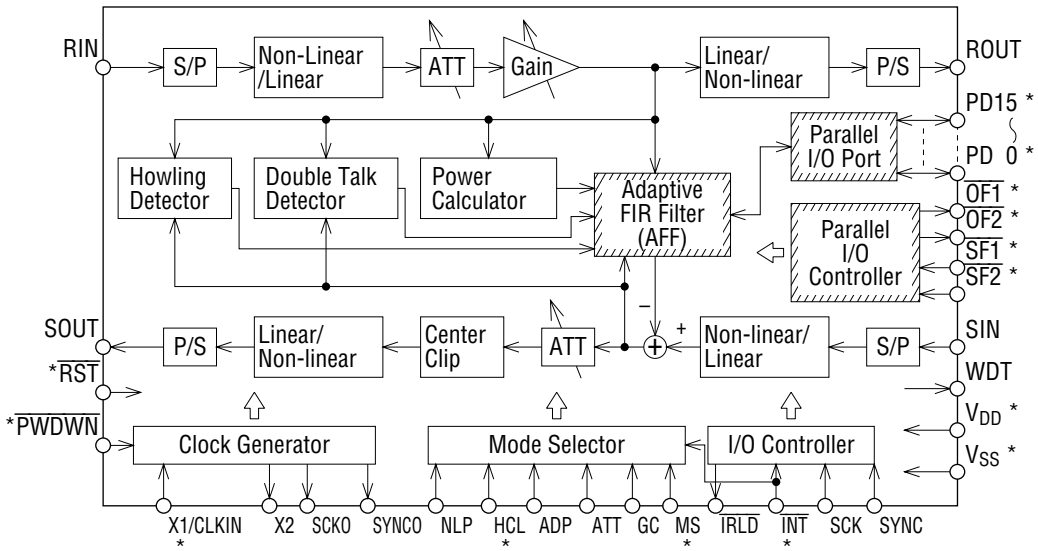
- Handles both acoustic echoes and telephone line echoes.
- Cancelable echo delay time:
  MSM7620-001 ..... For a single chip: 23 ms (max.)
  MSM7620-011 ..... For a cascade connection (can also be used for a single chip)
  Master chip: 23 ms (max.)
  Slave chip: 31 ms (max.)
  Cancelable up to 213 ms (one master plus six slaves)
  For a single chip: 23 ms (max.)
- Echo attenuation : 30 dB (typ.)
- Clock frequency : 18 MHz (36 MHz cannot be used)
  External input and internal oscillator circuit are provided.
- Power supply voltage : 5 V (4.5 V to 5.5 V)
- Power consumption : 150 mW (typ.) When powered down: 20 mW (typ.)
- Package options:
  32-pin plastic SSOP (SSOP32-P-640-0.80-K) (Product name : MSM7620-001GS-K)
  64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name : MSM7620-011GS-BK)

BLOCK DIAGRAM

MSM7620-001 (Single chip only)

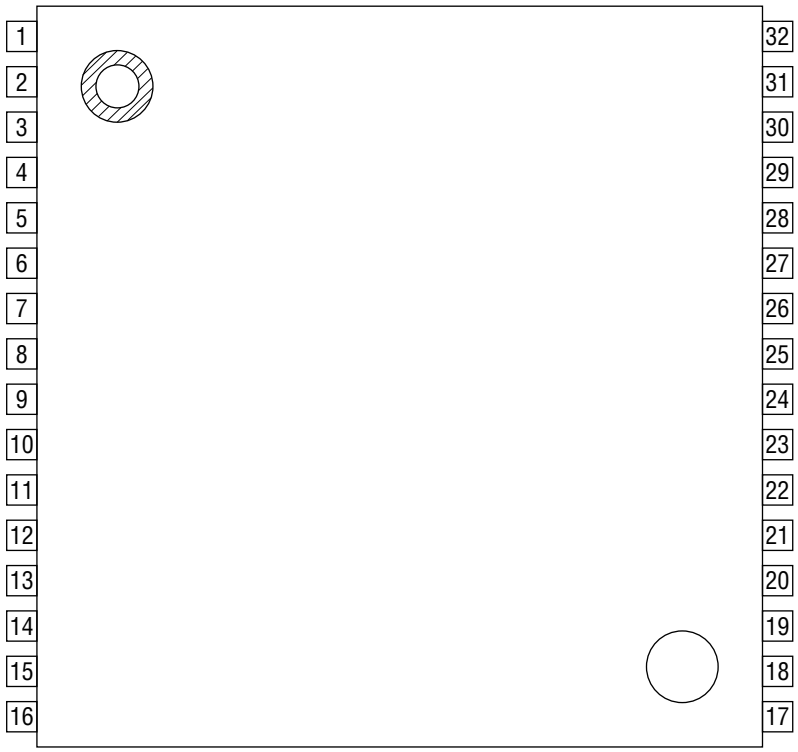


MSM7620-011 (Cascade connection or Single chip)



* If the MSM7620-011 is used in the slave mode, only the diagonally hatched blocks and the pins marked with * are used.

PIN CONFIGURATION (TOP VIEW)

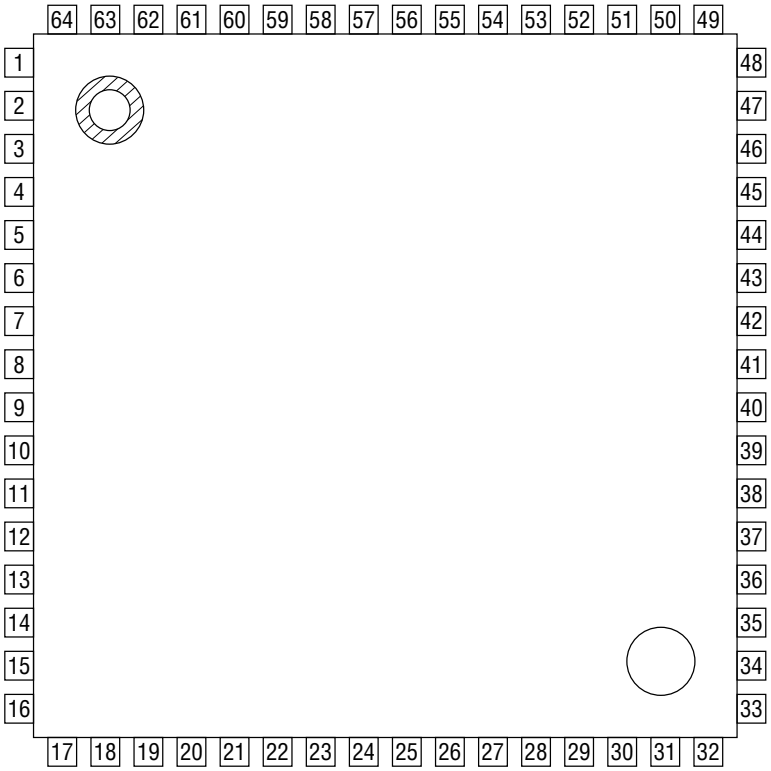


32-Pin Plastic SSOP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	*	9	SIN	17	*	25	SCKO
2	NLP	10	RIN	18	*	26	*
3	HCL	11	SCK	19	*	27	$\overline{RST}$
4	ADP	12	SYNC	20	X1/CLKIN	28	WDT
5	V_{SS}	13	SOUT	21	X2	29	GC
6	ATT	14	ROUT	22	*	30	*
7	$\overline{INT}$	15	*	23	$\overline{PWDWN}$	31	*
8	$\overline{IRLD}$	16	V_{SS}	24	SYNCO	32	V_{DD}

*: No connect pin

Note: Pin 26 of the MSM7520 is CKSEL, while that of the MSM7620 is in open state. It is possible to replace the MSM7520 with the MSM7620.



64-Pin Plastic SSOP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NLP	17	*	33	PD12	49	*
2	HCL	18	*	34	PD13	50	*
3	ADP	19	PD0	35	X1/CLKIN	51	PD14
4	MS	20	PD1	36	X2	52	PD15
5	ATT	21	PD2	37	*	53	*
6	$\overline{\text{INT}}$	22	PD3	38	$\overline{\text{PWDWN}}$	54	$\overline{\text{SF2}}$
7	*	23	PD4	39	*	55	$\overline{\text{OF1}}$
8	$\overline{\text{IRLD}}$	24	PD5	40	SYNCO	56	*
9	*	25	PD6	41	SCKO	57	*
10	SIN	26	PD7	42	*	58	*
11	RIN	27	PD8	43	*	59	$\overline{\text{SF1}}$
12	SCK	28	PD9	44	$\overline{\text{RST}}$	60	$\overline{\text{OF2}}$
13	SYNC	29	PD10	45	WDT	61	*
14	SOUT	30	PD11	46	GC	62	V_{DD}
15	ROUT	31	*	47	V_{DD}	63	*
16	V_{SS}	32	*	48	V_{DD}	64	*

*: No connect pin

Note: Pins 43, 53, and 61 of the MSM7520 are CKSEL, V_{DD}, and TST2 respectively. While these pins of the MSM7620 are in open state, it is possible to replace the MSM7520 with the MSM7620.

PIN DESCRIPTIONS (1/6)

Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
2	1	NLP	I	The control pin for the center clipping function. This forces the SOUT output to a minimum value (FF) when the SOUT signal is below -54 dBm0. Effective for reducing low-level noise. • Single Chip or Master Chip in a Cascade Connection "H": Center clip ON "L": Center clip OFF • Slave Chip in a Cascade Connection Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
3	2	HCL	I	The through mode control. When this pin is in the through mode, RIN and SIN data are output to ROUT and SOUT. At the same time, the coefficient of the adaptive FIR filter is cleared. • Single Chip or Master Chip in a Cascade Connection "H": Through mode "L": Normal mode (echo canceler operates) • Slave Chip in a Cascade Connection Same as master This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
4	3	ADP	I	AFF coefficient control pin. This pin stops updating of the adaptive FIR filter (AFF) coefficient and sets the coefficient to a fixed value, when this pin is configured to be the coefficient fix mode. This pin is used when holding the AFF coefficient which has been once converged. • Single Chip or Master Chip in a Cascade Connection "H": Coefficient fix mode "L": Normal mode (coefficient update) • Slave Chip in a Cascade Connection Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
—	4	MS	I	Selection of the Master Chip and slave chip when used in a cascade connection. "L": Single chip or master chip "H": Slave chip

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Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
6	5	ATT	I	Control for the ATT function that prevents howling by attenuators (ATT) for the RIN input and SOUT output. If there is input only to RIN, then the ATT for the SOUT output is activated. If there is no input to SIN, or if there is input to both SIN and RIN, the ATT for the RIN input is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. • Single Chip or Master Chip in a Cascade Connection "H": ATT OFF "L": ATT ON "L" is recommended for echo cancellation. • Slave Chip in a Cascade Connection • Fixed at "L" This input signal is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of the $\overline{RST}$ signal.
7	6	$\overline{INT}$	I	Interrupt signal which starts 1 cycle (8 kHz) of the signal processing. Signal processing starts when H-to-L transition is detected. • Single Chip or Master Chip in a Cascade Connection Connect the $\overline{IRLD}$ pin. • Slave Chip in a Cascade Connection Connect the $\overline{IRLD}$ pin of the master chip. $\overline{INT}$ input is invalid for 100 μs after reset due to initialization. Refer to the control pin connection example.
8	8	$\overline{IRLD}$	O	Load detection signal when the SIN and RIN serial input data is loaded in the internal registers. • Single Chip Connect to the $\overline{INT}$ pin. • Master Chip in a Cascade Connection Connect to the $\overline{INT}$ pin of the master chip and all the slave chips. • Slave Chip in a Cascade Connection Leave open. Refer to the control pin connection example.
9	10	SIN	I	Transmit serial data. Input the μ-law PCM signal synchronized to SYNC and SCK. Data is read in at the fall of SCK.

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Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
10	11	RIN	I	Receive serial data. Input the μ-law PCM signal synchronized to SYNC and SCK. Data is read in at the fall of SCK.
11	12	SCK	I	Clock pin for transmit/receive serial data. This pin uses the external SCK or the SCKO. Input the PCM CODEC transmit/receive clock (64 to 2048 kHz).
12	13	SYNC	I	Sync signal for transmit/receive serial data. This pin uses the external SYNC or SYNCO. Input the PCM CODEC transmit/receive sync signal (8 kHz).
13	14	SOUT	0	Transmit serial data. This pin outputs the μ-law PCM signal synchronized to SYNC and SCK. This pin is in a high impedance state while there is no data output.
14	15	ROUT	0	Receive serial data. This pin outputs the μ-law PCM signal synchronized to SYNC and SCK. This pin is in a high impedance state while there is no data output.
—	19	PD0	I/O	Bidirectional bus for parallel data transfer between the Master Chip and Slave Chip when used in a cascade connection. The PD15 pin corresponds to MSB. This pin is in a high impedance state while there is no data output. Data is loaded in at the falling edge of $\overline{SFx}$.
	|	|		
—	30	PD11		
—	33	PD12		
—	34	PD13		
—	51	PD14		
—	52	PD15		
20	35	X1/CLKIN	I	External input for the basic clock or for the crystal oscillator. Input the basic clock (18 MHz). Refer to the internal clock generator circuit example.
21	36	X2	0	Crystal oscilator. Used to configure the oscillation circuit. Refer to the internal clock generator circuit example. When inputting the basic clock externally, insert a 5 pF capacitor with excellent high frequency characteristics between X2 and GND.
23	38	$\overline{PWDWN}$	I	Power-down mode control. "L": Power-down mode "H": Normal operation mode During power-down, all input pins are disabled and output pins are in the following sates : High impedance : SOUT, ROUT, PD0 to 15 "L": SYNCO, SCKO "H": $\overline{OF1}$, $\overline{OF2}$ Holds the last state : WDT, $\overline{IRLD}$ Not affected: X2, MCKO Reset after power-down is released.

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Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
24	40	SYNCO	O	8 kHz sync signal for the PCM CODEC. Connect this pin to the SYNC pin and the PCM CODEC transmit/receive sync pin. Leave it open if using an external SYNC.
25	41	SCKO	O	Transmit clock signal (200 kHz) for the PCM CODEC. Connect this pin to the SCK pin and the PCM CODEC transmit/receive clock pin. Not affected by reset. Outputs "0" during power-down. Leave it open if using an external SCK.
27	44	$\overline{RST}$	I	Reset signal. "L": Reset mode "H": Normal operation mode During initialization, input signals, except for $\overline{PWDWN}$ are disabled for 100 μs after reset (after $\overline{RST}$ is returned from "L" to "H"). Input the basic clock during the reset. Output pins during reset are in the following sates : High impedance: SOUT, ROUT, PD0 to 15 "L": WDT "H": $\overline{OF1}$, $\overline{OF2}$ Not affected: X2, SYNCO, SCKO, $\overline{IRLD}$, MCKO After the power is turned on, initialize the LSI's internal registers by your execution of H→L sequence 1μs later than the master clock starts normal oscilation. This LSI starts a normal operation by releasing this pin to H after the H→L sequence above. Here, this pin must stay L for 1μs or longer.
28	45	WDT	O	Test pin. Leave this pin open.

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Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
29	46	GC	I	Input signal for the gain controller when RIN input is controlled and the RIN input level is controlled and howling is prevented. The gain controller adjusts the RIN input level when it is –20 dBm0 or above. RIN input levels from –20 to –11.5 dBm0 will be suppressed to –20 dBm0 in the attenuation range from 0 to 8.5 dB. RIN input levels above –11.5 dBm0 will always be attenuated by 8.5 dB. • Single Chip or Master Chip in a Cascade Connection "H": Gain control ON "L": Gain control OFF "H" is recommended for echo cancellation. • Slave Chip in a Cascade Connection Fixed at "L" This pin is loaded in synchronization with the falling edge of the $\overline{INT}$ signal or the rising edge of $\overline{RST}$.
—	54	$\overline{SF2}$	I	Parallel data transfer flag. • Single Chip Fixed at "H" • Master Chip in a Cascade Connection Fixed at "H" • Slave Chip in a Cascade Connection Connect $\overline{OF2}$ of the master chip to the first stage slave chip. Connect $\overline{OF1}$ of the previous stage slave chip to the second and later stage slave chips. Refer to the control pin connection example.
—	55	$\overline{OF1}$	O	Parallel data transfer flag. • Single Chip Leave this pin open. • Master Chip in a Cascade Connection Connect to the $\overline{SF1}$ of all slaves. • Slave chip in a Cascade Connection Connect to the $\overline{SF2}$ of the next stage slave chip. Connect the last stage slave chip to the $\overline{SF1}$ of the master chip. Refer to the control pin connection example.

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Pin		Symbol	Type	Description
32-pin SSOP	64-pin QFP			
—	59	$\overline{SF1}$	I	Parallel data transfer flag. • Single Chip Connect $\overline{OF2}$. • Master Chip in a Cascade Connection Connect $\overline{OF1}$ of the last stage slave chip. • Slave Chip in a Cascade Connection Connect $\overline{OF1}$ of master chip for all slave chips. Refer to the control pin connection example.
—	60	$\overline{OF2}$	O	Parallel data output flag. • Single Chip Connect to $\overline{SF1}$. • Master Chip in a Cascade Connection Connect to $\overline{SF2}$ of the first stage slave chip. • Slave Chip in a Cascade Connection Leave open. Refer to the control pin connection example.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D		1	W
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.5	5	5.5	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
Input High Voltage	V_{IH}	Pins other than X1	2.4	—	V_{DD}	V
		X1 pin	3.5	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0	—	0.8	V
Operating Temperature	Ta	—	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Output High Voltage	V_{OH}	I_{OH} = 40 µA		4.2	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0	—	0.4	V
High Level Input Current	I_{IH}	$V_{IH} = V_{DD}$		—	0.1	10	µA
Low Level Input Current	I_{IL}	V_{IL} = V_{SS} to V_{DD}	$\overline{SF1}$, $\overline{SF2}$ with pull-up	–100	–50	–10	µA
			Input other than the above	–10	–0.1	—	µA
High Level Output Current	I_{OZH}	$V_{OH} = V_{DD}$		—	0.1	10	µA
Low Level Output Current	I_{OZL}	V_{OL} = V_{SS} to V_{DD}	PD15 to PD0 with pull-up	–100	–50	+10	µA
			Input other than the above	–10	–0.1	—	µA
Power Supply Current (Operating)	I_{DDO}	—		—	30	40	mA
Power Supply Current(Stand-by)	I_{DDS}	When extarnal input is used as basic clock		—	4	5	mA
$\overline{PWDWN}$="L"		When oscillation circuit is used as basic clock		—	6	8	mA
Input Capacitance	C_I	—		—	—	15	pF
Output Load Capacitance	C_{LOAD}	—		—	—	20	pF

Echo Canceler Characteristics (Refer to Characteristics Diagram)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Attenuation	L_{RES}	R_{IN} = –10 dBm0 (5 kHz band white noise) E. R. L. (echo return loss) = 6 dB T_D = 20 ms ATT, GC, NLP: OFF	—	30	—	dB
Cancelable Echo Delay Time for a Single Chip or a Master Chip in a Cascade	T_D	R_{IN} = –10 dBm0 (5 kHz band white noise) E.R.L. = 6 dB ATT, GC, NLP: OFF	—	—	23	ms
Cancelable Echo Delay Time for a Slave Chip in a Cascade	T_{DS}		—	—	31	ms

AC Characteristics

(Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	f_C	—	17.5	18.0	18.5	MHz
Clock Cycle Time	t_{MCK}	—	54.1	55.56	57.1	ns
Clock Duty Ratio	t_{DMC}	—	40	50	60	%
Clock "H" Level Pulse Width	t_{MCH}	—	23.5	—	—	ns
Clock "L" Level Pulse Width	t_{MCL}	—	23.5	—	—	ns
Clock Rise Time	t_r	—	—	—	5	ns
Clock Fall Time	t_f	—	—	—	5	ns
Sync Clock Output Time	t_{DCM}	—	—	—	100	ns
Internal Sync Clock Frequency	f_{CO}	f_c = 18 MHz	—	200	—	kHz
Internal Sync Clock Output Cycle Time	t_{CO}	f_c = 18 MHz	—	5	—	µs
Internal Sync Clock Duty Ratio	t_{DCO}	f_c = 18 MHz	—	50	—	%
Internal Sync Signal Output Delay Time	t_{DCC}	f_c = 18 MHz	—	—	5	ns
Internal Sync Signal Period	t_{CYO}	f_c = 18 MHz	—	125	—	µs
Internal Sync Signal Output Width	t_{WSO}	f_c = 18 MHz	—	t_{CO}	—	µs
Transmit/receive Operation Clock Frequency	f_{SCK}	—	64	—	2048	kHz
Transmit/receive Sync Clock Cycle Time	t_{SCK}	—	0.488	—	15.6	µs
Transmit/receive Sync Clock Duty Ratio	t_{DSC}	—	40	50	60	%
Transmit/receive Sync Signal Period	t_{CYC}	—	123	125	—	µs
Sync Timing	t_{XS}	—	45	—	—	ns
	t_{SX}	—	45	—	—	ns
Sync Signal Width	t_{WSY}	—	t_{SCK}	—	t_{CYC}–t_{SCK}	µs
Receive Signal Setup Time	t_{DS}	—	45	—	—	ns
Receive Data Hold Time	t_{DH}	—	45	—	—	ns
Receive Data Input Time	t_{ID}	—	—	$7t_{SCK}$	—	µs
IRLD Signal Output Delay Time	t_{DIC}	—	—	—	138	ns
IRLD Signal Output Width	t_{WIR}	—	—	t_{SCK}	—	µs
Serial Output Delay Time	t_{SD}	—	—	—	90	ns
	t_{XD}	—	—	—	90	

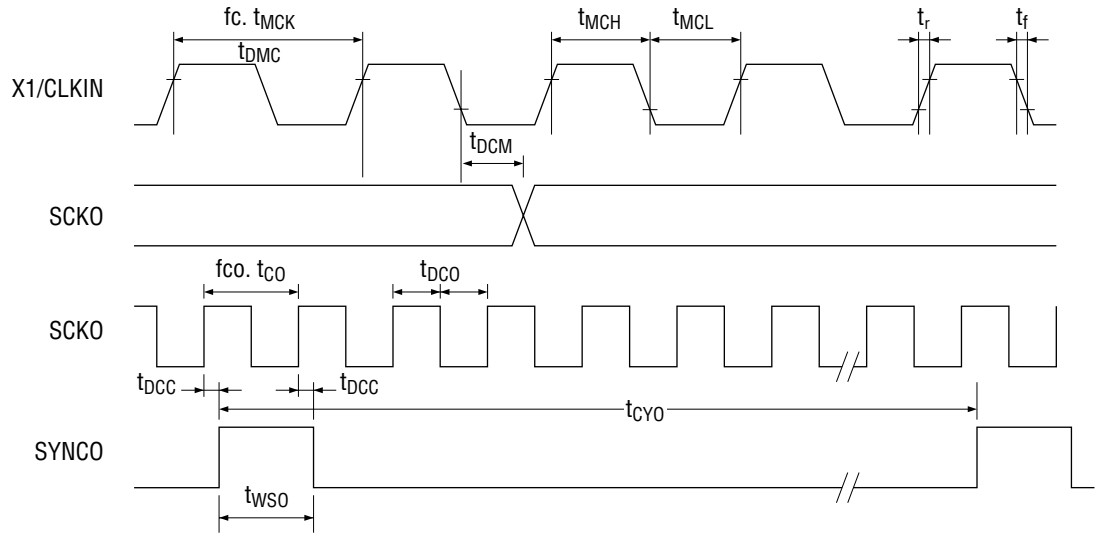
AC Characteristics (Continued)

(Ta = –40°C to +85°C)

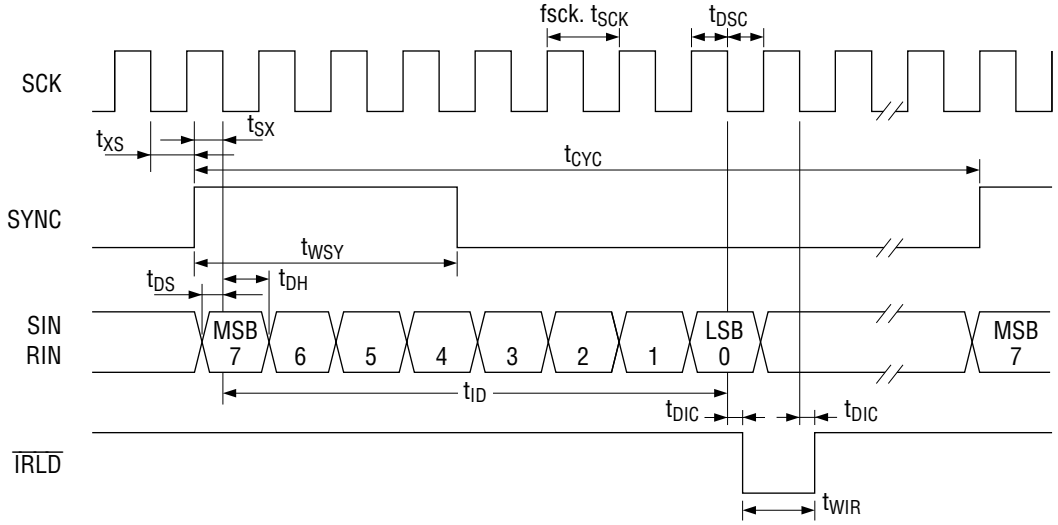
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Signal Input Width	t_{WR}	—	1	—	—	µs
Reset Start Time	t_{DRS}	—	5	—	—	ns
Reset End Time	t_{DRE}	—	—	—	52	ns
Processing Operation Start Time	t_{DIT}	—	100	—	—	µs
Power Down Start Time	t_{DPS}	—	—	—	111	ns
Power Down End Time	t_{DPE}	—	—	—	15	ns
Control Pin Setup Time ($\overline{INT}$)	t_{DTS}	—	20	—	—	ns
Control Pin Hold Time ($\overline{INT}$)	t_{DTH}	—	120	—	—	ns
Control Pin Setup Time ($\overline{RST}$)	t_{DSR}	—	20	—	—	ns
Control Pin Hold Time ($\overline{RST}$)	t_{DHR}	—	10	—	—	ns
Parallel Data Output Signal Width	t_{WPD}	—	—	$2t_{MCK}$	—	ns
Flag Signal Output Time	t_{DF}	—	—	t_{MCK}	—	ns
Flag Signal Output Width	t_{WFO}	—	—	$t_{MCK}/2$	—	ns
Flag Signal Input Width	t_{WFI}	$\overline{OFz}$ connected to $\overline{SFx}$	—	t_{WFO}	—	ns
Data Read Setup Time	t_{FS}	—	—	20	—	ns
Data Read Hold Time	t_{FH}	—	—	10	—	ns

TIMING DIAGRAM

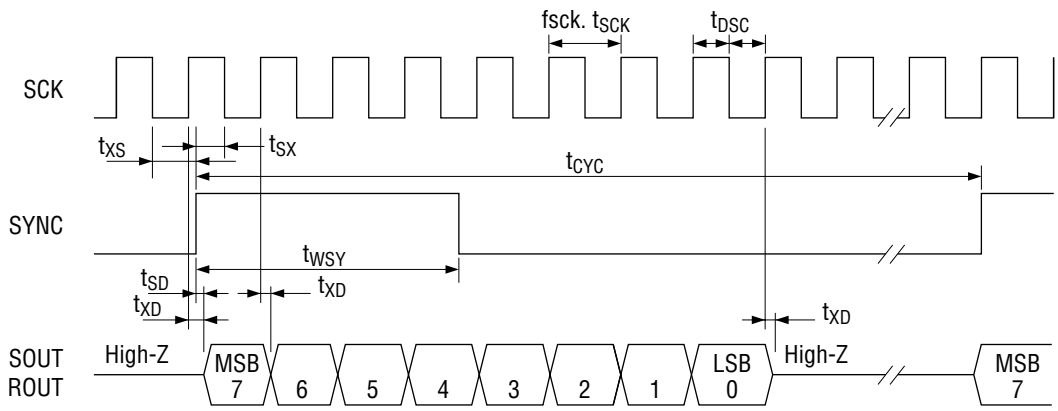
Clock Timing



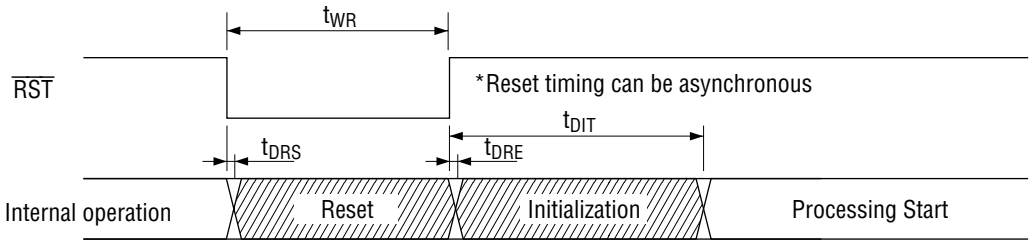
Serial Input Timing



Serial Output Timing

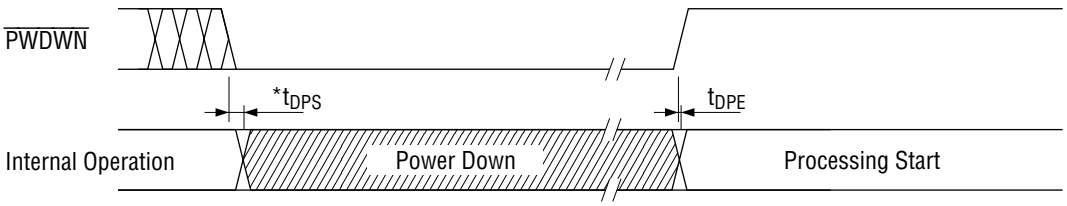


Operation Timing After Reset



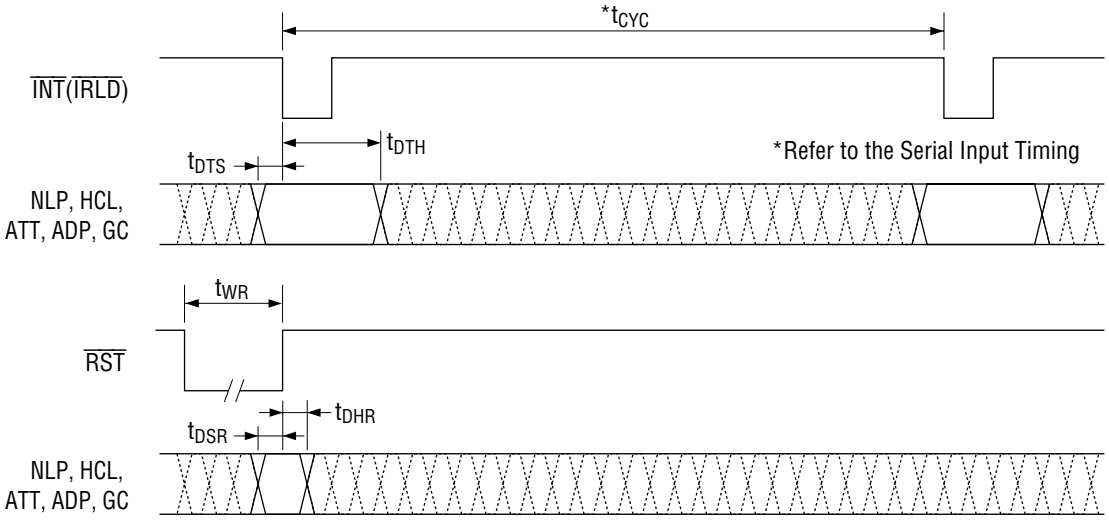
Note: $\overline{INT}$ is invalid in the diagonally shaded interval.

Power Down Timing

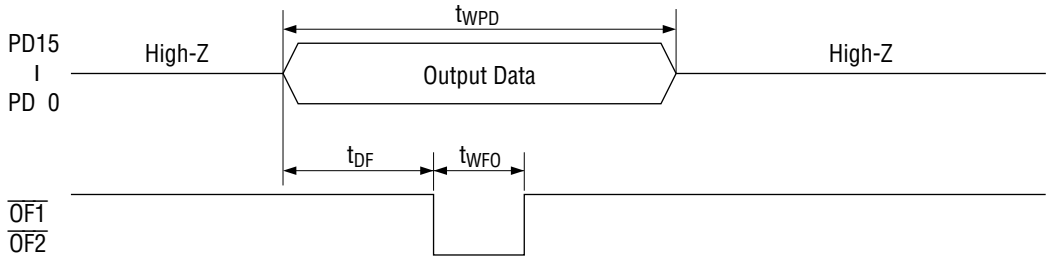


*Input MCK in the t_{DPS} interval.

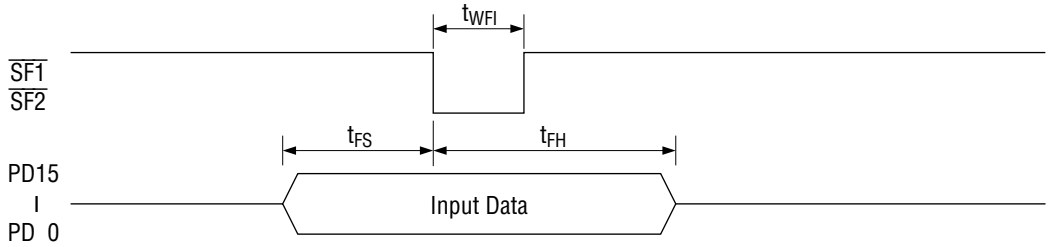
Control Pin Load-in Timing



Parallel Output Timing



Parallel Input Timing

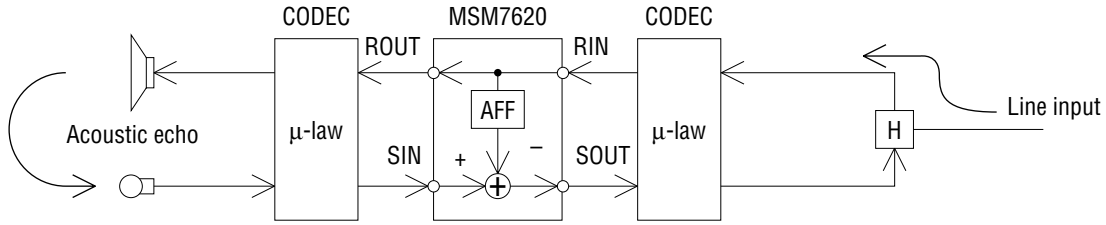


HOW TO USE THE MSM7620

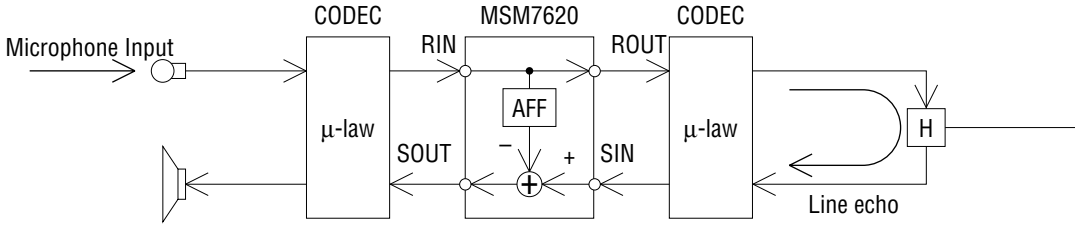
The MSM7620 cancels the echo which returns to SIN using the RIN signal.
Connect the base signal to the R-side and the echo generated signal to the S-side.

Connection Methods According to Echos

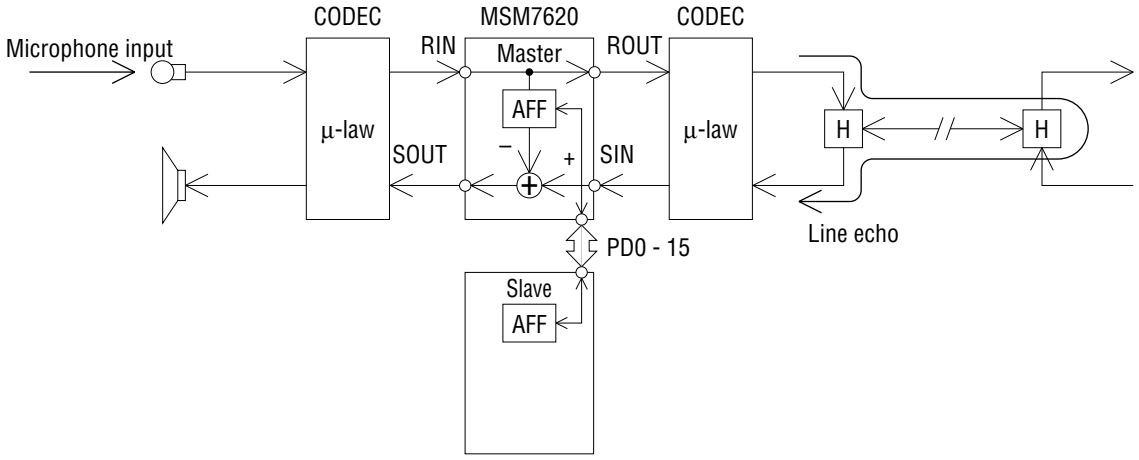
Example 1: Canceling acoustic echo (to handle acoustic echo from line input)



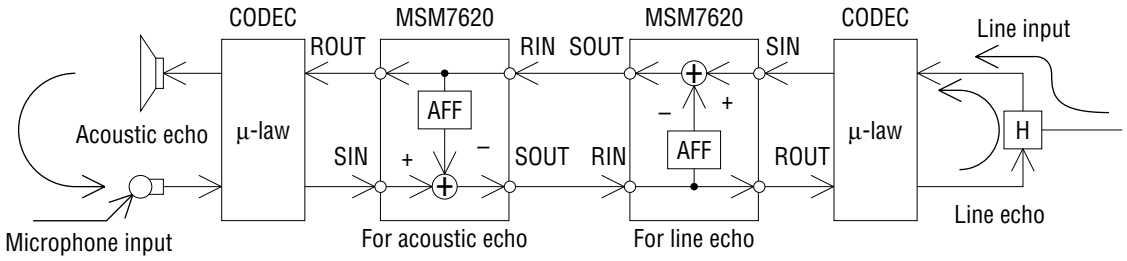
Example 2: Canceling line echo (to handle line echo from microphone input)



Example 3: Canceling line echo in a cascade connection
(to handle line echo from microphone input)

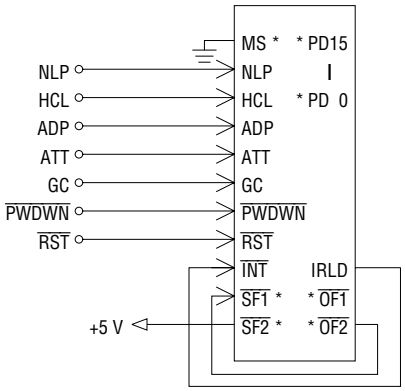


Example 4: Canceling of both acoustic echo and line echo
(to handle both acoustic echo from line input and line echo from microphone input)



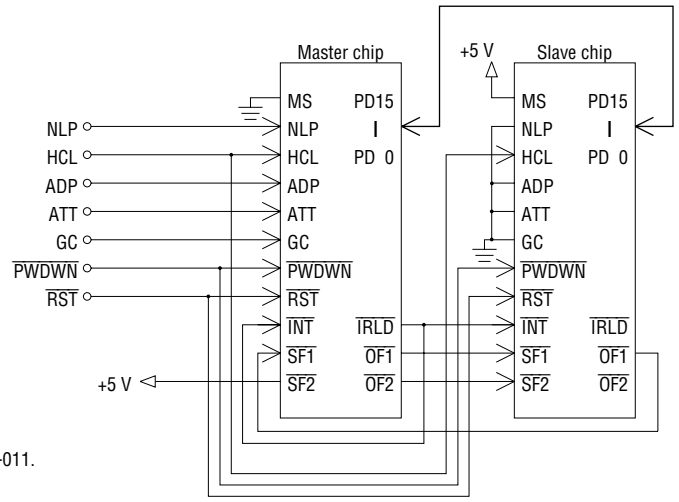
Control Pin Connection Example

Single Chip Connection

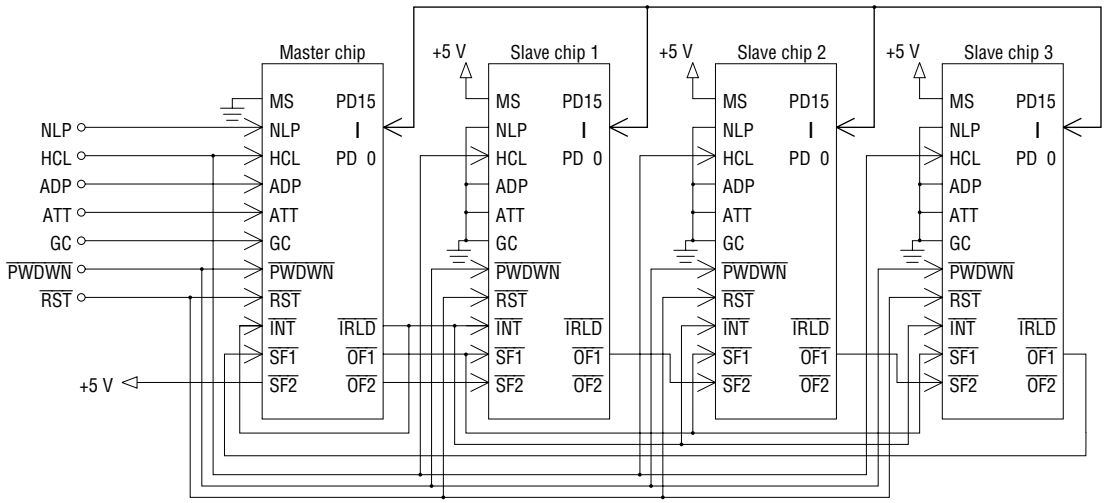


Asterisk * mark indicates a pin only for the MSM7620-011.

Two-stage Cascade Connection
Master + (slave × 1)

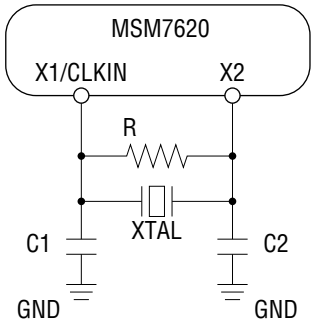


Four-stage Cascade Connection
Master + (slave × 3)



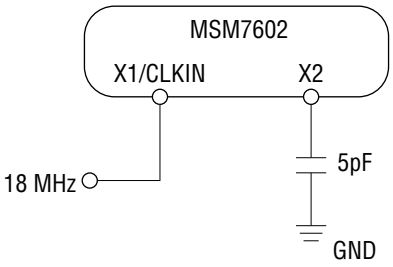
Clock Circuit Example

Internal clock generator circuit



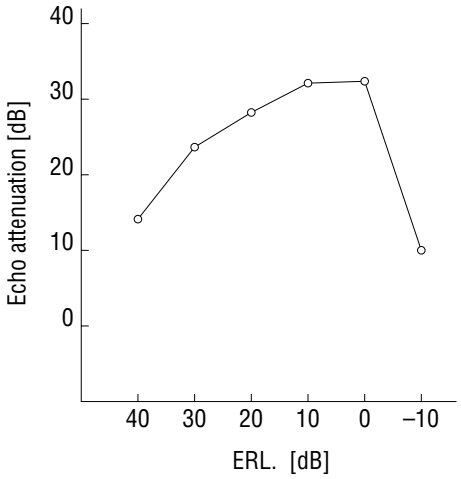
XTAL : 18 MHz
R : 1 MΩ
C1 : 27 pF
C2 : 27 pF

External clock input circuit



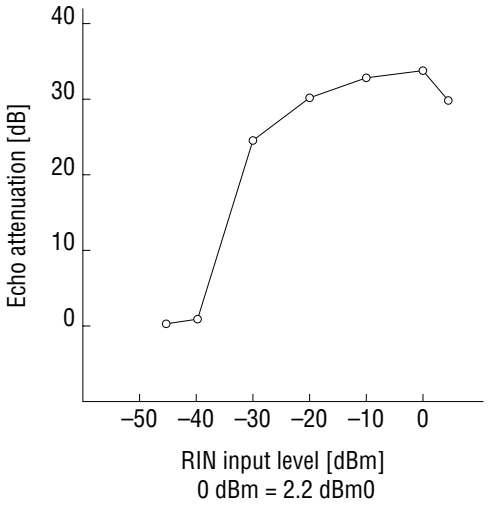
ECHO CANCELER CHARACTERISTICS DIAGRAM

ERL vs. echo attenuation



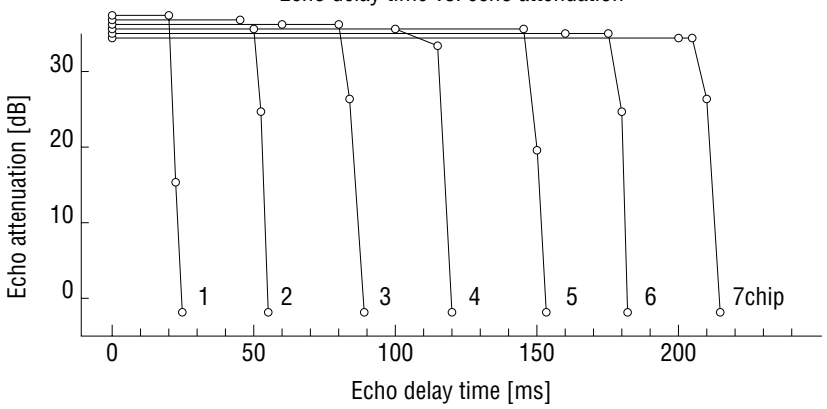
Measurement Conditions
RIN input = –10 dBm 5 kHz band white noise
(0 dBm = 2.2 dBm0)
Echo delay time T_D = 20 ms
ATT, GC, NLP = OFF

RIN input level vs. echo attenuation



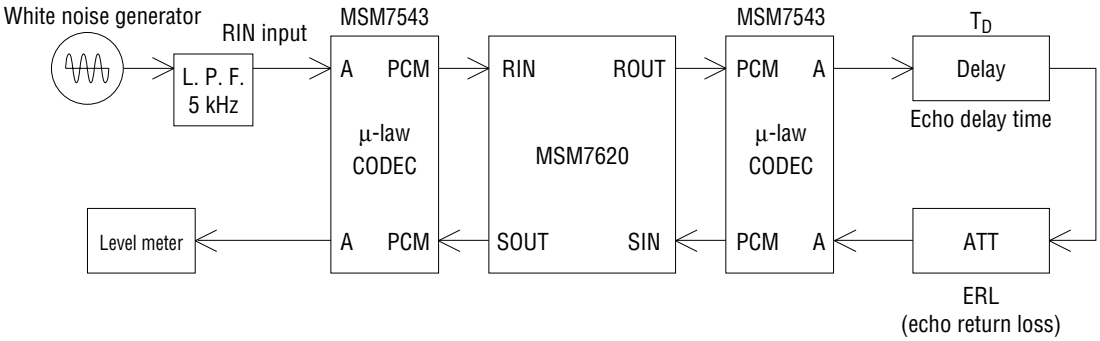
Measurement Conditions
RIN input: 5 kHz band white noise
Echo delay time T_D = 20 ms
ERL = 6 dB
ATT, GC, NLP = OFF

Echo delay time vs. echo attenuation



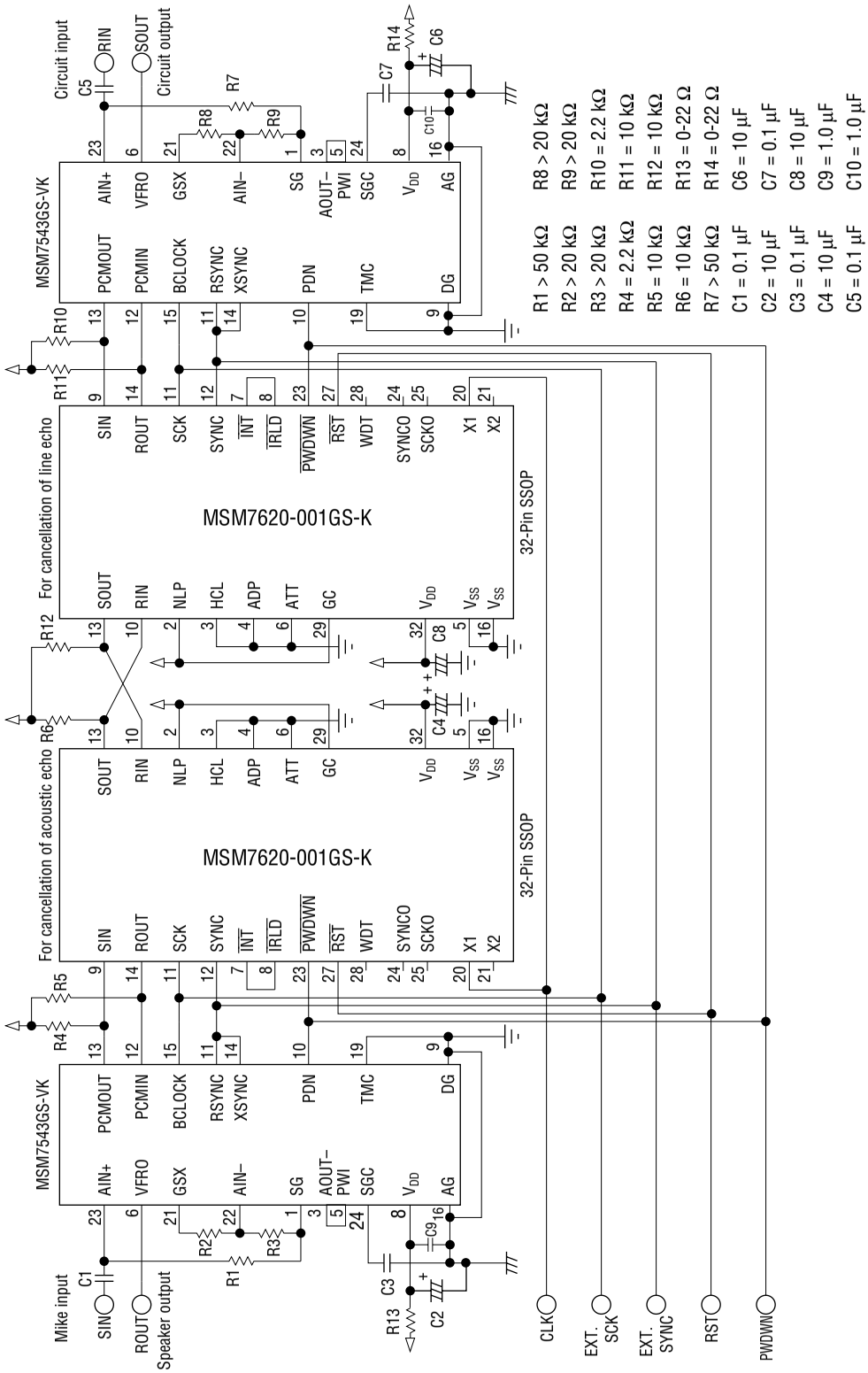
Measurement Conditions
RIN input = –10 dBm
5 kHz band white noise
(0 dBm = 2.2 dBm0)
ERL = 6 dB
ATT, GC, NLP = OFF
The second through seventh chips are connected in a cascade.

Measurement System Block Diagram

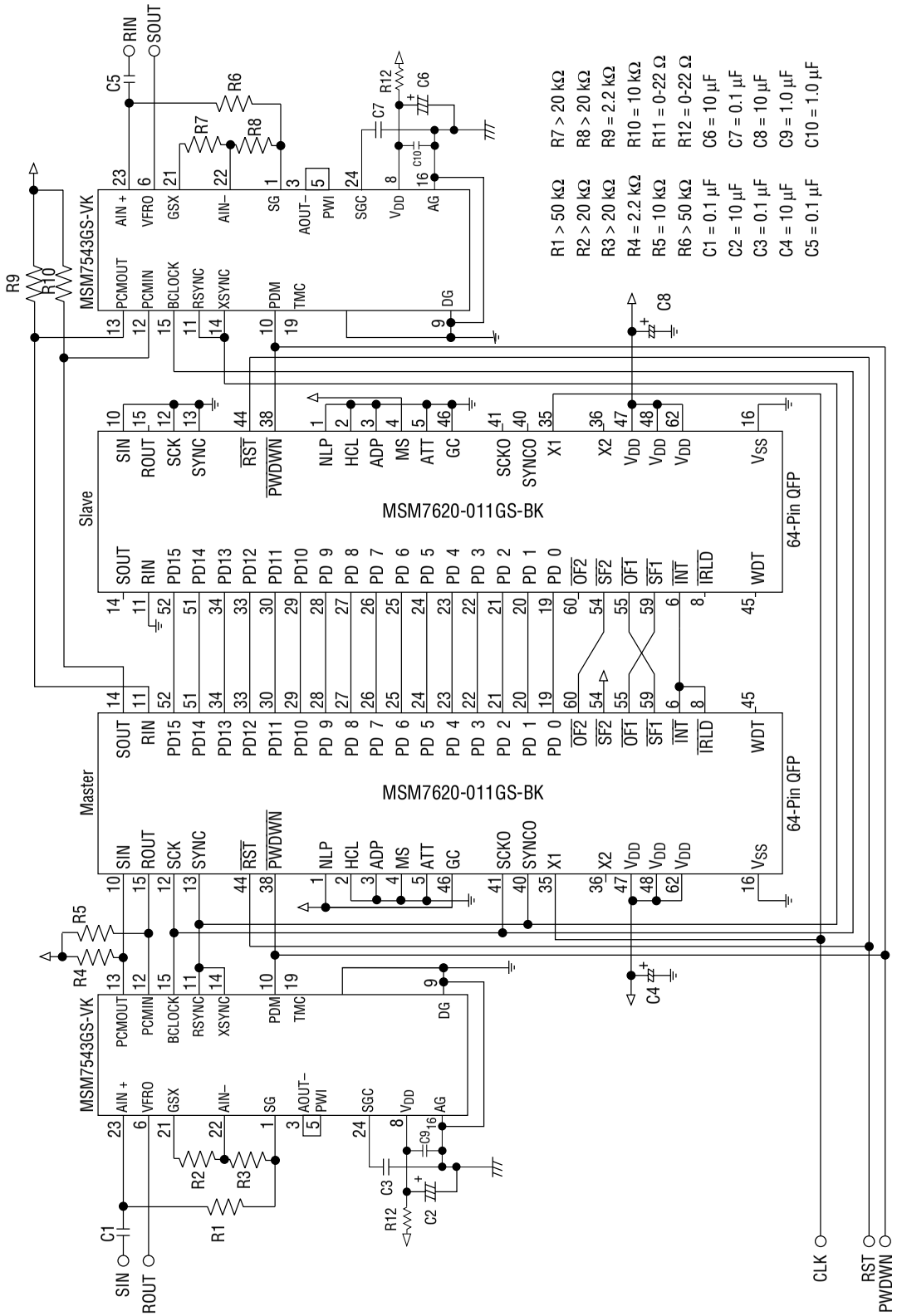


APPLICATION CIRCUIT

Bidirectional Connection Example



Cascade Connection Example



NOTES ON USE

1. Set echo return loss (ERL) to be attenuated. If the echo return loss is set to be amplified, the echo can not be eliminated.
   Refer to the characteristics diagram for ERL vs. echo attenuation quantity.

2. Set the level of the analog input so that the PCM CODEC does not overflow.

3. The recommended input level is –10 to –20 dBm0. Refer to the characteristics diagram for the RIN input level vs. echo attenuation quantity.

4. Applying the tone signal to this echo canceler will decrease echo attenuation. If the tone signal is input to the SIN pin during the time that a signal is input to the RIN pin, this echo cancceler operates faultily.
   A signal must be input to either the RIN pin or the SIN pin. The ADP or HCL pin must be driven at "H" if the tone signal is input to the SIN pin during the time that a signal is input to the RIN pin.

5. For changes in the echo path (retransmit, circuit switching during transmission, and so on), convergence may be difficult.
   Perform a reset to make it converge.
   If the state of the echo path changes after a reset, convergence may again be difficult.
   In cases such as a change in the echo path, perform a reset when possible.

6. When turning the power ON, set the $\overline{\text{PWDWN}}$ pin to "1" and input the basic clock simultaneouly with power ON.
   If powering down immediately after power ON, be sure first input 10 or more clocks of the basic clock.

7. After powering ON, be sure to reset.

8. After the power down pin is changed to a "1" from a "0", be sure to reset.

9. If this canceler is used to cancel acoustic echoes, an echo attenuation may be less than 30 dB.

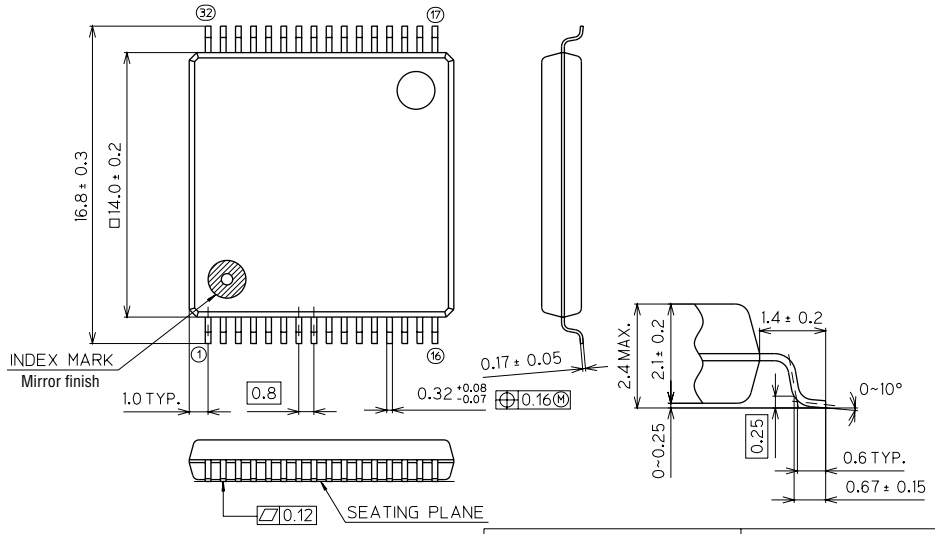
EXPLANATION OF TERMS

Attenuating Function :	This function prevents howling and controls the noise level with an attenuator for the RIN input and SOUT output. Refer to the explanation of pins (ATT pin).
Echo Attenuation :	If there is talking (input only to RIN) in the path of a rising echo arises, the echo attenuation refers to the difference in the echo return loss (canceled amount) when the echo canceler is not used and when it is used. Echo attenuation = (SOUT level during through mode operation) – (SOUT level during echo canceler operation) [dB]
Echo Delay Time :	This is the time from when the signal is output from ROUT until it returns to SIN as an echo or other similar device.
Acoustic Echo :	When using a hands free phone, and so on, the signal output from the speaker echoes and is input again to the microphone. The return signal is referred to as acoustic echo.
Telephone Line Echo :	This is a signal which is delayed midway in a telephone line and returns as an echo, due to reasons such as a hybrid impedance mismatch.
Gain Control Function :	This function prevents howling and controls the sound level by with a gain controller for the RIN input. Refer to the explanation of pins (GC pin).
Center Clipping Function :	This function forces the SOUT output to a minimum value when the signal is below –54 dBm0. Refer to the explanation of pins (NLP pin).
Double Talk Detection :	Double talk refers to a state in which the SIN and RIN signals are input simultaneously. In a double talk state, a signal outside the echo signal which is to be canceled can be input to the SIN input, resulting in misoperation. The double talk detector prevents such misoperations of the canceler.
Howling Detection :	This is the oscillating state caused by the acoustic coupling between the loud speaker and the microphone during hands free talking. Howling not only interferes with talking, but can also cause misoperation of the echo canceler. The howling detector prevents such misoperation and prevents howling.
Echo Return Loss (ERL) :	When the signal output from ROUT returns to SIN as an echo, ERL refers to how much loss there is in the signal level during ROUT. ERL = (ROUT level) – (SIN level of the ROUT signal which returns as an echo) [dB] If ERL is positive (ROUT > SIN), the system is an attenuator system. If ERL is negative (ROUT < SIN), the system is an amplifier system.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP32-P-640-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.83 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

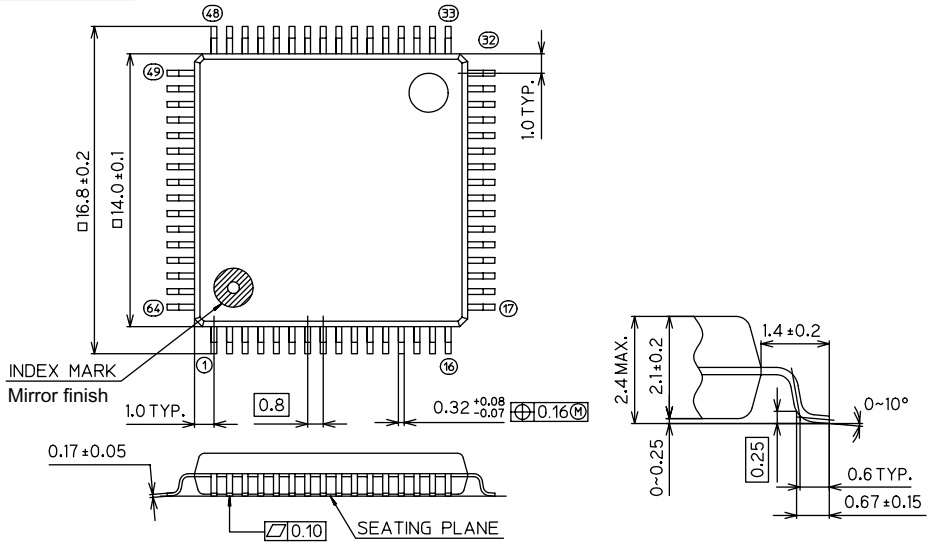
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

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Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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