OKI Semiconductor

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MSM7586-01/03

π/4 Shift QPSK MODEM/ADPCM CODEC

GENERAL DESCRIPTION

The MSM7586 is a CMOS IC developed for use with digital cordless telephones. The device provides a π/4 shift QPSK modem function and a CODEC function which performs transcoding between the voice band analog signal and 32 kbps ADPCM data.
The MSM7586 performs DTMF tone and several types of tone generation, transmit/receive data, mute and gain control, side-tone pass and its gain control, and VOX function.

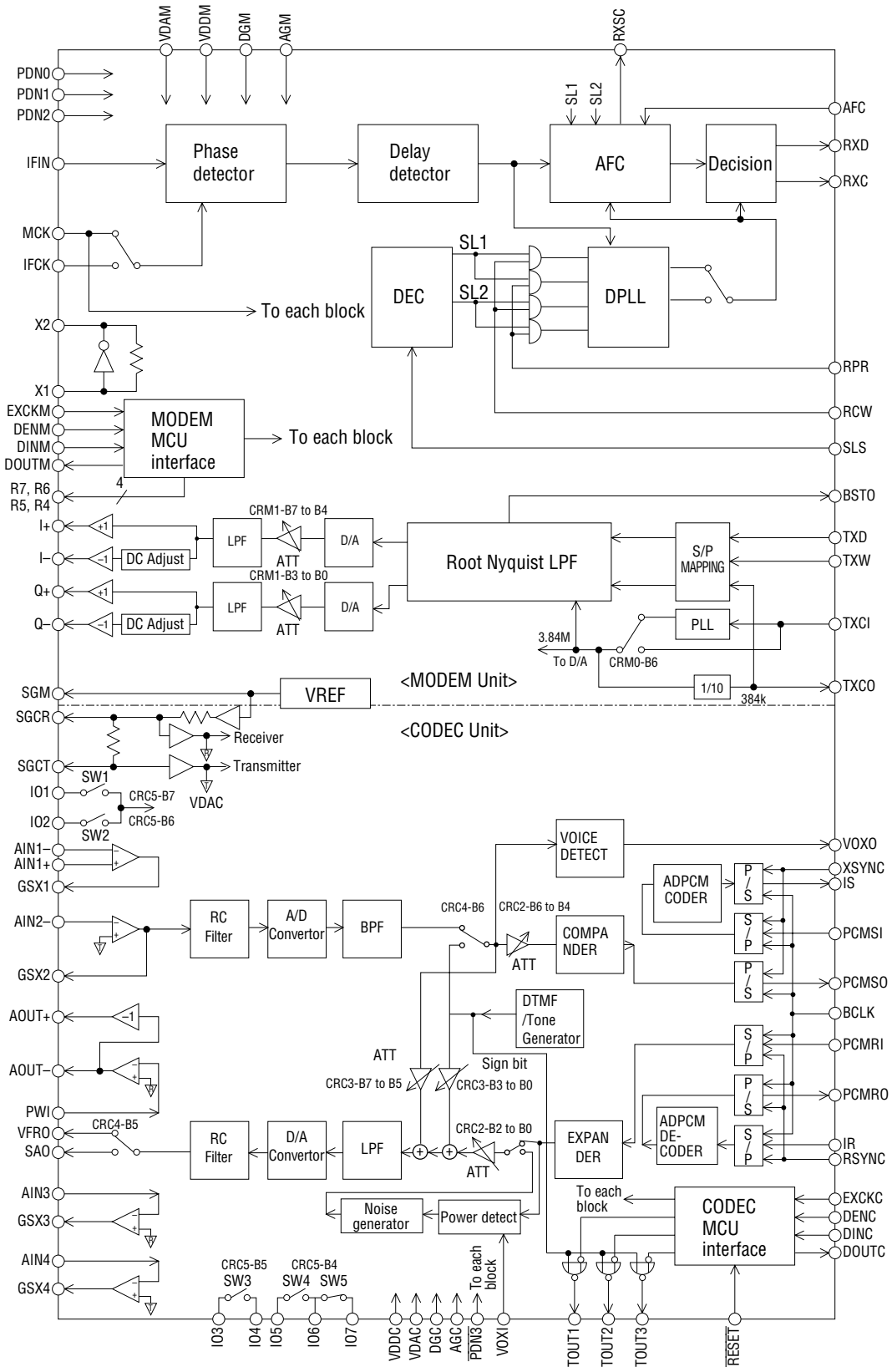
FEATURES

(π/4 Shift QPSK Modem Unit)
- 384 kbps transmission speed
- Built-in root Nyquist digital filter for the baseband band limiter
- Built-in D/A converters for the analog outputs of the quadrature signal component I and Q
- The DC offset and gain can be adjusted with respect to the differential I and Q analog outputs
- Completely digitized π/4 shift QPSK demodulator system

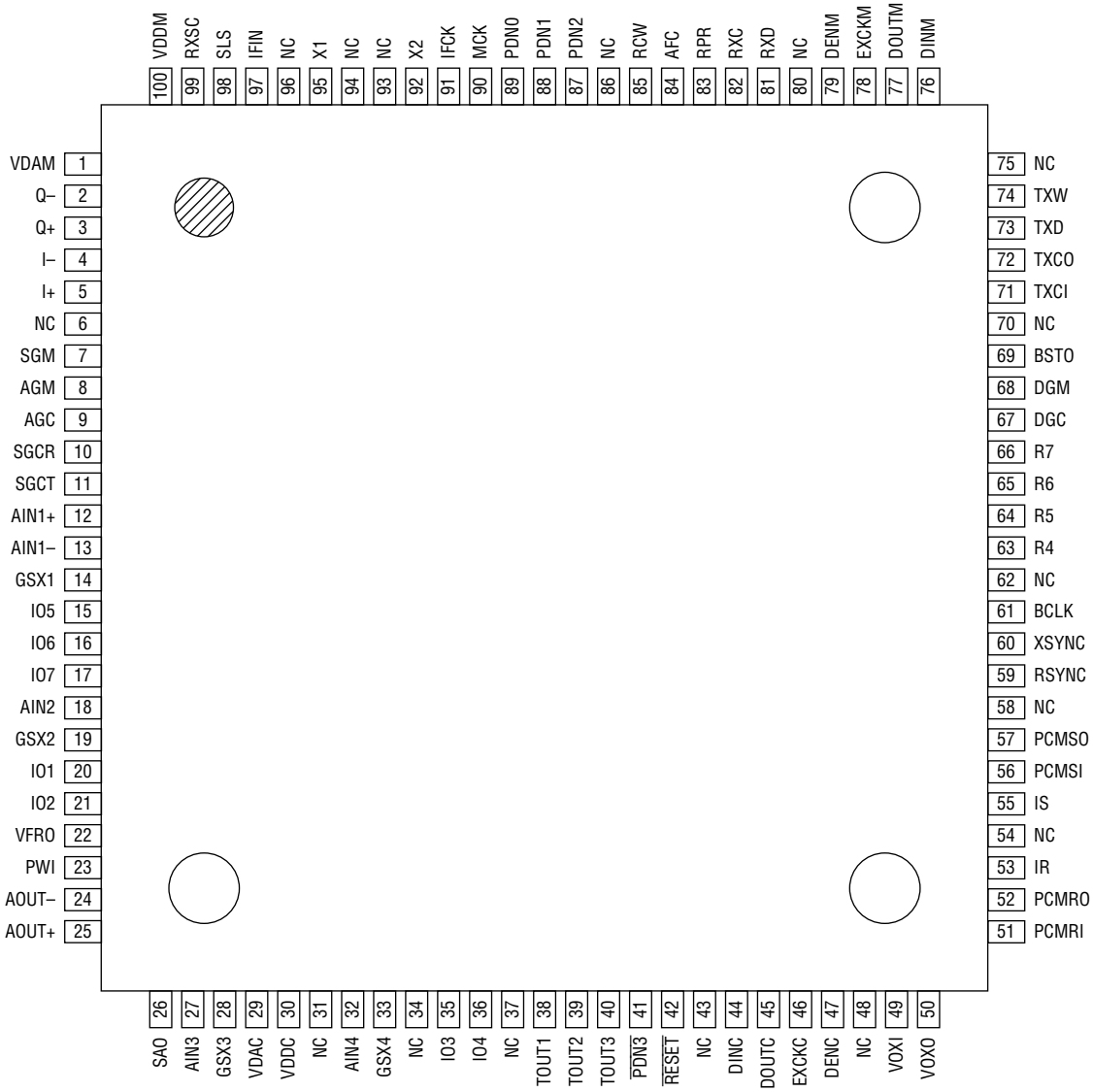
(ADPCM CODEC Unit)
- ADPCM system: built-in ITU-T Recommendations G.726 (32kbps, 24 kbps, 16 kbps)
- Transmit/receive full-duplex capability
- PCM interface code format: selectable between μ-law and A-law
- Serial ADPCM and PCM transmission rate: 64 kbps to 2,048 kbps
- Transmit/receive mute function; transmit/receive programmable gain setting
- Side tone generator (8-step level adjustment)
- Built-in DTMF tone, ringing tone, and various ringing tone generators
- Built-in VOX function

(Common Unit)
- Operate with a single 3 V power supply (V_{DD}: 2.7 V to 3.6 V)
- Low power consumption
  When entire system is operating: 20 mA Typ.
  When powered down: 0.02 mA Typ.
- Package:
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product name: MSM7586-01TS-K)
  (Product name: MSM7586-03TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

100-Pin Plastic TQFP

PIN AND FUNCTIONAL DESCRIPTIONS

(**Modem Unit**)

TXD

Transmit data input for 384 kbps.

TXCI

Transmit clock input.
When the control register CRM0 - B6 is "0", a 384 kHz clock pulse synchronous with TXD should be input to this pin. This clock pulse should be continuous because this device use APLL to generate an internal clock pulse.
When CRM0 - B6 is "1", a 3.84 MHz clock pulse should be input to this pin. When the 3.84 MHz clock pulse is applied to TXCL, TXCO outputs a 384 kHz clock pulse, which is generated by dividing the TXCL input by 10. The transmit data, synchronous to the 384 kHz clock pulse, should be input to the TXD. In this case the devices do not use APLL, and the 3.84 MHz clock pulse need not be continuous. (Refer to Fig. 1.)

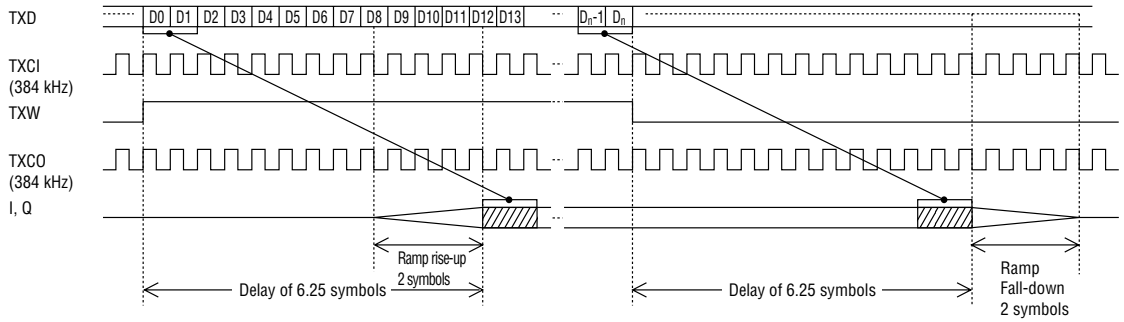
TXCO

Transmit clock output.
When CRM0 - B6 is "0", TXCO outputs the 384 kHz clock pulse (APLL output) for monitoring purposes. When CRM0 - B6 is "1", this pin outputs a 384 kHz clock pulse generated by dividing the TXCI input by 10. (Refer to Fig. 1.)

TXW

Transmit data window signal input.
The transmit timing signal for the burst data is input to this pin. If TXW is "1", the modulation data is output. (Refer to Fig. 1)

(1) CRM0 – B6 = "0"



(2) CRM0 – B6 = "1"

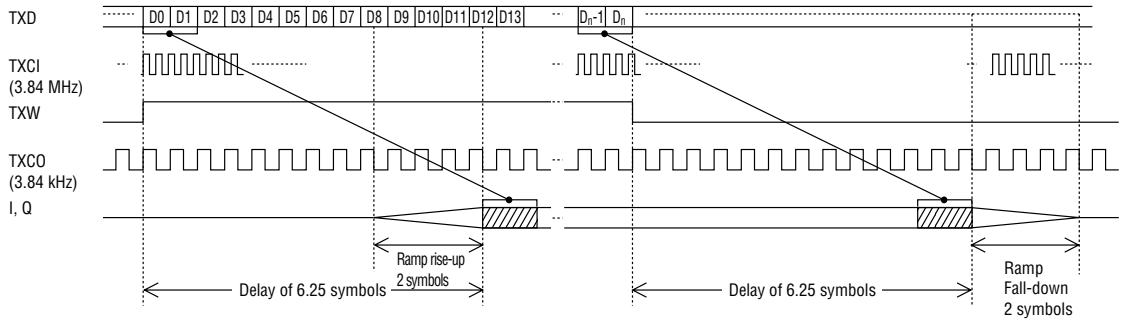


Figure 1 Transmit Timing Diagram

BSTO

BSTO is the modulator side burst window output.
The burst position of the I and Q baseband modulator output is output.

I+, I–

Quadrature modulation signal I Component differential analog output.
Their output levels are 500 mV_{pp} (when TXD = "0": 360 mV_{pp} typ.) with 1.6 Vdc as the center value. The output pin load conditions are: R ≥ 10 kΩ, C ≤ 20 pF. The gain of these pins can be adjusted using the control register CRM1 - B7 to B4, and the offset voltage at the I– pin can be adjusted using CRM3 - B7 to B3.

Q+, Q–

Quadrature modulation signal Q component differential analog outputs.
Their output levels are 500 mV_{pp} (when TXD = "0": 360 mV_{pp} typ.) with 1.6 Vdc as the center value. The output pin load conditions are: R ≥ 10 kΩ, C ≤ 20 pF. The gain of these pins can be adjusted using the control register CRM1 - B3 to B0, and the offset voltage at the Q– pin can be adjusted by using CRM4 - B7 to B3.

SGM

Internal reference voltage output.
The output voltage value is approximately 2.0 V. Insert a bypass capacitor between this pin and the AGM pin. During power down, this output is at 0 V.
The external SG voltage if necessary should be used via a buffer.

PDN0, PDN1, PDN2

Various power down control.
PDN0 controls the standby mode/communication mode; PDN1 controls the modulator unit; and PDN2 controls the demodulator unit. Refer to Table 1 for details.
The control register reset input width should be 200ns or more.
Be sure to reset all the control registers by keeping Mode A as well as by keeping $\overline{\text{RESET}}$ pin to digital "0" level for 200ns or longer after the power is turned on and the V_{DD} exceeds 2.7V.

Table 1: Description of Modem Power Down Control

	PDN0	PDN2	PDN1	Operation State	Mode Name
Standby Mode	0	0/1	1	Entire system is powered down. The control register is reset.	Mode A
	0	0	0	Entire system is powered down. The control register is not reset.	Mode B
	0	1	0	Modulator unit is powered off. (VREF and PLL also powered off.) Demodulator unit is powered on.	Mode C
Communication Mode	1	0	0	Modulator unit is powered off. (VREF and PLL are powered on.) I and Q outputs are in a high impedance state. Only the demodulator clock regenerator unit is powered on.	Mode D
	1	0	1	Modulator unit is powered on. Only the demodulator clock regenerator unit is powered on.	Mode E
	1	1	0	Modulator unit is powered off. (VREF and PLL are powered off.) I and Q outputs are in a high impedance state. Demodulator unit is powered on.	Mode F
	1	1	1	Modulator unit is powered on. Demodulator unit is powered on.	Mode G

VDDM, VDAM

+3 V power supply for the modem unit.
Supplied to the digital circuits through the VDDM pin and to the analog circuits through the VDAM pin. VDDM and VDAM, and VDDC and VDAC should be connected as close as possible on the PC board.

DGM, AGM

Ground pins for the modem unit.
DGM is the ground pin of the digital system, and AGM is the ground pin of the analog system. Since DGM and AGM are isolated inside the IC, connect them as close as possible on the circuit board.

MCK

Master clock input.
The clock frequency is 19.2 MHz.

IFIN

Modulated signal input for the demodulator block.
Select the IF frequency can be selected from 1.2 MHz, 10.7 MHz, 10.75 MHz, and 10.8 MHz, based on CRM0 - B4 and B3.

IFCK

Clock frequency 19.0222 MHz input for demodulator block IF frequencies of 10.7 MHz.
If the IF frequency is 1.2 MHz or 10.8 MHz, set this pin to "0" or "1". (Refer to Fig. 2.)

X1, X2

Crystal oscillator connection pins.
When supplying a 19.0222 MHz clock to IFCK, use these pins. (Refer to Fig. 2.)

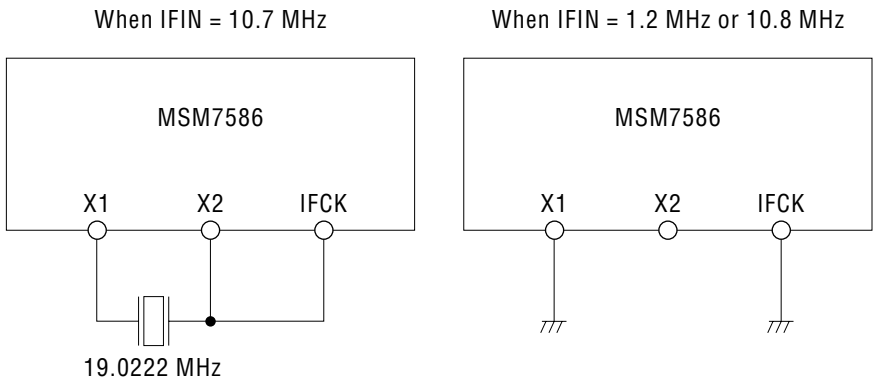


Figure 2 How to Use IFCK, X1, and X2

RXD, RXC, RXSC

Receive data and receive clock outputs.
When the modem unit is powered on, RXD, RXC and RXSC are selected based on SLS as shown in Figure 3. These outputs are used by the clock regenerator circuit.

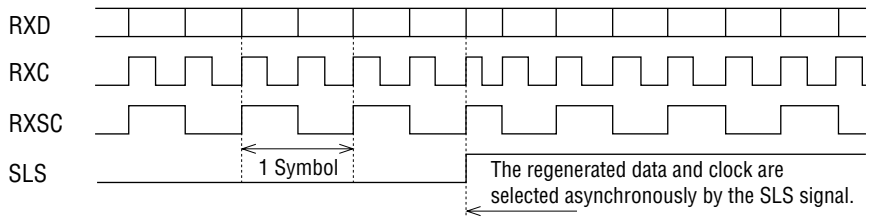


Figure 3 Timing Diagram of RXD, RXC, and RXSC

SLS

Receive side operation slot selection signal.
This device has two clock regenerator circuits and two AFC data memory registers. If SLS is "0", slot 1 is selected, if SLS is "1", slot 2 is selected.

RPR

High-speed phase clock control signal input for the clock recovery circuit.
If this pin is at "0", the circuit is always in the low-speed phase clock mode. If this pin is at "1", the clock recovery circuit enters the high-speed phase clock mode. When the phase difference is less than a defined value, the circuit shifts to the low-speed phase clock mode automatically.

AFC

AFC operation range specification signal input.
As shown in Fig. 4, the AFC information is reset when both AFC and RPR are set to "1". AFC operation starts after a fixed number of clock cycles and the AFC information is reset. If RPR is set to "1", an average number of times that AFC turns on is low. If RPR is "0", AFC is high. If AFC is "0", frequency error is not calculated, but the frequency is corrected using an error that is held.

RCW

Clock recovery circuit operation ON/OFF control signal input.
If RCW this pin is "0", DPLL does not make any phase corrections.

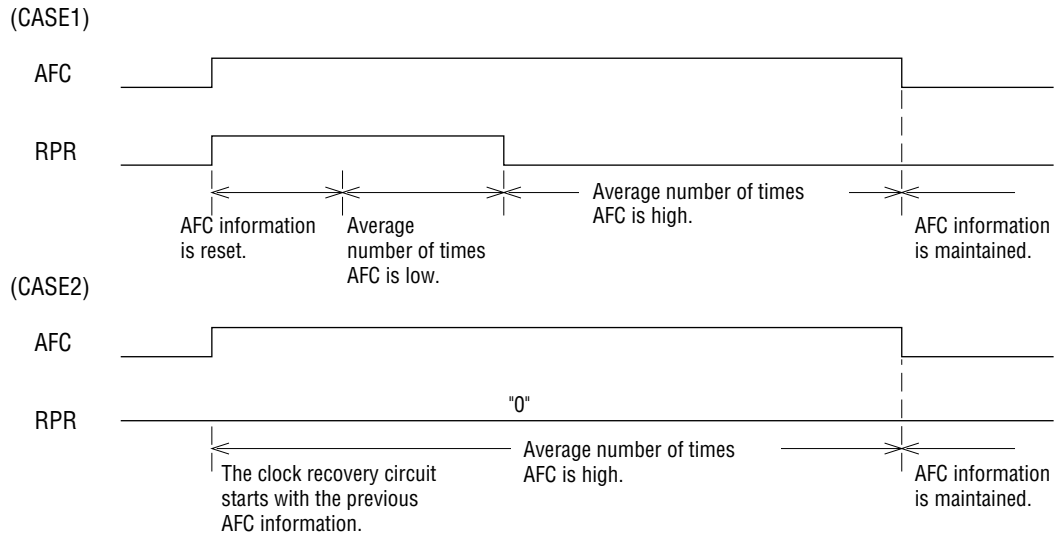


Figure 4 AFC Control Timing Diagram

DENM , EXCKM, DINM, DOUTM

Serial control ports for the microprocessor interface.
The device contains a 6-byte control register (CRM0 - 5). An external CPU uses these pins to read data from and write data to the control register. DENM is the "Enable" signal input pin. EXCKM is a data shift clock pulse input pin. DINM is an address and data input pin. DOUTM is a data output pin. Figure 5 shows input/output timing diagram.

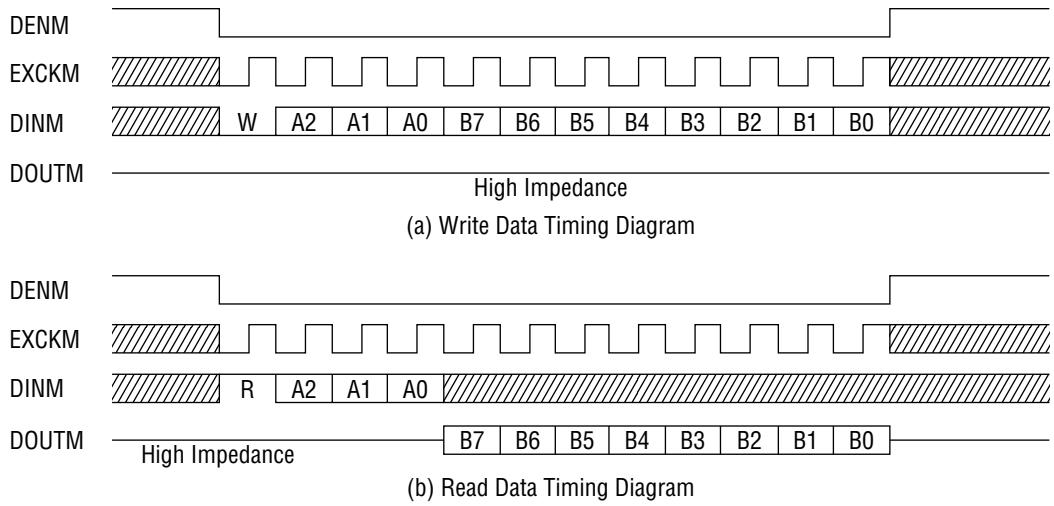


Figure 5 Modem Unit MCU Interface I/O Timing

The register map is shown below.

Table 2: Modem Unit Control Register (CRM0 to 5) Map

Register	Address			Data Description								R/W
Name	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CRM0	0	0	0	—	TXC SEL	MOD OFF	IFSEL1	IFSEL0	—	TEST1	TEST0	R/W
CRM1	0	0	1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0	R/W
CRM2	0	1	0	R7	R6	R5	R4	—	—	—	—	R/W
CRM3	0	1	1	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—	R/W
CRM4	1	0	0	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—	R/W
CRM5	1	0	1	ICT5	ICT4	ICT3	ICT2	LOCAL INV1	LOCAL INV0	ICT1	ICT0	R/W

R/W: Read/Write enable R: Read-only register

R7, R6, R5, R4

These are the control register data output pins.
These output the data CRM2 - B7, B6, B5, and B4, respectively.

(CODEC Unit)

AIN1+, AIN1-, AIN2, GSX1, GSX2

The transmit analog input and the output for transmit gain adjustment.
The pin AIN1–(AIN2) connects to the inverting input of the internal transmit amplifier, and the pin AIN1+ connects to the non-inverting input of the internal transmit amplifier. The pin GSX1 (GSX2) connects to output of the internal transmit amplifier. See Fig. 6 for gain adjustment.

VFRO, AOUT+, AOUT-, PWI

Used for the receive analog output and the output for receive gain adjustment.
VFRO is an output of the receive filter. AOUT+ and AOUT– are differential analog signal outputs which can directly drive Z_L = 350 Ω+120 nF or the 1.2 kΩ load. See Fig. 6 for gain adjustment. However, these outputs are in high impedance state during power down.

SAO, AIN3, AIN4, GSX3, GSX4

Input pins for the internal operational amp.
Refer to Fig. 6 for connection information. However, these output pins are in the high impedance state during power down.

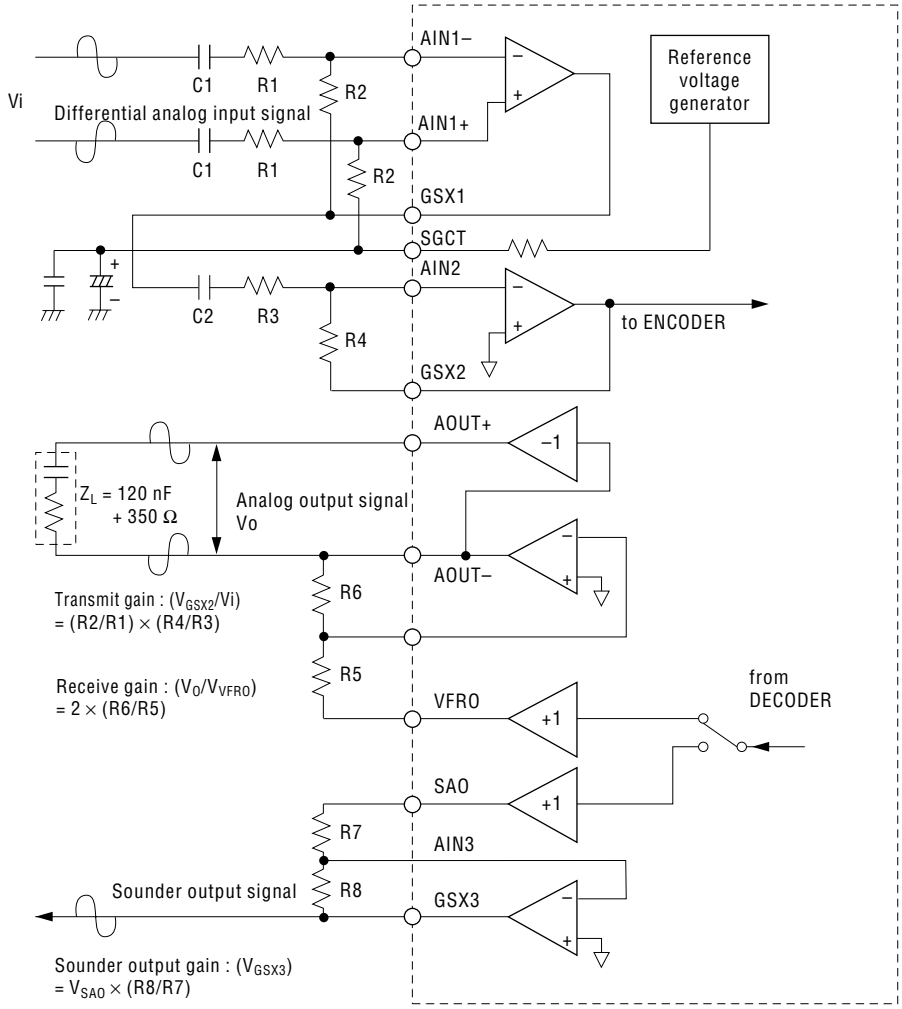


Figure 6 CODEC Unit Analog Interface

IO1 to IO7

I/O pins of the internal analog switch.
Refer to the control register description table (CRC5) and the block diagram for connection information and control methods.

TOUT1 to TOUT3

Sign bit output pins of the tone generator.
Output control of each pin is performed by the control register. Refer to the control register description table (CRC5) and the block diagram for connection information and control methods.

SGCT, SGCR

Output pins of the CODEC unit analog signal ground voltage.
SGCT outputs the analog signal ground voltage of the transmit system, and SGCR outputs the same for the receive system. The output voltage value is approximately 1.4 V. Connect 10 µF and 0.1 µF bypass capacitors (ceramic type) between these pins and the AGC pin. During power down, the output changes to 0 V. The external SG voltage if necessary should be used via a buffer.

VDDC, VDAC

CODEC unit +3 V power supply.
VDDC is supplied to the digital system power supply, and VDAC is supplied to the analog system power supply. VDDC and VDAC, and VDDM and VDAM must be connected as possible on the PC board.

DGC, AGC

CODEC unit ground.
DGC is the digital system ground pin, and AGC is the analog system ground pin. Since DGC and AGC are unconnected in the device, place them as close together as possible on the circuit board.

$\overline{\text{PDN3}}$

CODEC unit power-down control input.
The CODEC unit changes to the power - down state when set to a digital "0." Since the power-down control is handled by an OR with control register CRC0 - B5, set CRC0 - B5 to digital "0" when using this pin.

$\overline{\text{RESET}}$

Reset control input pin of the CODEC unit control register.
When set to digital "0," each bit of the control register is reset. During normal operation, set this pin to digital "1." A more than 200ns reset signal should be input.
Be sure to initialize all the control registers by executing this reset to keep this pin to digital "0" level as well as by keeping Mode A for 200ns or longer after the power is turned on and the V_{DD} exceeds 2.7V.

PCMSO

Transmit PCM data output.
This PCM output signal is output from MSB synchronous with the rising edge of BCLK and XSYNC.

PCMSI

Transmit PCM data input.
This signal is converted to the ADPCM data. The PCM signal is shifted on the falling edge of BCLK. Normally, this pin is connected to PCMSO.

PCMRO

Receive PCM data output.
The PCM signal is the output signal after ADPCM decoder processing. This signal is serially output from the MSB synchronous with the rising edge of BCLK and RSYNC.

PCMRI

Receive PCM data input.
The PCM input signal is shifted on the falling edge of BCLK and input from MSB. Normally, this pin is connected to PCMRO.

IS

Transmit ADPCM signal output.
This signal is the output signal after ADPCM encoding, and is serially output from MSB synchronous with the rising edge of BCLK and XSYNC. This pin is an open drain output which remains in a high impedence state during power-down, and requires a pull-up resistor.

IR

Receive ADPCM signal input.
Input data is shifted serially from MSB on the falling edge of BCLK synchronous with RSYNC.

BCLK

Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI) and the ADPCM data(IS, IR) .
The frequency ranges from 64 kHz to 2048 kHz.

XSYNC

Transmit PCM and ADPCM data 8 kHz synchronous signal input.
This signal should be synchronous with BCLK. XSYNC is used for indicating MSB of the transmit serial PCM and ADPCM data stream.

RSYNC

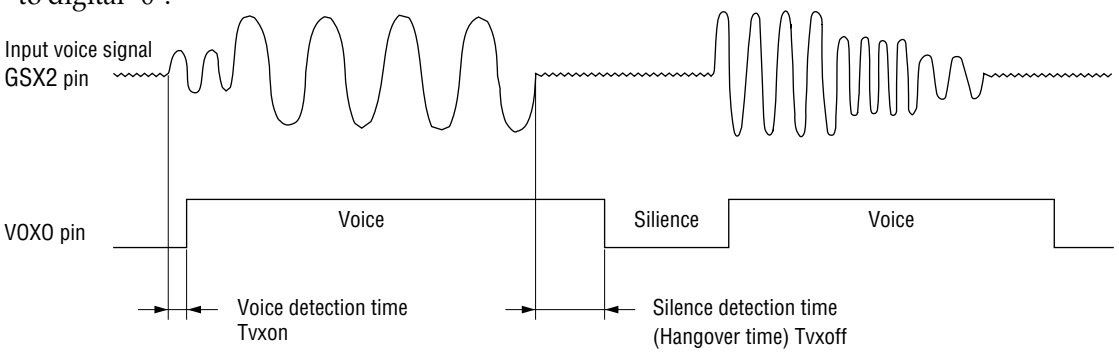
Receive PCM and ADPCM data 8 kHz synchronous signal input.
This signal should be synchronous with BCLK signal. RSYNC is used for indicating MSB of the receive serial PCM and ADPCM data stream.

VOXO

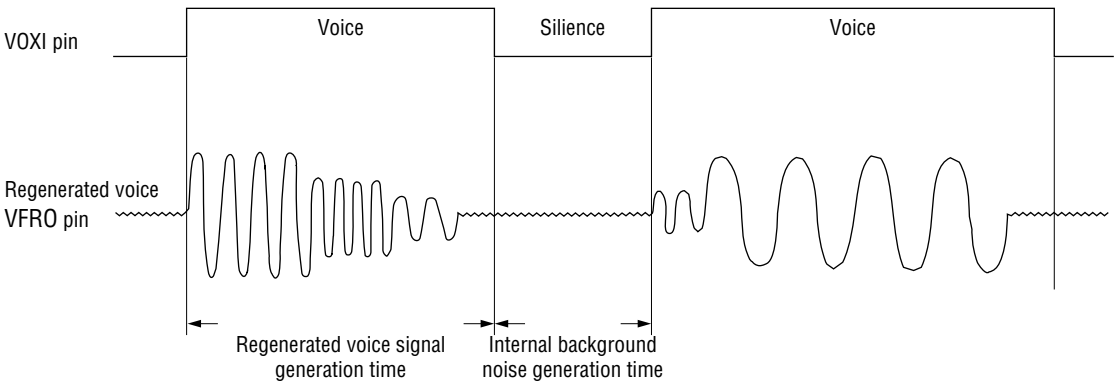
Transmit VOX function signal output.
VOX function is used to recognize the presence or absence of the transmit voice signal by detecting the signal energy. "H" and "L" levels on this pin correspond to the presence and the absence, respectively. This result also appears at the register data CRC7 - B7. The signal energy detect threshold is set by the control register data CRC6 - B6, B5.

VOXI

Signal input for receive VOX function.
The "H" level on VOXI indicates the presence of voice signal, the decoder block processes normal receive signal, and the voice signal appears at analog output pins . The "L" level indicates the absence of voice signal, the background noise generated in this device is transferred to the analog output pins. The background noise amplitude is set by the control register CRC6. Because this signal is ORed with the register data CRC6 - B3, the control register data CRC6 - B3 should be set to digital "0".



(a) Transmission Side VOX Function Timing Diagram



(b) Receive Side VOX Function Timing Diagram

Note: The VOXO and VOXI pin function are enabled when CRC6 - B7 is set to "1".

Figure 7 VOX Function

DENC, EXCKC, DINC, DOUTC

Serial control ports for MCU interface.
Reading and writing data are performed by an external MCU through these pins. The 8-byte control registers (CRC0 - 7) are provided for the CODEC unit in this device. DENC is the "Enable" control signal input, EXCKC is the data shift clock input, DINC is the address and data input, and DOUTC is the data output. Figure 8 shows input/output timing diagram.

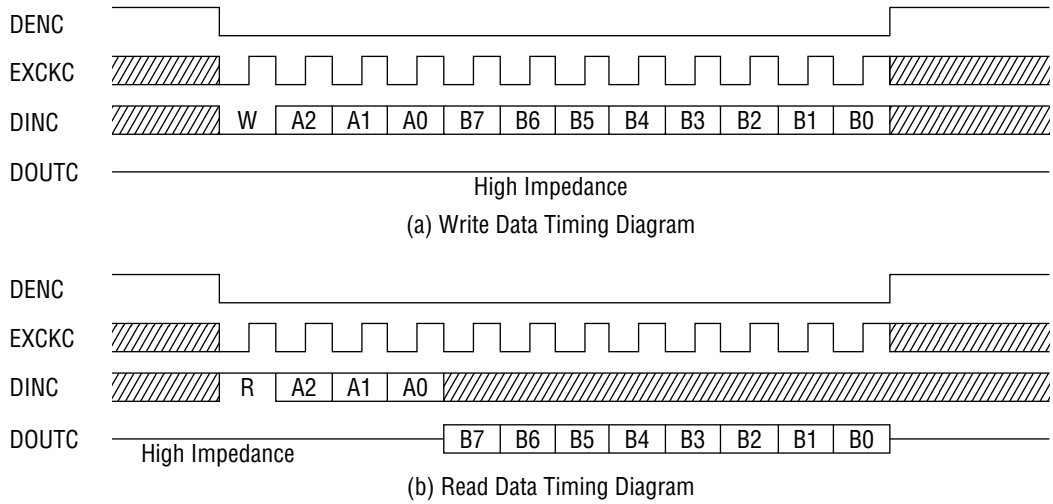


Figure 8 CODEC Unit MCU Interface I/O Timing

The register map is shown below.

Table 3: CODEC Unit Control Register (CRC0 to 7) Map

Register	Address			Data Description								R/W
Name	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CRC0	0	0	0	A/μ SEL	—	PDN ALL	—	—	—	—	PDN SAO/AOUT	R/W
CRC1	0	0	1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD	R/W
CRC2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CRC3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0	R/W
CRC4	1	0	0	DTMF/ OTHERS SEL	TONE SEND	SAO/ VFRO	TONE4	TONE3	TONE2	TONE1	TONE0	R/W
CRC5	1	0	1	SW1 CONT	SW2 CONT	SW3 CONT	SW4/5 CONT	—	TOUT3 CONT	TOUT2 CONT	TOUT1 CONT	R/W
CRC6	1	1	0	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0	R/W
CRC7	1	1	1	VOX OUT	TX NOISE LVL1	TX NOISE LVL0	—	—	—	—	—	R

R/W: Read/Write enable R: Read-only register

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +5	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

	Parameter	Symbol	Conditon		Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}	Voltage must be fixed		2.7	—	3.6	V
Operating Temperature		Ta	—		–25	+25	+70	°C
Input High Voltage		V_{IH}	Input pins fully digital		0.45 × V_{DD}	—	V_{DD}	V
Input Low Voltage		V_{IL}	Input pins fully digital		0	—	0.16 × V_{DD}	V
Digital Input Rise Time		t_{Ir}	Input pins fully digital		—	—	50	ns
Digital Input Fall Time		t_{If}	Input pins fully digital		—	—	50	ns
Digital Output Load		R_{DL}	IS (Pull-up resistance)		500	—	—	Ω
		C_{DL}	Input pins fully digital		—	—	100	pF
Bypass Capacitor for SG		C_{SG}	Between SGM and AGM, and between SGCT/R and AGC		10 + 0.1	—	—	µF
Master Clock Frequency		F_{MCK}	MCK		–0.01%	19.2	+0.01%	MHz
Master Clock Duty Ratio		D_{MCK}	MCK		40	50	60	%
Modem Unit	Modulator Side Input Frequency	F_{TXC1}	TXCI (When CRM0 - B6 = "0")		—	384	—	kHz
		F_{TXC2}	TXCI (When CRM0 - B6 = "1")		—	3.84	—	MHz
	Demodulator Side Input Frequency	F_{IFCK1}	IFCK (When IFIN = 10.7 MHz)		—	19.0222	—	MHz
		F_{IFCK2}	IFCK (When IFIN = 10.75 MHz)		—	19.1111	—	MHz
	Clock Duty Ratio	D_{CKM}	IFCK, TXCI, EXCKM		40	50	60	%
	IF Input Duty Ratio	D_{CIF}	IFIN		45	50	55	%
	Transmit Sync Pulse Setting Time	t_{XSM}, t_{SXM}	TXCI↔TXW	Fig.9	200	—	—	ns
		t_{SDM}, t_{DHM}	TXCI↔TXD		200	—	—	ns
CODEC Unit	Bit Clock Frequency	F_{BCK}	BCLK		64	—	2048	kHz
	Synchronous Signal Frequency	F_{SYNC}	XSYNC, RSYNC		—	8.0	—	kHz
	Clock Duty Ratio	D_{CKC}	BCLK, EXCKC		40	50	60	%
	Transmit Sync Pulse Setting Time	t_{XSC}, t_{SXC}	BCLK↔XSYNC	Fig.12	100	—	—	ns
	Receive Sync Pulse Setting Time	t_{RSC}, t_{SRC}	BCLK↔RSYNC		100	—	—	ns
	Synchronous Signal Width	t_{WSC}	XSYNC, RSYNC		1 BCLK	—	100	µs
	PCM, ADPCM Set-up Time	t_{DSC}	—		100	—	—	ns
	PCM, ADPCM Hold Time	t_{DHC}	—		100	—	—	ns

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current (Modem Unit) * When CODEC Unit is in a Power Down State	I_{DD1}	Mode A, Mode B (When V_{DD} = 3.0 V)	—	0.02	0.1	mA
	I_{DD2}	Mode C (When V_{DD} = 3.0 V)	—	5.5	11.0	mA
	I_{DD3}	Mode D (When V_{DD} = 3.0 V)	—	5.5	11.0	mA
	I_{DD4}	Mode E (When V_{DD} = 3.0 V)	—	11.5	23.0	mA
	I_{DD5}	Mode F (When V_{DD} = 3.0 V)	—	9.5	19.0	mA
	I_{DD6}	Mode G (When V_{DD} = 3.0 V)	—	14.0	28.0	mA
Power Supply Current (CODEC Unit) * When Modem Unit is in a Power Down State	I_{DD7}	When operating * (When no signal, and V_{DD} = 3.0 V)	—	8.0	16.0	mA
	I_{DD8}		—	12.0	19.0	mA
	I_{DD9}	When powered down (When V_{DD} = 3.0 V)	—	0.02	0.1	mA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	0.5 × V_{DD}	—	V_{DD}	V
		I_{OH} = 1 µA	0.8 × V_{DD}	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.2 mA (IS pin is 500 Ω pull-up)	0	0.2	0.4	V
Output Leakage Current	I_O	IS pin	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

* I_{DD7} applies when CRC0 - B0 = "0" and CRC4 - B5 = "0"; I_{DD8} applies when operating at other times.

Analog Interface Characteristics (Modem Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Resistance Load	R_{LIQ}	I+, I–, Q+, Q–	10	—	—	kΩ
Output Capacitance Load	C_{LIQ}	I+, I–, Q+, Q–	—	—	20	pF
Output DC Voltage Level	V_{DCM}	I+, I–, Q+, Q– (TXW = 0)	1.55	1.6	1.65	V
Output AC Voltage Level	V_{ACM}	I+, I–, Q+, Q– (For TXD = 0 continuous input)	340	360	380	mV_{PP}
Offset Voltage Difference	V_{OFF}	Difference among I+, I–, Q+ and Q–	–20	—	+20	mV
Modulator D/A Conversion Sampling Frequency	F_{SDA}	—	—	1.92	—	MHz
Modulator D/A Conversion Offset Frequency	F_{CDA}	—	—	380	—	kHz
Output DC Voltage Adjustment Level Range	D_{CVL}	—	—	±45	—	mV
Output AC Voltage Adjustment Level Range	A_{CVL}	—	—	±4	—	%
Out-of-band Spectrum	P600	600 kHz detuning (continuous)	60	—	—	dB
	P900	900 kHz detuning (continuous)	65	—	—	dB
Modulation Accuracy	E_{VM}	—	—	1.0	3.0	% rms
Demodulator Side IF Input Level	I_{FV}	IFIN input level	0.4	—	V_{DD}	V_{PP}
IFIN Input Impedance	R_{IF}	DC impedance	—	20	—	kΩ
SGM Output Voltage	V_{SGM}	—	—	2.0	—	V
SGM Output Impedance	R_{SGM}	—	—	1.5	—	kΩ
Master Clock External Input Level	I_{X11}	X1 input level (When CRM5 – B1 = "0")	1.5	—	V_{DD}	V_{PP}
	I_{X12}	X1 input level (When CRM5 – B1 = "1")	0.7	—	V_{DD}	V_{PP}
X1 Input Impedande	RX1	—	—	2.0	—	MΩ
X1 Input Capacitance	CX1	—	—	10	—	pF

Digital Interface Characteristics (Modem Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Transmit Digital I/O Setting Time	$t_{XDM1,2}$	C load = 50 pF	Fig. 9	0	—	200	ns
	$t_{XDM3,4}$			0	—	400	ns
Receive Digital I/O Setting Time	$t_{RDM1,2}$	C load = 50 pF	Fig. 10	0	—	200	ns
Serial Port Digital I/O Setting Time	t_{M1}	C load = 50 pF	Fig. 11	50	—	—	ns
	t_{M2}			50	—	—	ns
	t_{M3}			50	—	—	ns
	t_{M4}			50	—	—	ns
	t_{M5}			100	—	—	ns
	t_{M6}			50	—	—	ns
	t_{M7}			50	—	—	ns
	t_{M8}			0	—	100	ns
	t_{M9}			50	—	—	ns
	t_{M10}			50	—	—	ns
	t_{M11}			0	—	50	ns
	t_{M12}			200	—	—	ns
EXCK Clock Frequency	Feckm	EXCKM	—	—	—	10	MHz

Analog Interface Characteristics (CODEC Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INC}	AIN+, AIN–, AIN2, PWI, AIN3, AIN4	10	—	—	MΩ
Output Resistance Load	R_{LC1}	GSX1, GSX2, VFRO, SAO	20	—	—	kΩ
	R_{LC2}	AOUT+, AOUT–, GSX4	1.2	—	—	kΩ
	R_{LC3}	GSX3	150	—	—	Ω
Output Capacitance Load	C_{LC1}	GSX1, GSX2, VFRO, SAO	—	—	100	pF
	C_{LC2}	AOUT+, AOUT–, GSX4	—	—	100	pF
	C_{LC3}	GSX3	—	—	100	pF
Output Voltage Level (*1)	V_{OC1}	GSX1, GSX2, VFRO, SAO(RL = 20 kΩ)	—	—	1.3	V_{PP}
	V_{OC2}	AOUT+, AOUT–, GSX4 (RL = 1.2 kΩ)	—	—	1.3	V_{PP}
	V_{OC3}	GSX3(RL = 150 Ω)	—	—	1.3	V_{PP}
Offset Voltage	V_{OFC1}	VFRO, SAO	–100	—	+100	mV
	V_{OFC2}	GSX1, GSX2, AOUT+, AOUT–, GSX3, GSX4	–20	—	+20	mV
SGCT, SGCR Output Voltage	V_{SGC}	SGCT, SGCR	—	1.4	—	V
SGCT Output Impedance	R_{SGCT}	SGCT	—	40	80	kΩ
SGCR Output Impedance	R_{SGCR}	SGCR	—	4	8	kΩ
SGCT Rise Time	T_{SGCT}	For the Recommended Circuit (Rise time to 90% of max. level)	—	600	—	ms
SGCR Rise Time	T_{SGCR}	For the Recommended Circuit (Rise time to 90% of max. level)	—	15	—	ms
Analog Switch OFF Resistance	R_{SWof}	SW1 to SW5	50	—	—	MΩ
Analog Switch ON Resistance	R_{SWon}	SW1 to SW5	100	—	400	Ω

Note : *1 –7.7 dBm (600 Ω) = 0 dBm0, +3.14 dBm0 = 1.30 V_{PP} (A-law)
–7.7 dBm (600 Ω) = 0 dBm0, +3.17 dBm0 = 1.30 V_{PP} (μ-law)

Digital Interface Characteristics (CODEC Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Digital Output Delay Time PCM, ADPCM Interface	t_{SDXC}, t_{SDRC}	1 LSTTL + 100 pF pull-up : 500 Ω Items in parenthesis ( ) mean C load = 10 pF, and the pull-up ≤ 2 kΩ	Fig. 12	0	—	200 (100)	ns
	t_{XDC1}, t_{RDC1}			0	—	200 (100)	ns
	t_{XDC2}, t_{RDC2}			0	—	200 (100)	ns
	t_{XDC3}, t_{RDC3}			0	—	200 (100)	ns
Serial Port Digital I/O Timing Characteristics	t_{C1}	C load = 50 pF	Fig. 13	50	—	—	ns
	t_{C2}			50	—	—	ns
	t_{C3}			50	—	—	ns
	t_{C4}			50	—	—	ns
	t_{C5}			100	—	—	ns
	t_{C6}			50	—	—	ns
	t_{C7}			50	—	—	ns
	t_{C8}			0	—	100	ns
	t_{C9}			50	—	—	ns
	t_{C10}			50	—	—	ns
	t_{C11}			0	—	50	ns
	t_{C12}			200	—	—	ns
EXCK Clock Frequency	Feckc	EXCKC	—	—	—	10	MHz

AC Characteristics (CODEC Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	25	—	—	dB
	L_{OSS} T2	300 to 3 k		–0.15	—	+0.20	dB
	L_{OSS} T3	1020		Reference			dB
	L_{OSS} T4	3300		–0.15	—	+0.80	dB
	L_{OSS} T5	3400		0	—	0.80	dB
	L_{OSS} T6	3968.75		13	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	–0.15	—	+0.20	dB
	L_{OSS} R2	1020		Reference			dB
	L_{OSS} R3	3300		–0.15	—	+0.80	dB
	L_{OSS} R4	3400		0	—	0.80	dB
	L_{OSS} R5	3968.75		13	—	—	dB
Transmit Signal to Distortion Ratio (*2)	SD T1	1020	3	35	—	—	dB
	SD T2		0	35	—	—	dB
	SD T3		–30	35	—	—	dB
	SD T4		–40	28	—	—	dB
	SD T5		–45	23	—	—	dB
Receive Signal to Distortion Ratio (*2)	SD R1	1020	3	35	—	—	dB
	SD R2		0	35	—	—	dB
	SD R3		–30	35	—	—	dB
	SD R4		–40	28	—	—	dB
	SD R5		–45	23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	–0.2	—	+0.2	dB
	GT T2		–10	Reference			dB
	GT T3		–40	–0.2	—	+0.2	dB
	GT T4		–50	–0.5	—	+0.5	dB
	GT T5		–55	–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	–0.2	—	+0.2	dB
	GT R2		–10	Reference			dB
	GT R3		–40	–0.2	—	+0.2	dB
	GT R4		–50	–0.5	—	+0.5	dB
	GT R5		–55	–1.2	—	+1.2	dB

Note: *2 P-message filter used

AC Characteristics (CODEC Unit)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level dBm0	Other				
Idle Channel Noise (*2)	N_{IDLT}	—	AIN = SG	—	—	—	–68 (–75.7)	dBm0p (dBmp)
	N_{IDLR}	—	(*3)	—	—	—	–72 (–79.7)	
Absolute Level (*4)	A_{VT}	1020	0	GSX2	0.285	0.320	0.359	Vrms
	A_{VR}			VFRO	0.285	0.320	0.359	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise frequency: 0 kHz to 50 kHz	Noise level: 50 mVpp	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB

Notes: *2 P-message filter used
*3 PCMRI input: "11010101" (A-law), "11111111" (μ-law)
*4 0.320 Vrms = 0 dBm0 = –7.7 dBm (600 W)

ADPCM unit characteristics are fully compliant with ITU-T Recommendation G.726.

AC Characteristics (DTMF and Other Tones)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Frequency Deviation	D_{FT1}	DTMF tones		–7	—	+7	Hz
	D_{FT2}	Other various tones		–7	—	+7	Hz
Tone Reference Output Level (*5)	V_{TL}	Transmit side tone (Gain setting 0dB)	DTMF (low group)	–18	–16	–14	dBm0
	V_{TH}		DTMF (high group), other	–16	–14	–12	dBm0
	V_{RL}	Receive side tone (Tone generator gain setting –6dB)	DTMF (low group)	–10	–8	–6	dBm0
	V_{RH}		DTMF (high group), other	–8	–6	–4	dBm0
DTMF Tone Level Relative Value	R_{DTMF}	V_{TH}/V_{TL}, V_{RH}/V_{RL}		1	2	3	dB

Note: *5 Not including programmable gain set values

AC Characteristics (Gain Settings)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/Receive Gain Setting Accuracy	D_G	For all gain set values	–1	0	+1	dB

AC Characteristics (VOX Function)

(V_{DD} = 2.7 V to 3.6 V, Ta = –25°C to +70°C)

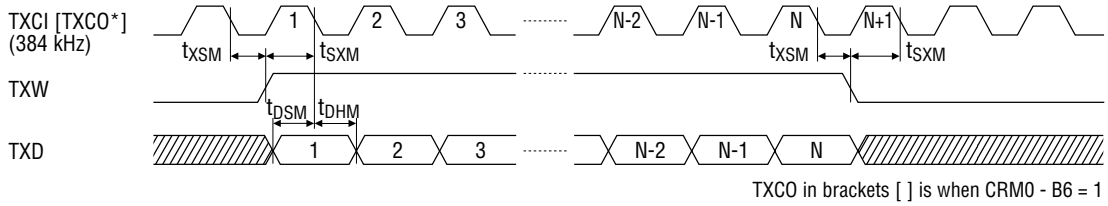
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit VOX Detection Time (Voice and Silence Test Time)	T_{VXON}	Silence→voice	VOXO pin: See Fig. 7	—	10*6	—	ms
	T_{VXOF}	Voice→silence	Voice/silence differential: 10 dB	140/300	160/320	180/340	ms
Transmit VOX Detection Level Accuracy (Voice Detection Level)	D_{VX}	For detection level set values by CRM6 - B6, B5		–2.5	0	+2.5	dB

Note: *6 When single tone is input at 1000Hz

TIMING DIAGRAM

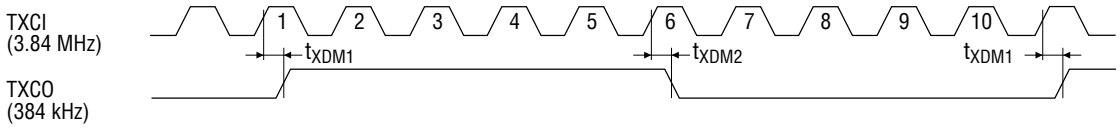
(Modem Unit)

Transmit Data Input Timing



TXCO in brackets [ ] is when CRM0 - B6 = 1

Transmit Clock (TXCO) Timing (When CRM0 - B6 = 1)



Transmit Burst Position (BSTO) Output Timing (When CRM0 - B6 = 0)

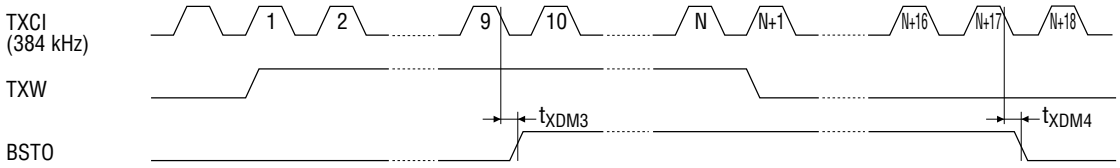


Figure 9 Modem Unit Transmit Side (Modulator Side) Digital I/O Timing

Receive Side Data I/O Timing

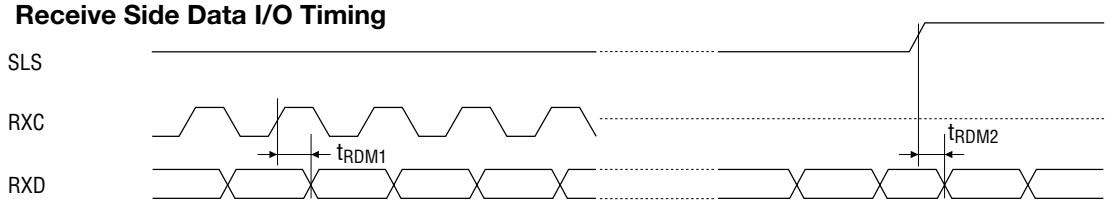


Figure 10 Modem Unit Receive Side (Demodulator Side) Digital I/O Timing

Serial Port Timing for Microcontroller Interface

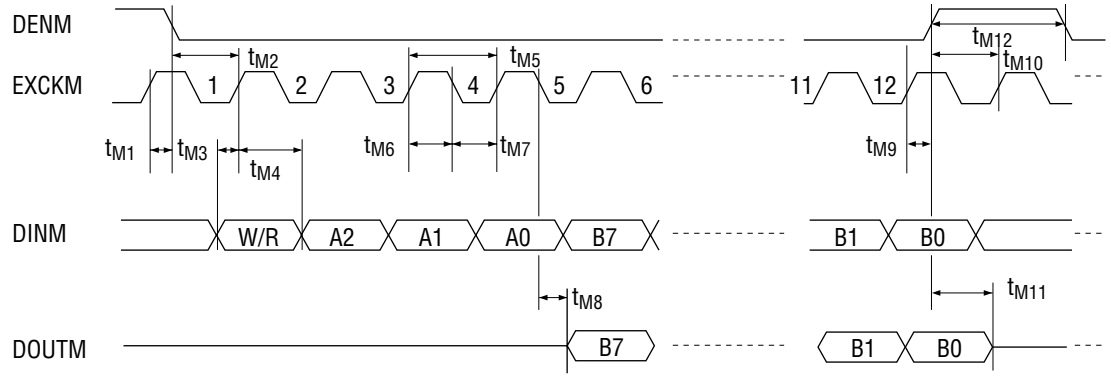
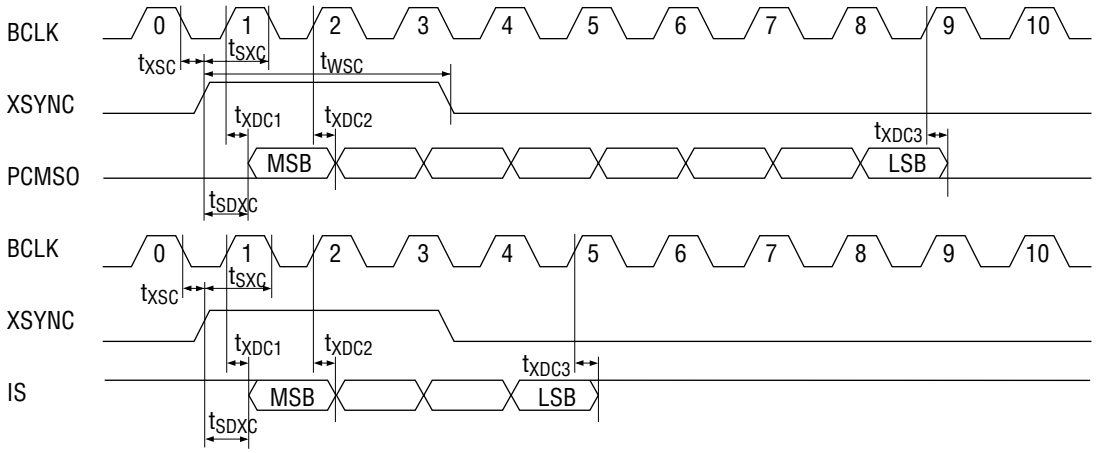


Figure 11 Modem Unit Serial Control Port Interface

(CODEC Unit)

Transmit Side PCM, ADPCM Timing



Receive Side PCM, ADPCM Timing

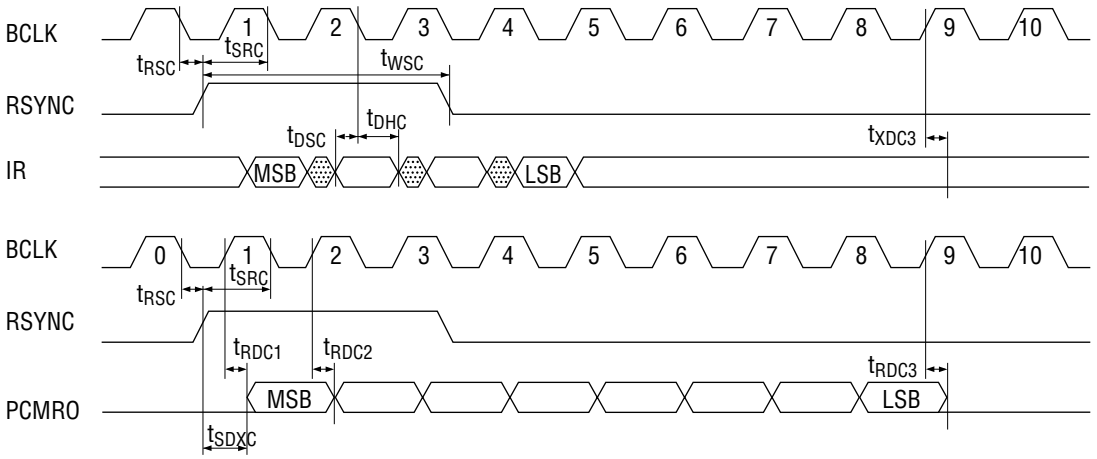


Figure 12 CODEC Unit PCM, ADPCM Interface

Serial Port Timing for Microcontroller Interface

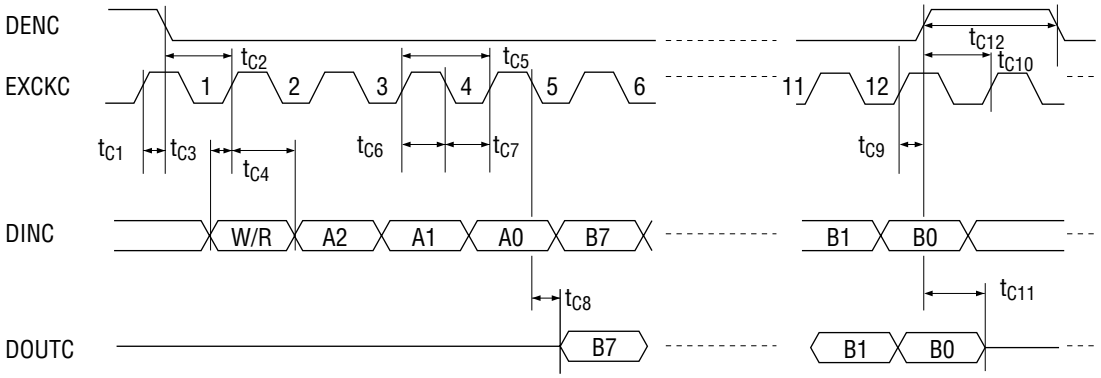


Figure 13 CODEC Unit Serial Control Port Interface

Modem Unit Mode State Transition Time

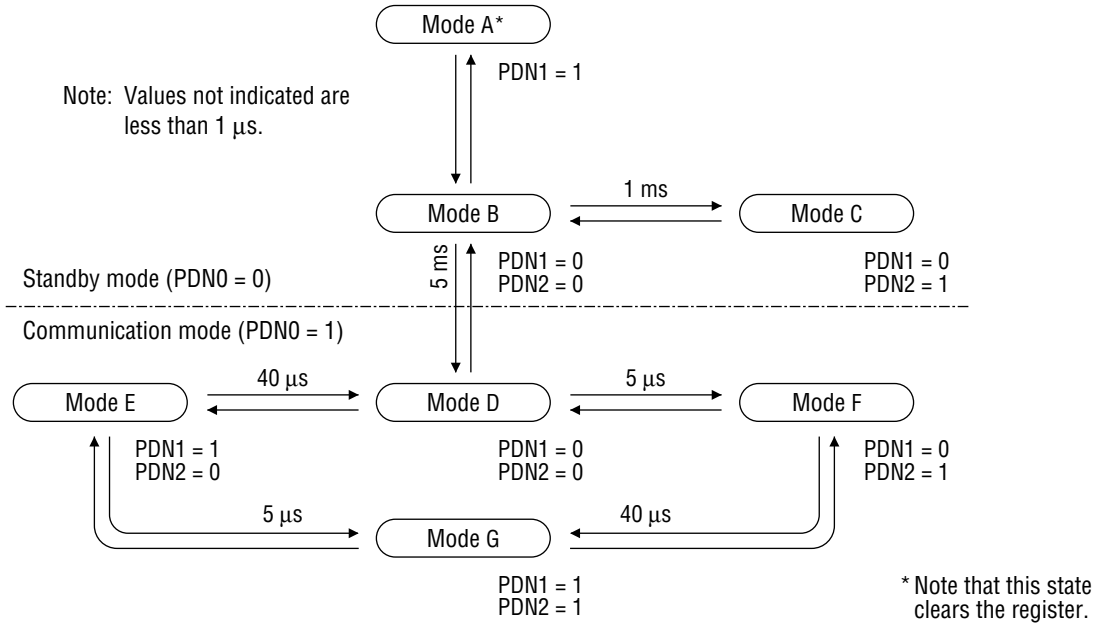


Figure 14 Modem Unit Power Down State Transition Time

Modem Unit Demodulator Control Timing Diagram (Example)

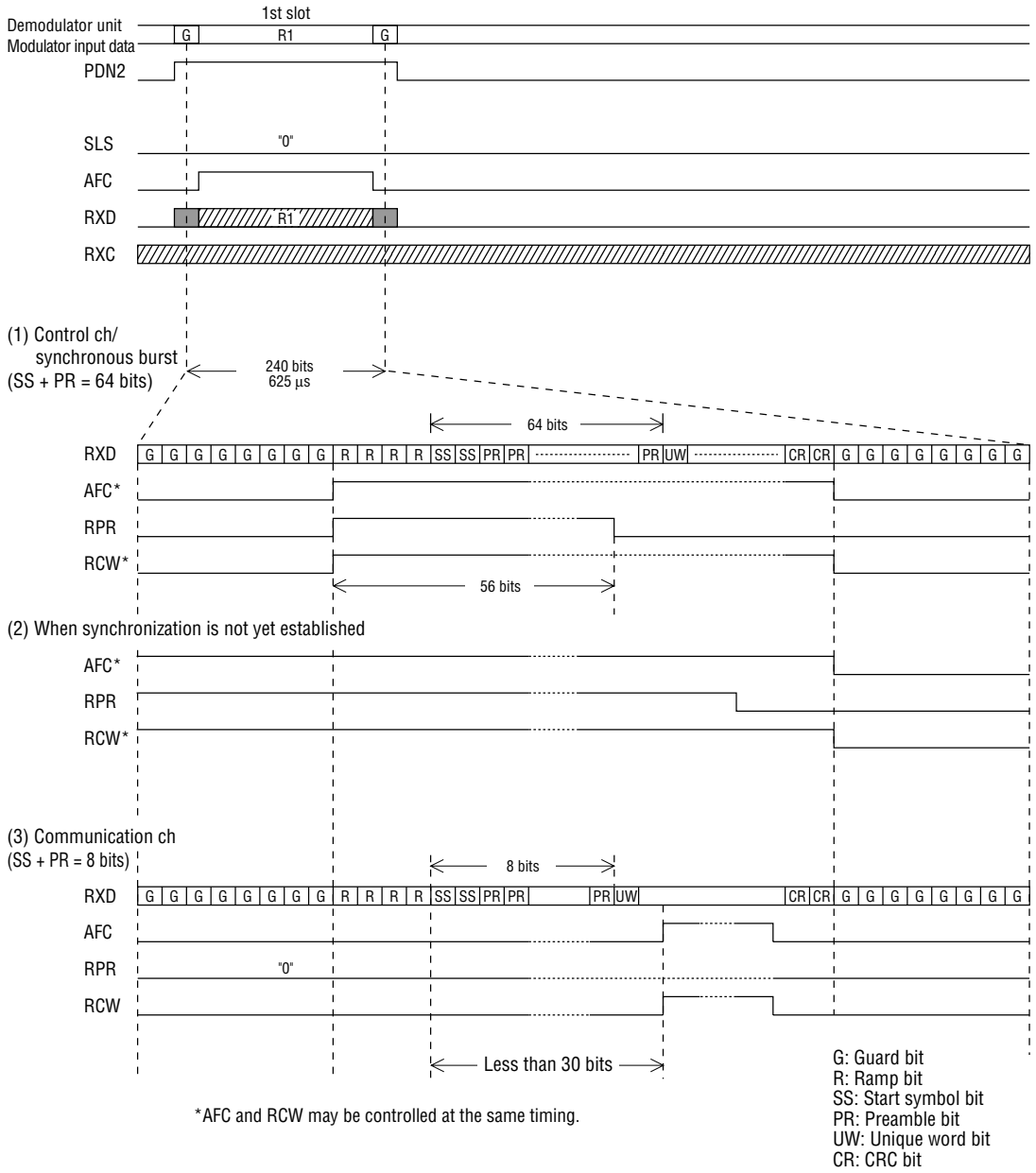


Figure 15 Modem Unit Demodulator Timing Diagram Example

FUNCTIONAL DESCRIPTION

Control Register Description Table (Modem Unit)

(1) CRM0 (Basic Operation Mode Setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM0	—	TXC SEL	MOD OFF	IFSEL1	IFSEL0	—	TEST1	TEST0
Initial Value (Note)	0	0	0	0	0	0	0	0

Note: The initial value is the value set when a reset is applied by the $\overline{\text{RESET}}$ pin.

B7, B2: ..... Not used
B6: ..... Transmission timing clock selection
0: TXCI input: 384 kHz TXCO output: APLL 384 kHz output
Transmission data TXD is input synchronized to the rise of TXCI. APLL is ON.
1: TXCI input: 3.84 MHz TXCO output: 384 kHz (TXCI divided by 10)
Transmission data TXD is input synchronized to the rise of TXCO. APLL is OFF.
B5: Modulation OFF/ON control
0: Modulation ON 1: Modulation OFF
B4, B3: ..... Receive side input IF frequency selection
(0,0), (0,1): 1.2 MHz
(1,0): 10.8 MHz
(1,1): 10.7 MHz/10.75 MHz
B1, B0: ..... Device test control bit
Since it is used for LSI testing, it is normally set to "0."

(2) CRM1 (I and Q Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7 to B4: ....I+ and I- output gain setting: 3 mV steps (refer to Table 4)
B3 to B0: ....Q+ and Q- output gain setting: 3 mV steps (refer to Table 4)

Table 4: I and Q Gain Setting Table

CRM1 - B7 / CRM1 - B3	B6 / B2	B5 / B1	B4 / B0	Description
0	1	1	1	Amplitude value: 1.042 reference value
0	1	1	0	1.036
0	1	0	1	1.030
0	1	0	0	1.024
0	0	1	1	1.018
0	0	1	0	1.012
0	0	0	1	1.006
0	0	0	0	1.000 (Reference value)
1	1	1	1	0.994
1	1	1	0	0.988
1	1	0	1	0.982
1	1	0	0	0.976
1	0	1	1	0.970
1	0	1	0	0.964
1	0	0	1	0.958
1	0	0	0	0.952

(3) CRM2 (Output to R7 to R4 pins)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM2	R7	R6	R5	R4	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 to B4: ....Output to R7 to R4 pin

(4) CRM3 (I- Output Offset Voltage Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM3	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 to B3: ....I- output pin offset voltage adjustment (refer to Table 5)
B2 to B0: ....Not used

(5) CRM4 (Q- Output Offset Voltage Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM4	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—
Initial Value	0	0	0	0	0	0	0	0

B7 to B3: ....Q- output pin offset voltage adjustment (refer to Table 5)
B2 to B0: ....Not used

Table 5: Ich and Qch Offset Adjustment Values

CRM3 - B7 / CRM4 - B7	B6	B5	B4	B3	Offset Voltage	CRM3 - B7 / CRM4 - B7	B6	B5	B4	B3	Offset Voltage
0	1	1	1	1	+45 mV	1	1	1	1	1	–3 mV
0	1	1	1	0	+42 mV	1	1	1	1	0	–6 mV
0	1	1	0	1	+39 mV	1	1	1	0	1	–9 mV
0	1	1	0	0	+36 mV	1	1	1	0	0	–12 mV
0	1	0	1	1	+33 mV	1	1	0	1	1	–15 mV
0	1	0	1	0	+30 mV	1	1	0	1	0	–18 mV
0	1	0	0	1	+27 mV	1	1	0	0	1	–21 mV
0	1	0	0	0	+24 mV	1	1	0	0	0	–24 mV
0	0	1	1	1	+21 mV	1	0	1	1	1	–27 mV
0	0	1	1	0	+18 mV	1	0	1	1	0	–30 mV
0	0	1	0	1	+15 mV	1	0	1	0	1	–33 mV
0	0	1	0	0	+12 mV	1	0	1	0	0	–36 mV
0	0	0	1	1	+9 mV	1	0	0	1	1	–39 mV
0	0	0	1	0	+6 mV	1	0	0	1	0	–42 mV
0	0	0	0	1	+3 mV	1	0	0	0	1	–45 mV
0	0	0	0	0	0 mV	1	0	0	0	0	–48 mV

(6) CRM5 (IC Test)

	B7	B6	B5	B4	B3	B2	B1	B0
CRM5	ICT5	ICT4	ICT3	ICT2	LOCAL INV1	LOCAL INV0	ICT1	ICT0
Initial Value	0	0	0	0	0	0	0	0

B7 to B4: ....LSI test control bit

Note: Since B7 to B4 of CRM5 are used for LSI testing, they should normally be set to "0".

B3, B2: .....Local inverted mode setting bit
(Use if the phase of the demodulator side IF input is inverted due to the system configuration.)
(0,0): Normal mode(1,1): Local inverted mode

B1: .....Waveform shaping mode switching bit of the oscillator circuit unit clock
(When using a master clock external input, increase the X1 pin input sensitivity.)
0: Normal mode 1: Clock waveform shaping mode

B0: .....Oscillator circuit unit power on control bit
0: Normal mode 1: Oscillator circuit unit is always powered on

(CODEC Unit)

(1) CRC0 (Basic Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC0	A/μ SEL	—	PDN ALL	—	—	—	—	PDN SAO/AOUT
Initial Value	0	0	0	0	0	0	0	0

B7: ..... PCM interface companding selection 0: μ-law 1: A-law
B6, B4, B3, B2, B1: . Not used (These pins are used to test the device. They should be set to "0" during normal operation.)
B5: ..... Power down (entire unit) 0: Power ON 1: Power down
ORed with the inverse of the external power down signal. When using this data, set $\overline{\text{PDN3}}$ to "1."
B0: ..... The sounder output amp (SAO, GSX3) and receiver system output amp (VFRO, AOUT+, AOUT-) power down control
0: The output amp of the side not selected by CRC4 - B5 is powered down.
1: The sounder system output amp and receiver system output amp are both powered ON.

(2) CRC1 (ADPCM Unit Operation Mode Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD
Initial Value	0	0	0	0	0	0	0	0

B7, B6: ..... ADPCM unit compression algorithm selection
(0,0): 32 kbps (0,1): 64 kbps (G.711 through)
(1,0): 24 kbps (1,1): 16 kbps
B5: ..... Transmit side ADPCM reset (according to the G.726 specifications): 1: Reset
The ADPCM reset input width should be 125 μs or more.
B4: ..... Receive side ADPCM reset (according to the G.726 specifications): 1: Reset
The ADPCM reset input width should be 125 μs or more.
B3: ..... Transmit side ADPCM data mute: 1: Mute
B2: ..... Receive side ADPCM data mute: 1: Mute
B1: ..... Not used
B0: ..... Receive side PAD 0: No PAD
1: A PAD with a 12 dB loss is inserted in the receive side voice path

(3) CRC2 (PCM CODEC Unit Operation Mode Settings and Transmit/Receive Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7: ..... Transmit side PCM signal ON/OFF 0: ON 1: OFF
When OFF, transmits a PCM idle pattern.
B6, B5, B4: Transmit side signal gain adjustment (refer to Table 6)
B3: ..... Receive side PCM signal ON/OFF 0: ON 1: OFF
When OFF transmits a PCM idle pattern.
B2, B1, B0: . Receive side signal gain adjustment (refer to Table 6)

Table 6: Receive/Transmit Gain Settings

• MSM7586-01

B6	B5	B4	Transmit Side Gain	B2	B1	B0	Receive Side Gain
0	0	0	–6 dB	0	0	0	–6 dB
0	0	1	–4 dB	0	0	1	–4 dB
0	1	0	–2 dB	0	1	0	–2 dB
0	1	1	0 dB	0	1	1	0 dB
1	0	0	+2 dB	1	0	0	+2 dB
1	0	1	+4 dB	1	0	1	+4 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+8 dB

• MSM7586-03

B6	B5	B4	Transmit Side Gain	B2	B1	B0	Receive Side Gain
0	0	0	–6 dB	0	0	0	–12 dB
0	0	1	–4 dB	0	0	1	–9 dB
0	1	0	–2 dB	0	1	0	–6 dB
0	1	1	0 dB	0	1	1	–3 dB
1	0	0	+2 dB	1	0	0	0 dB
1	0	1	+4 dB	1	0	1	+3 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+9 dB

The above gain settings table shows the transmit/receive voice signal gain settings and the transmit side gain settings for DTMF tones and other tones. Tone signal transmission is enabled by CRC4 - B6 (discussed later), and the gain setting is set to the levels shown below.

DTMF tones (low group): ..... –16 dBm0
DTMF tones (high group) and other tones: ... –14 dBm0

For example, if the transmit gain set value is set to +8 dB (B6, B5, B4) = (1, 1, 1), then the following tones appear at the PCMSO pin.

DTMF tones (low group): ..... –8 dBm0
DTMF tones (high group) and other tones: ... –6 dBm0

However, the gain of the receive side tone and the gain of the side tones (path from transmit side to receive side) are set by the CRC3 register.

(4) CRC3 (Side Tone and Tone Generator Gain Adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	TONE ON/OFF	TONE GAIN3	TONE GAIN2	TONE GAIN1	TONE GAIN0
Initial Value	0	0	0	0	0	0	0	0

B7, B6, B5: ..... Side tone gain adjustment (refer to Table 7)
B4: ..... Tone generator ON/OFF 0: OFF 1: ON
B3, B2, B1, B0: . Tone generator Receive side gain adjustment (refer to Table 8)

Table 7: Side Tone Gain Settings

• MSM7586-01

B7	B6	B5	Side Tone Gain
0	0	0	OFF
0	0	1	–21 dB
0	1	0	–19 dB
0	1	1	–17 dB
1	0	0	–15 dB
1	0	1	–13 dB
1	1	0	–11 dB
1	1	1	– 9 dB

• MSM7586-03

B7	B6	B5	Side Tone Gain
0	0	0	OFF
0	0	1	–15 dB
0	1	0	–13 dB
0	1	1	–11 dB
1	0	0	– 9 dB
1	0	1	– 7 dB
1	1	0	– 5 dB
1	1	1	– 3 dB

Table 8: Receive Side Tone Generator Gain Settings

• MSM7586-01

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	–36 dB	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	– 8 dB
1	1	1	1	–22 dB	1	1	1	1	– 6 dB

• MSM7586-03

B3	B2	B1	B0	Tone Generator Gain	B3	B2	B1	B0	Tone Generator Gain
0	0	0	0	OFF	1	0	0	0	–20 dB
0	0	0	1	–34 dB	1	0	0	1	–18 dB
0	0	1	0	–32 dB	1	0	1	0	–16 dB
0	0	1	1	–30 dB	1	0	1	1	–14 dB
0	1	0	0	–28 dB	1	1	0	0	–12 dB
0	1	0	1	–26 dB	1	1	0	1	–10 dB
0	1	1	0	–24 dB	1	1	1	0	– 8 dB
1	1	1	1	–22 dB	1	1	1	1	– 6 dB

The receive side tone generator gain settings shown in Table 8 are set with the following levels as a reference.

DTMF tones (low group): ..... –2 dBm0
DTMF tones (high group) and other tones: ... 0 dBm0

For example, if the tone generator gain set value is set to -6 dB (B3, B2, B1, B0)=(1, 1, 1, 1), then tones at the following levels appear at the SAO or VFRO pin.

DTMF tones (low group): ..... –8 dBm0
DTMF tones (high group) and other tones: ... –6 dBm0

(5) CRC4 (Tone Generator Operation Mode and Frequency Settings)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC4	DTMF/OTHERS SEL	TONE SEND	SAO/VFRO	TONE4	TONE3	TONE2	TONE1	TONE0
Initial Value	0	0	0	0	0	0	0	0

B7: ..... Selection of DTMF signal and other tones
(S tone, F tone, R tone, etc.) 0: Other tones 1: DTMF tones
B6: ..... Transmission side tone transmit
0: Voice signal transmit 1: Tone transmit
B5: ..... Receive side tone output pin selection
0: VFRO output 1: SAO output
B4, B3, B2, B1, B0: . Tone frequency setting (refer to Table 9)

Table 9: Tone Generator Frequency Settings

(a) When B7 = 1 (DTMF Tones)

B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
*	0	0	0	0	697 Hz + 1209 Hz	*	1	0	0	0	852 Hz + 1209 Hz
*	0	0	0	1	697 Hz + 1336 Hz	*	1	0	0	1	852 Hz + 1336 Hz
*	0	0	1	0	697 Hz + 1477 Hz	*	1	0	1	0	852 Hz + 1477 Hz
*	0	0	1	1	697 Hz + 1633 Hz	*	1	0	1	1	852 Hz + 1633 Hz
*	0	1	0	0	770 Hz + 1209 Hz	*	1	1	0	0	941 Hz + 1209 Hz
*	0	1	0	1	770 Hz + 1336 Hz	*	1	1	0	1	941 Hz + 1336 Hz
*	0	1	1	0	770 Hz + 1477 Hz	*	1	1	1	0	941 Hz + 1477 Hz
*	0	1	1	1	770 Hz + 1633 Hz	*	1	1	1	1	941 Hz + 1633 Hz

(b) When B7 = 0 (Outside of DTMF Tones)

B4	B3	B2	B1	B0	Description	B4	B3	B2	B1	B0	Description
0	0	0	0	0	2730 Hz/2500 Hz 8 Hz Wamble	1	0	0	0	0	—
0	0	0	0	1	2000 Hz/2667 Hz 8 Hz Wamble	1	0	0	0	1	1300 Hz Single tone
0	0	0	1	0	1000 Hz/1333 Hz 8 Hz Wamble	1	0	0	1	0	1333 Hz Single tone
0	0	0	1	1	—	1	0	0	1	1	—
0	0	1	0	0	—	1	0	1	0	0	—
0	0	1	0	1	—	1	0	1	0	1	2000 Hz Single tone
0	0	1	1	0	—	1	0	1	1	0	—
0	0	1	1	1	—	1	0	1	1	1	—
0	1	0	0	0	—	1	1	0	0	0	—
0	1	0	0	1	400 Hz Single tone	1	1	0	0	1	—
0	1	0	1	0	—	1	1	0	1	0	—
0	1	0	1	1	—	1	1	0	1	1	—
0	1	1	0	0	—	1	1	1	0	0	2667 Hz Single tone
0	1	1	0	1	—	1	1	1	0	1	—
0	1	1	1	0	—	1	1	1	1	0	2730 Hz Single tone
0	1	1	1	1	1000 Hz Single tone	1	1	1	1	1	—

(6) CRC5 (Control of Switches, etc.)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC5	SW1 CONT	SW2 CONT	SW3 CONT	SW4/5 CONT	—	TOUT3 CONT	TOUT2 CONT	TOUT1 CONT
Initial Value	0	0	0	0	0	0	0	0

B7, B6: .....SW1, SW2 control 0: Open 1: Closed
B5: .....SW3 control 0: Open 1: Closed
B4: .....SW4/5 control 0: SW4 open, SW5 closed
1: SW4 closed, SW5 open
B2, B1, B0: . TOUT3 to 1 control 0: TOUT3 to 1 disable
1: TOUT3 to 1 enable

(7) CRC6 (VOX Function Control)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC6	VOX ON/OFF	ON LVL1	ON LVL0	OFF TIME	VOX IN	RX NOISE LEVEL SEL	RX NOISE LVL1	RX NOISE LVL0
Initial Value	0	0	0	0	0	0	0	0

B7: ..... VOX function ON/OFF 0: OFF 1: ON
B6, B5: .....Transmit side voice/silence detector level settings (For the signal of 1kHz)
MSM7586-01
(0,0): –30 dBm0 (0,1): –35 dBm0
(1,0): –40 dBm0 (1,1): –45 dBm0
MSM7586-03
(0,0): –20 dBm0 (0,1): –26 dBm0
(1,0): –32 dBm0 (1,1): –38 dBm0
B4: ..... Hangover time (refer to Fig. 7) settings 0: 160 ms 1: 320 ms
B3: .....Receive side VOX input signal
0: Internal background noise transmit 1: Voice receive signal transmit
When using this data, set the VOXI pin to "0."
B2: .....Receive side background noise level setting
0: Internal automatic setting 1: External (by B1, B0) setting
Internal automatic setting → Sets to the voice signal level when B3 (VOXI) changes from "1" to "0."
B1, B0: .....External setting background noise level
(0,0): No noise (0,1): –55 dBm0
(1,0): –45 dBm0 (1,1): –35 dBm0

(8) CRC7 (Detect Register: Read-only)

	B7	B6	B5	B4	B3	B2	B1	B0
CRC7	VOX OUT	Silent Level 1	Silent Level 0	—	—	—	—	—
Initial Value	0	0	0	*	*	*	*	*

B7: ..... Transmit side voice/silence detection 0: Silence 1: Voice

B6, B5: ..... Transmit side silence level (indicator)

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(0,0):Below –60 dBm0 (0,1): –50 to –60 dBm0

(1,0): –40 to –50 dBm0 (1,1): Above –40 dBm0

MSM7586-03

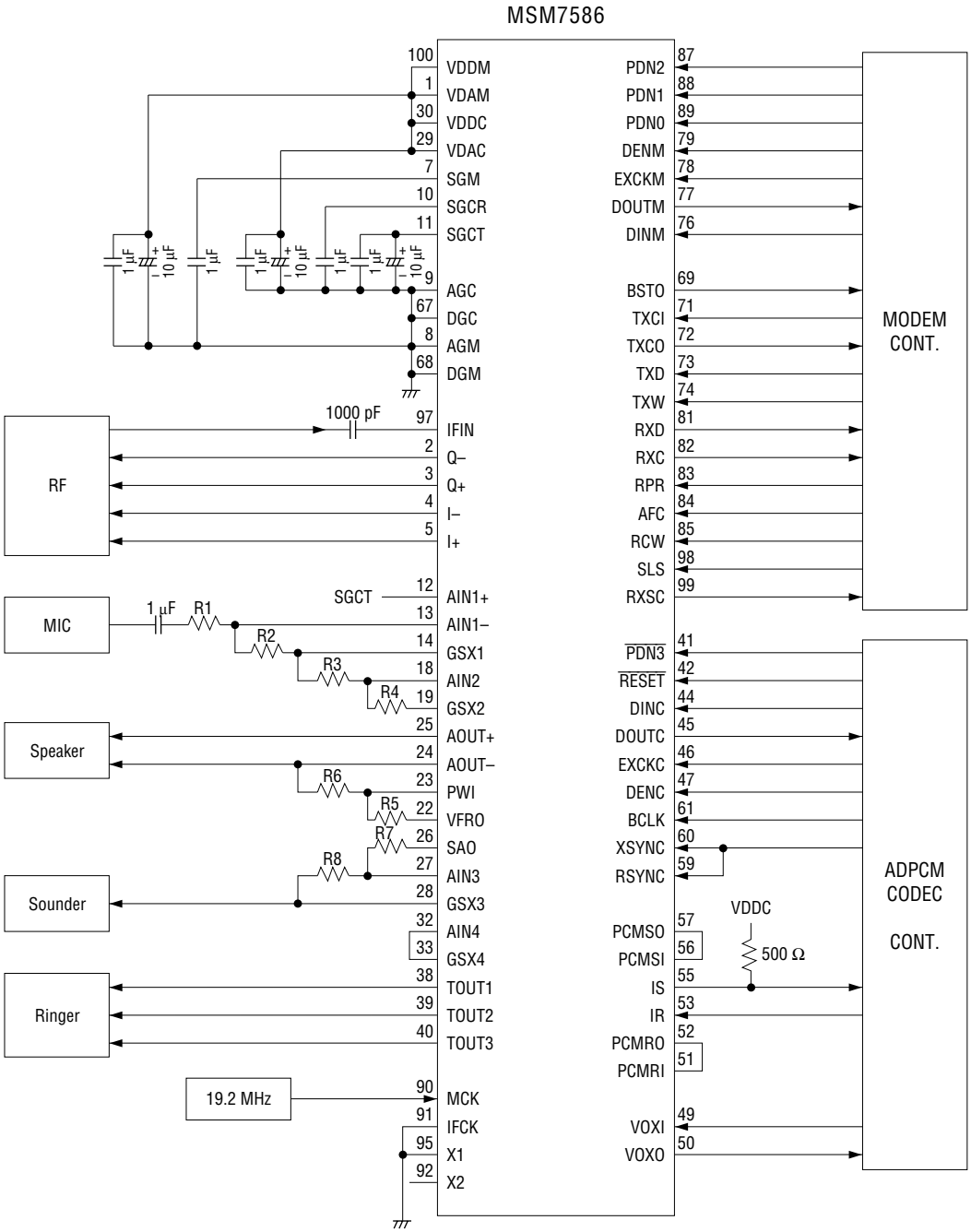
(0,0):Below –50 dBm0 (0,1): –40 to –50 dBm0

(1,0): –30 to –40 dBm0 (1,1): Above –30 dBm0

Note: These outputs are enabled when the VOX function is turned ON by CRC6 - B7.

B4, B3, B2, B1, B0: . Not used

APPLICATION CIRCUIT

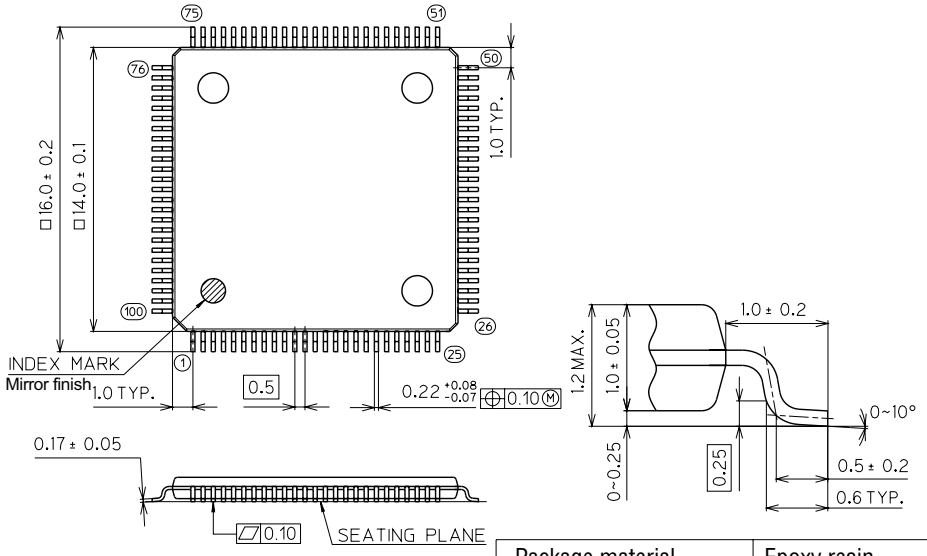


R1 ≥ Output drive resistance of MIC
R2//R3 ≥ 20 kΩ
R4, R5, R7 ≥ 20 kΩ
R6//Input resistance of speaker ≥ 1.2 kΩ
R8//Input resistance of sounder ≥ 150 Ω

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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