OKI Semiconductor

This version: Sep. 1998
Previous version: Mar. 1996

MSM6408

High speed and High performance 4-Bit Microcontroller

GENERAL DESCRIPTION

The MSM6408 microcontroller is a low-power, single-chip device implemented in complementary metal-oxide semiconductor technology.
The MSM6408 is optimized for high-speed processing and complicated-control applications, in which conventional microcontrollers are difficult to use.

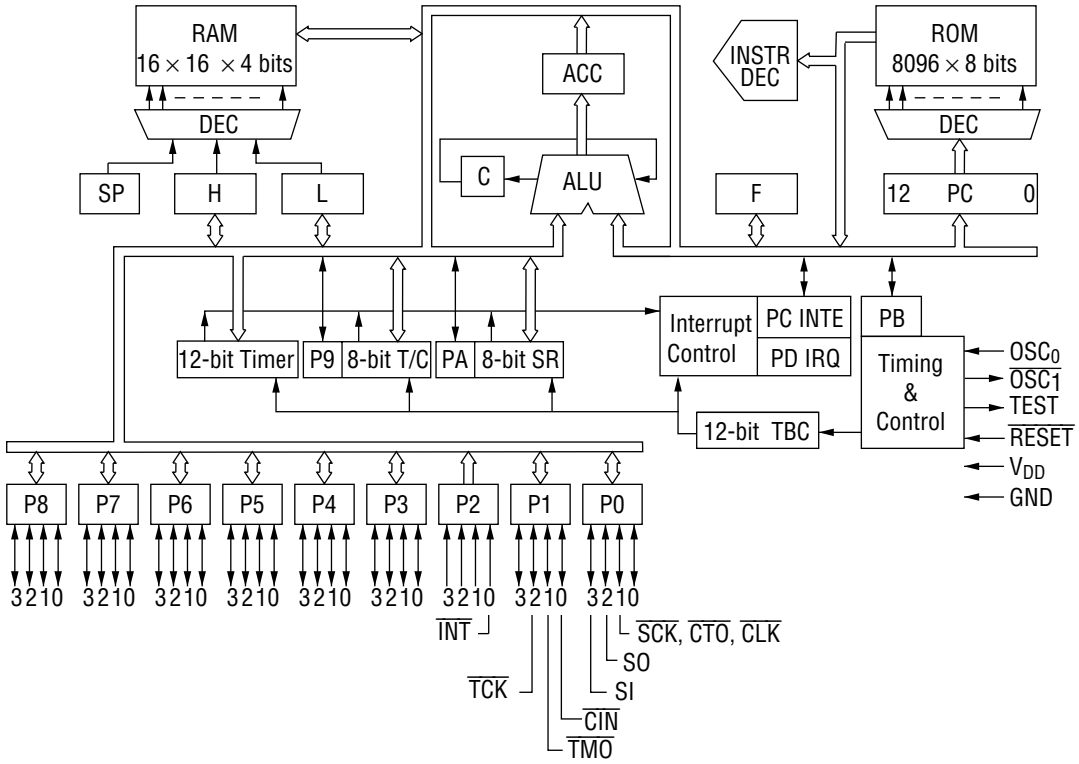
FEATURES

- Mask ROM : 8096 words × 8 bits
- RAM (including the stack area) : 256 words × 4 bits
- I/O port
  - Input-output port : 8 ports × 4 bits
  - Input port : 1 port × 4 bits

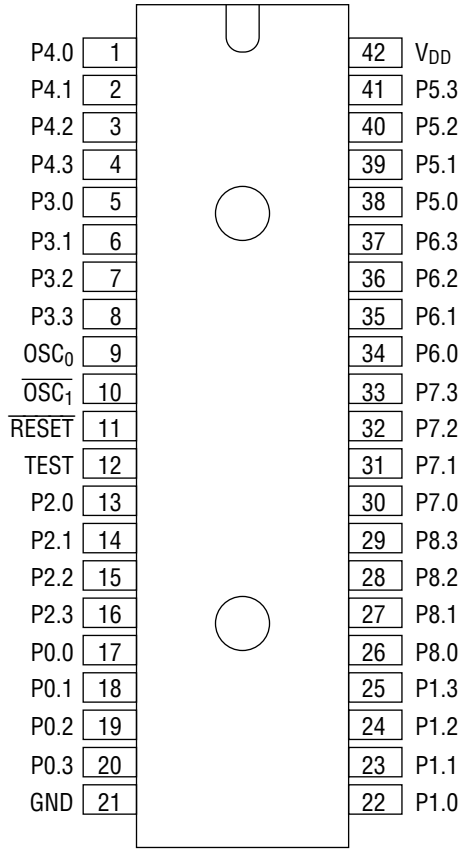
  4 bits are for input ports having a latch; the other 32 bits are for input/output ports that allow bit manipulation
- Three built-in counters : 12-bit time-base counter
  12-bit programmable timer
  8-bit high-speed programmable timer/event counter
- Built-in 8-bit serial I/O register (with 3-bit counter)
- Five interrupts with five priority levels (4 internal, 1 external)
- 32 stack levels (in RAM)
- Power down features
- Minimum instruction execution time : 1.0 µs @ 4.0 MHz clock
- Instruction systems suitable for control
- Fully static operation
- Low power consumption
- Single 5 V power supply
- Package options:
  - 42-pin plastic DIP (DIP42-P-600-2.54) (Product name : MSM6408-×××RS)
  - 44-pin plastic QFP (QFP44-P-910-0.80-K) (Product name : MSM6408-×××GS-K)
  - 44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name : MSM6408-×××GS-2K)

  ××× indicates a code number.

BLOCK DIAGRAM

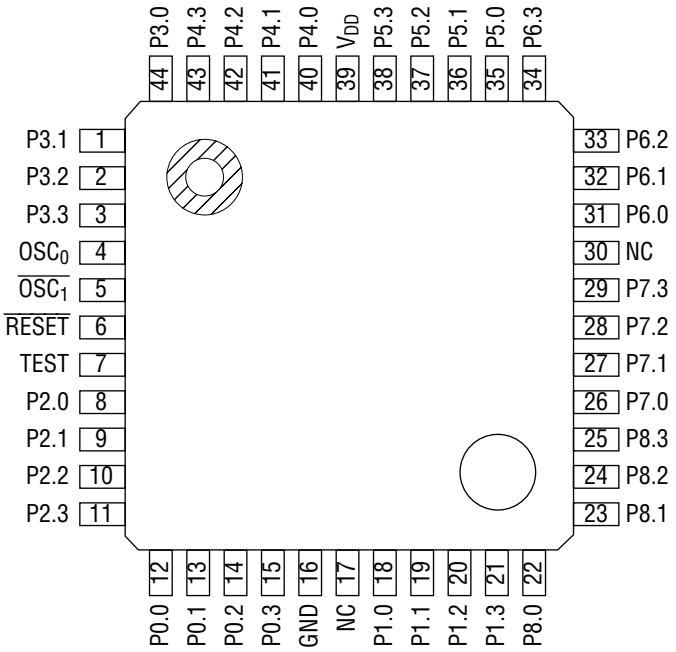


PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

PIN CONFIGURATION (TOP VIEW) (continued)



NC : No-connection pin

44-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description	During reset
P0.0 P0.1/$\overline{SCK}$ P0.2/SO P0.3/SI	I/O	P0.1 is shared with serial clock ($\overline{SLK}$) input/output. P0.2 is shared with serial data (SO) output. P0.3 is shared with serial data (SI) input.	"1"
P1.0/$\overline{CIN}$ P1.1/$\overline{TMO}$ P1.2/$\overline{TCK}$ P1.3	I/O	P1.0 is shared with counter input ($\overline{CIN}$). P1.1 is shared with timer output ($\overline{TMO}$). P1.2 is shared with timer clock input ($\overline{TCK}$).	"1"
P2.0/$\overline{INT}$ P2.1 P2.2 P2.3	I	P2.0 is shared with external interrupt input ($\overline{INT}$). Input ports with a latch, with built-in pull-up resistor.	The latch is reset.
P3.0 to 3.3	I/O	—	"1"
P4.0 to 4.3	I/O	—	"0"
P5.0 to 5.3	I/O	—	"0"
P6.0 to 6.3	I/O	—	"0"
P7.0 to 7.3	I/O	—	"0"
P8.0 to 8.3	I/O	—	"0"
OSC_0	I	Crystal connection pins for clock oscillation.	Oscillation waveform
$\overline{OSC_1}$	O		
TEST	O	(Test pin for manufacturer)	Pulse output
$\overline{RESET}$	I	Input pin for system reset.	—
V_{DD} GND	—	Power supply voltage pins.	—

Note: 1. The pins except for pins P2.0 to P2.3 are pseudo bidirectional ports.
2. When each port is used for output, the MSM6408 can drive one TTL (one input).

INSTRUCTION LIST

	Mnemonic	Code	Byte	Cycle	Description
Load, Push, Pop	LAI n	9n	1	1	A←n
	LLI n	8n	1	1	L←n
	LHLI nn	15nn	2	2	HL←nn
	LMI nn	14nn	2	2	M(w)←nn
	LAL	21	1	1	A←L
	LLA	2D	1	1	L←A
	LAH	22	1	1	A←H
	LHA	2E	1	1	H←A
	LAM	38	1	1	A←M
	LMA	2F	1	1	M←A
	LAM+	24	1	1	A←M, L←L + 1,Skip if L = 0
	LAM–	25	1	1	A←M, L←L – 1,Skip if L = F
	LMA+	26	1	1	M←A, L←L + 1,Skip if L = 0
	LMA–	27	1	1	M←A, L←L – 1,Skip if L = F
	LAMM n_2	39-3B	1	1	A←M, H←H∀n_2
	LAMD mm	10mm	2	2	A←Md
	LMAD mm	11mm	2	2	Md←A
	LMTD mm	19mm	2	3	Md(w)←T (M(w), A), T = ROM table
	LMCT	3E59	2	2	M(w)←CT
	LCTM	3E51	2	2	CT←M(w)
	LMSR	3E5A	2	2	M(w)←SR
	LSRM	3E52	2	2	SR←M(w)
	LTMM	3E50	2	2	TM←(M(w), A)
	PUSH	1C	1	3	ST←C, A, H, L, SP←SP – 4
	POP	1D	1	3	C, A, H, L, ←ST SP←SP + 4
Exchange	X	28	1	1	A↔M
	XM n_2	29-2B	1	1	A↔M, H←H∀n_2
	X+	3C	1	1	A↔M, L←L+1, Skip if L = 0
	X–	2C	1	1	A↔M, L←L–1, Skip if L = F
Increment/ Decrement	INA	30	1	1	A←A + 1, Skip if A = 0
	INM	33	1	1	A←M + 1, Skip if M = 0
	INL	31	1	1	L←L + 1, Skip if L = 0

INSTRUCTION LIST (continued)

	Mnemonic	Code	Byte	Cycle	Description
Increment/Decrement	INH	32	1	1	H←H + 1, Skip if M = 0
	INMD mm	12mm	2	2	Md←Md + 1, Skip if Md = 0
	DCA	34	1	1	A←A – 1, Skip if A = F
	DCM	37	1	1	M←M – 1, Skip if M = F
	DCL	35	1	1	L←L – 1, Skip if L = F
	DCH	36	1	1	H←H – 1, Skip if H = F
	DCMD mm	13mm	2	2	Md←Md – 1, Skip if Md = F
Arithmetic	ADS	02	1	1	A←A + M, Skip if Cy = 1
	ADCS	01	1	1	A, C←A + M + C, Skip if Cy =1
	ADC	03	1	1	A, C←A + M + C
	AIS n	3E4n	2	2	A←A + n, Skip if Cy = 1
	DAA	06	1	1	A←A + 6
	DAS	0A	1	1	A←A + 10
	AND	0D	1	1	A←A∧M
	OR	05	1	1	A←A∨M
	EOR	04	1	1	A←A∀M
	CMA	0B	1	1	A←$\overline{A}$
	CIA	0C	1	1	A←$\overline{A}$ + 1
	RAL	0E	1	1	Rotate left with C
	RAR	0F	1	1	Rotate right with C
	TC	09	1	1	Skip if C = 1
	SC	07	1	1	C←1
	RC	08	1	1	C←0
Compare	CAI n	3E0n	2	2	Skip if A = n
	CLI n	3E2n	2	2	Skip if L = n
	CPI p, n	17pn	2	2	Skip if Pp = n
	CMI n	3E1n	2	2	Skip if M = n
	CAM	16	1	1	Skip if A = M
Bit manipulation	TAB n_2	54-57	1	1	Skip if Abit (n_2) = 1
	RAB n_2	64-67	1	1	Abit (n_2)←0
	SAB n_2	74-77	1	1	Abit (n_2)←1
	TMB n_2	58-5B	1	1	Skip if Mbit (n_2) = 1
	RMB n_2	68-6B	1	1	Mbit (n_2)←0

INSTRUCTION LIST (continued)

	Mnemonic	Code	Byte	Cycle	Description
Bit manipulation	SMB n	78-7B	1	1	Mbit (n_2)←1
	TFB n_2	5C-5F	1	1	Skip if Fbit (n_2) = 1
	RFB n_2	6C-6F	1	1	Fbit (n_2)←0
	SFB n_2	7C-7F	1	1	Fbit (n_2)←1
	TPB n_2	50-53	1	1	Skip if Pbit (n_2) = 1
	RPB n_2	60-63	1	1	Pbit (n_2)←0
	SPB n_2	70-73	1	1	Pbit (n_2)←1
	TPBD pn_2	30 p_{0-3}	2	2	Skip if Ppbit (n_2) = 1
	RPBD pn_2	3D p_{4-7}	2	2	Ppbit (n_2) = 0
	SPBD pn_2	3D p_8-B	2	2	Ppbit (n_2) = 1
Interrupt	MEI	3E60	2	2	MEIF←1
	MDI	3E61	2	2	MEIF←0
	EITB	3DC9	2	2	EITBF←1
	EITM	3DCA	2	2	EITMF←1
	EICT	3DCB	2	2	EICTF←1
	EIEX	3DC8	2	2	EIEXF←1
	DITB	3DC5	2	2	EITBF←0
	DITM	3DC6	2	2	EITMF←0
	DICT	3DC7	2	2	EICTF←0
	DIEX	3DC4	2	2	EIEXF←0
	TITB	3DC1	2	2	Skip if EITBF = 1
	TITM	3DC2	2	2	Skip if EITMF = 1
	TICT	3DC3	2	2	Skip if EICTF = 1
	TIEX	3DC0	2	2	Skip if EIEXF = 1
	TQEX	3D20	2	2	Skip if IRQEX = 1
	TQTB	3DD0	2	2	Skip if IRQTB = 1
	TQTM	3DD1	2	2	Skip if IRQTM = 1
	TQCT	3DD2	2	2	Skip if IRQCT = 1
	TQSR	3DD3	2	2	Skip if IRQSR = 1
	RQEX	3D24	2	2	IRQ EX←0
	RQTB	3DD4	2	2	IRQ TB←0
	RQTM	3DD5	2	2	IRQ TM←0
	RQCT	3DD6	2	2	IRQ CT←0
	RQSR	3DD7	2	2	IRQ SR←0

INSTRUCTION LIST (continued)

	Mnemonic	Code	Byte	Cycle	Description
Counter/Shift register control	ECT	3DBB	2	2	CTF←1 (start)
	ESR	3DBA	2	2	SRF←1 (start)
	DCT	3DB7	2	2	CTF←0 (stop)
	DSR	3DB6	2	2	SRF←0 (stop)
	TCT	3DB3	2	2	Skip if CTF = 1
	TSR	3DB2	2	2	Skip if SRF = 1
Branch	JCP a_6	C0-FF	1	1	PC←a_6
	JP a_{12}	$4a_{12}$	2	2	PC←a_{12}
	LJP a_{13}	3F	3	4	PC←a_{13}
	CZP a	Ba	1	4	ST←PC + 1, PC←2a, SP←SP – 4
	CAL a_{12}	Aa_{12}	2	4	ST←PC + 2, PC←a_{12}, SP←SP – 4
	RT	IE	1	4	PC←ST, SP←SP + 4
	RTS	IF	1	4	PC←ST, SP←SP + 4, Unconditional skip
	JA	IA	1	1	PC←(PC←A) + 1
	JM	IB	1	2	PC←(M(w), A)
Input/Output	IP	20	1	1	A←P
	IPD p	3DpD	2	2	A←Pp
	OP	23	1	1	P←A
	OPD p	3DpC	2	2	Pp←A
CPU control	NOP	00	1	1	No operation
	HALT	3DB8	2	2	Halt CPU
	STOP	3DB9	2	2	Stop clock

Notes: a : ROM address data
m : RAM address data
n : Immediate data
p : Port address data

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Input Voltage	V_I		–0.3 to V_{DD}	V
Output Voltage	V_O		–0.3 to V_{DD}	V
Power Dissipation	P_D	Ta = 25°C per package	200	mW
		Ta = 25°C per output	50	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 1$ MHz	3 to 6	V
		$f_{OSC} \leq 4.0$ MHz	4.5 to 5.5	V
Data-Hold Voltage	V_{DDH}	f_{OSC} = 0 Hz	2 to 6	V
Operating Temperature	T_{op}	—	–40 to +85	°C
Fan Out	N	MOS load	15	—
		TTL load	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5 V ±10%, Ta = –40 to +85°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	*1, *2	V_{IH}	—	2.4	—	V_{DD}	V
"H" Input Voltage	*3, *4	V_{IH}	—	3.6	—	V_{DD}	V
"L" Input Voltage		V_{IL}	—	–0.3	—	+0.8	V
"H" Output Voltage	*1, *5	V_{OH}	I_O = –15 µA	4.2	—	—	V
"L" Output Voltage	*1	V_{OL}	I_O = 1.6 mA	—	—	0.4	V
"L" Output Voltage	*5	V_{OL}	I_O = 15 µA	—	—	0.4	V
Input Current	*3	I_{IH}/I_{IL}	$V_I = V_{DD}/0$ V	—	—	15/–15	µA
Input Current	*2, *4	I_{IH}/I_{IL}	$V_I = V_{DD}/0$ V	—	—	1/–30	µA
"H" Output Current	*1	I_{OH}	V_O = 2.4 V	–0.1	—	—	mA
"H" Output Current	*1	I_{OH}	V_O = 0.4 V	—	—	–1.2	mA
Input Capacitance		C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output Capacitance		C_O		—	7	—	
Power Supply Current (In Stopped State)		I_{DDS}	V_{DD} = 2 V, no load, Ta = 25°C	—	0.2	5	µA
			No load	—	1	100	µA
Power Supply Current		I_{DD}	Crystal oscillation f = 4 MHz, no load	—	6	12	mA

*1 Applied to P0, P1, P3, P4, P5, P6, P7 and P8
*2 Applied to P2
*3 Applied to OSC_0
*4 Applied to $\overline{RESET}$
*5 Applied to $\overline{OSC_1}$

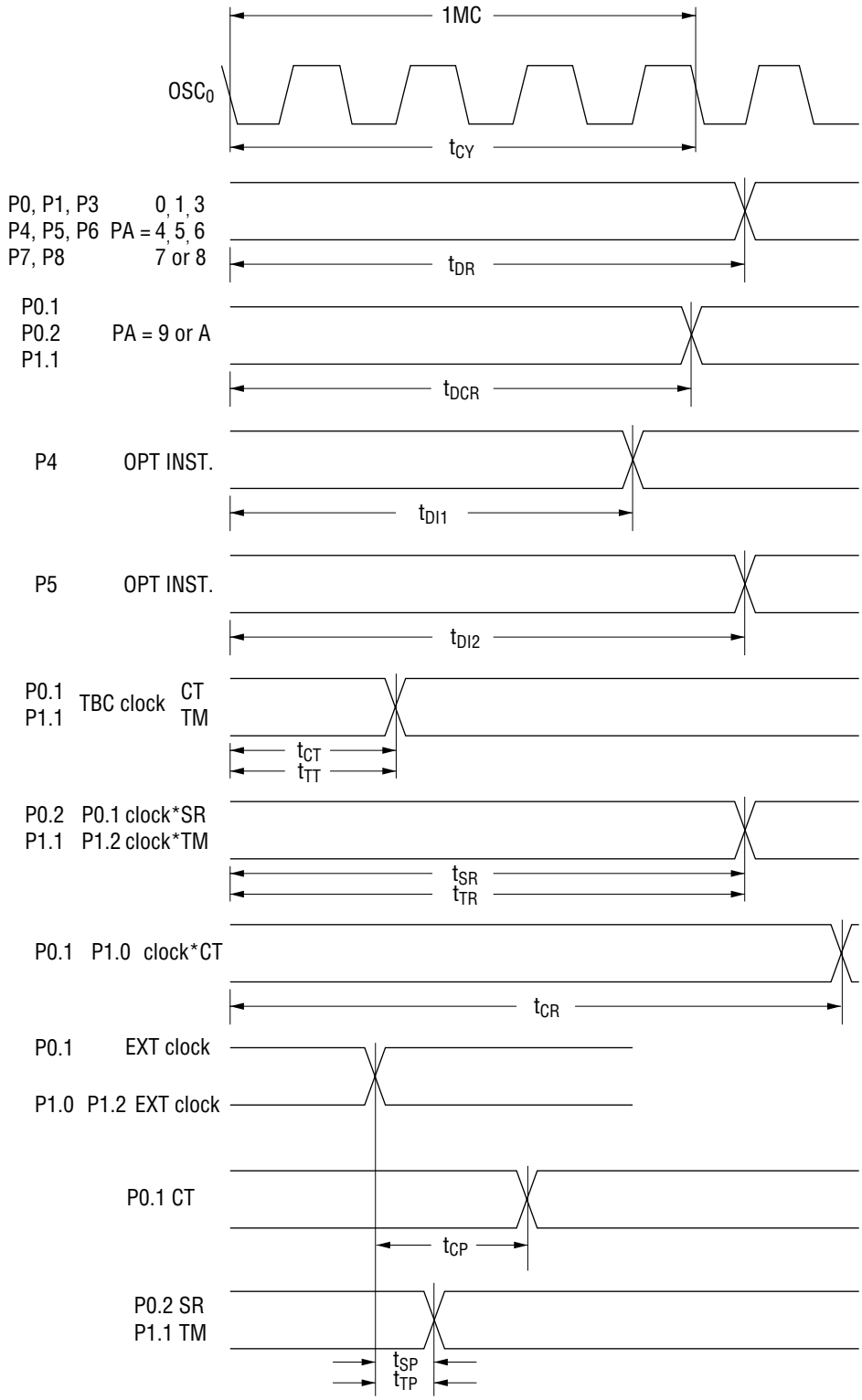
AC Characteristics

(V_{DD} = 5 V ±10%, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock (OSC_0) Pulse Width	$t_{\phi W}$	—	125	—	—	ns
Cycle Time	t_{CY}	—	1	—	—	µs
Input Data Setup Time	t_{DS}	—	120	—	—	ns
Input Data Hold Time	t_{DH}	—	120	—	—	ns
SR/TM Clock Pulse Width	t_{WS}/t_{WT}	—	120	—	—	ns
CT Clock Pulse Width	t_{WC}	—	2/8 t_{CY} + 120	—	—	ns
P2 Input Data Clock Pulse Width	t_{WP}	—	120	—	—	ns
SR Data Setup Time	t_{SS}	—	120	—	—	ns
SR Data Hold Time	t_{SH}	—	120	—	—	ns
Data Delay Time	t_{DR}	C_L = 15 pF	—	—	t_{CY} + 300	ns
Data Delay Time at Mode Switching	t_{DCR}	C_L = 15 pF	—	—	7/8 t_{CY} + 300	ns
Data Delay Time at OPT Instruction	t_{DI1}	C_L = 15 pF	—	—	6/8 t_{CY} + 300	ns
Data Delay Time at OPT Instruction	t_{DI2}	C_L = 15 pF	—	—	7/8 t_{CY} + 300	ns
CT/TM Data Delay Time Using TBC Clock	t_{CT}/t_{TT}	C_L = 15 pF	—	—	2/8 t_{CY} + 360	ns
SR/TM Data Delay Time Using PORT Clock	t_{SR}/t_{TR}	C_L = 15 pF	—	—	t_{CY} + 480	ns
CT Data Delay Time Using PORT Clock	t_{CR}	C_L = 15 pF	—	—	10/8 t_{CY} + 480	ns
CT Data Delay Time Using External Clock	t_{CP}	C_L = 15 pF	—	—	2/8 t_{CY} + 360	ns
SR/TM Data Delay Time Using External Clock	t_{SP}/t_{TP}	C_L = 15 pF	—	—	360	ns
SR Clock Invalid Time	t_{SINH}	—	2/8 t_{CY}	—	—	ns
INT Invalid Time	t_{IINH}	—	1/8 t_{CY}	—	—	ns

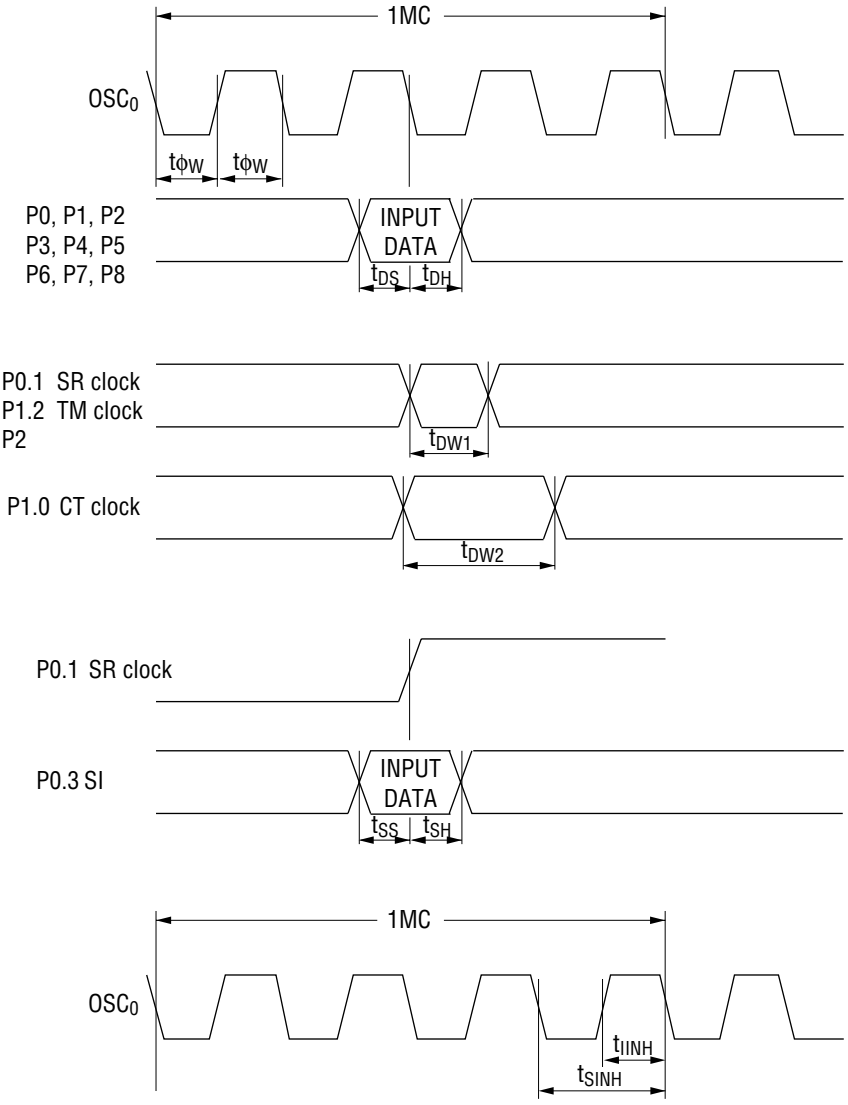
Timing Diagrams

Output Conditions



* Output data to port is clock for SR, TM or CT.

Input Conditions

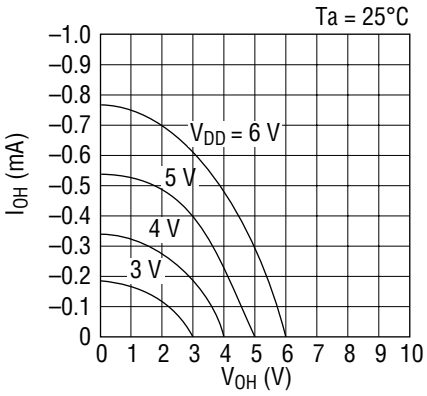


t_{SINH} : P0.1 (SR clock) INH period during LMSR INST.
(Note: P0.1 is used for clock of SR.)

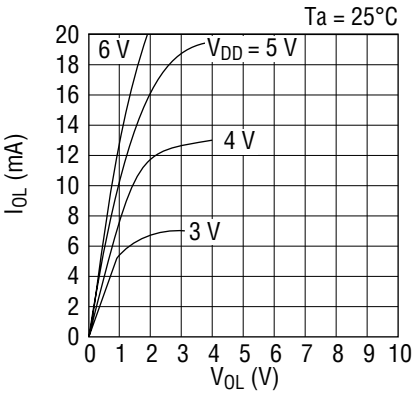
t_{IINH} : P2.0 (interrupt) INH period during RPB and RPBD INST.

Operating Characteristics

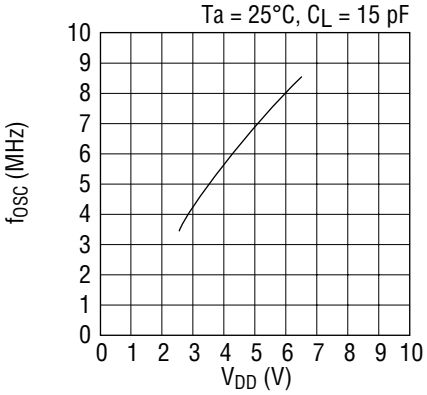
Typ. Current (I_{OH}) vs Voltage (V_{OH}) for High State Output



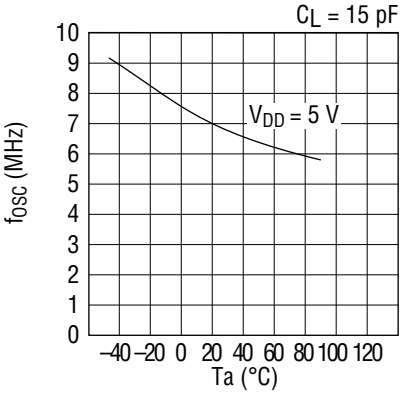
Typ. Current (I_{OL}) vs Voltage (V_{OL}) for Low State Output



Typ. Maximum Oscillator Frequnecy (f_{OSC}) vs Supply Voltage (V_{DD})

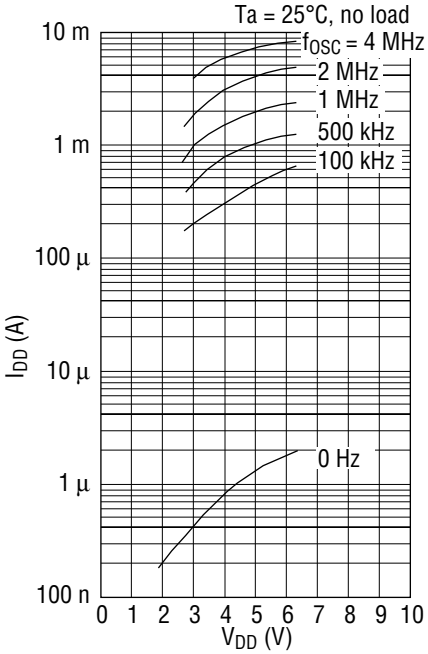


Typ. Maximum Oscillator Frequnecy (f_{OSC}) vs Temperature (Ta)



Operating Characteristics (continued)

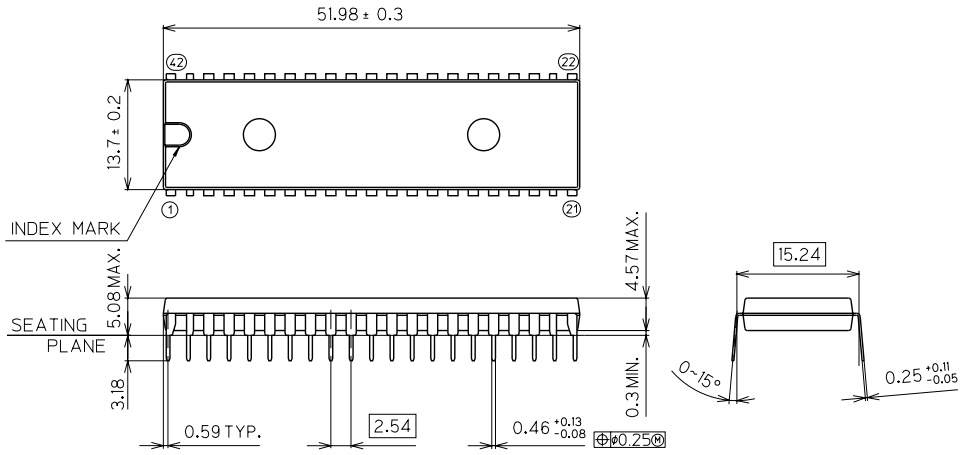
Typ. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})



PACKAGE DIMENSIONS

(Unit : mm)

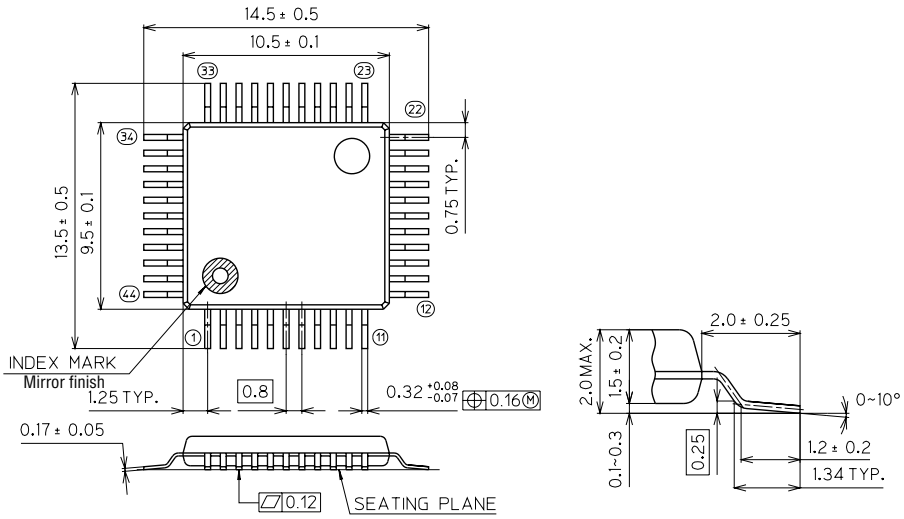
DIP42-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.20 TYP.

(Unit : mm)

QFP44-P-910-0.80-K



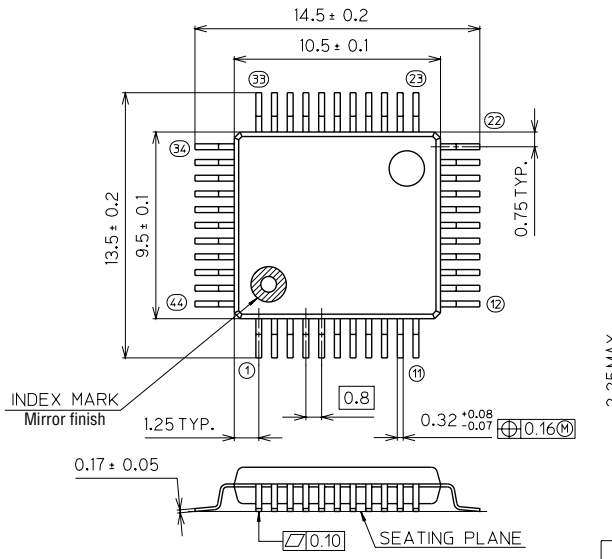
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.35 TYP.

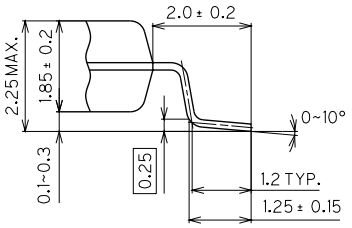
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

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