OKI Semiconductor

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MSC1164

20-Bit Grid/Anode Driver

GENERAL DESCRIPTION

The MSC1164 is a monolithic IC using the Bi-CMOS process technology for hybridizing CMOS and bipolar transistors on the same chip. The logic portion such as the input stage, shift register and latch is fabricated by CMOS and the output driver requiring a high withstand voltage is fabricated by bipolar transistors.

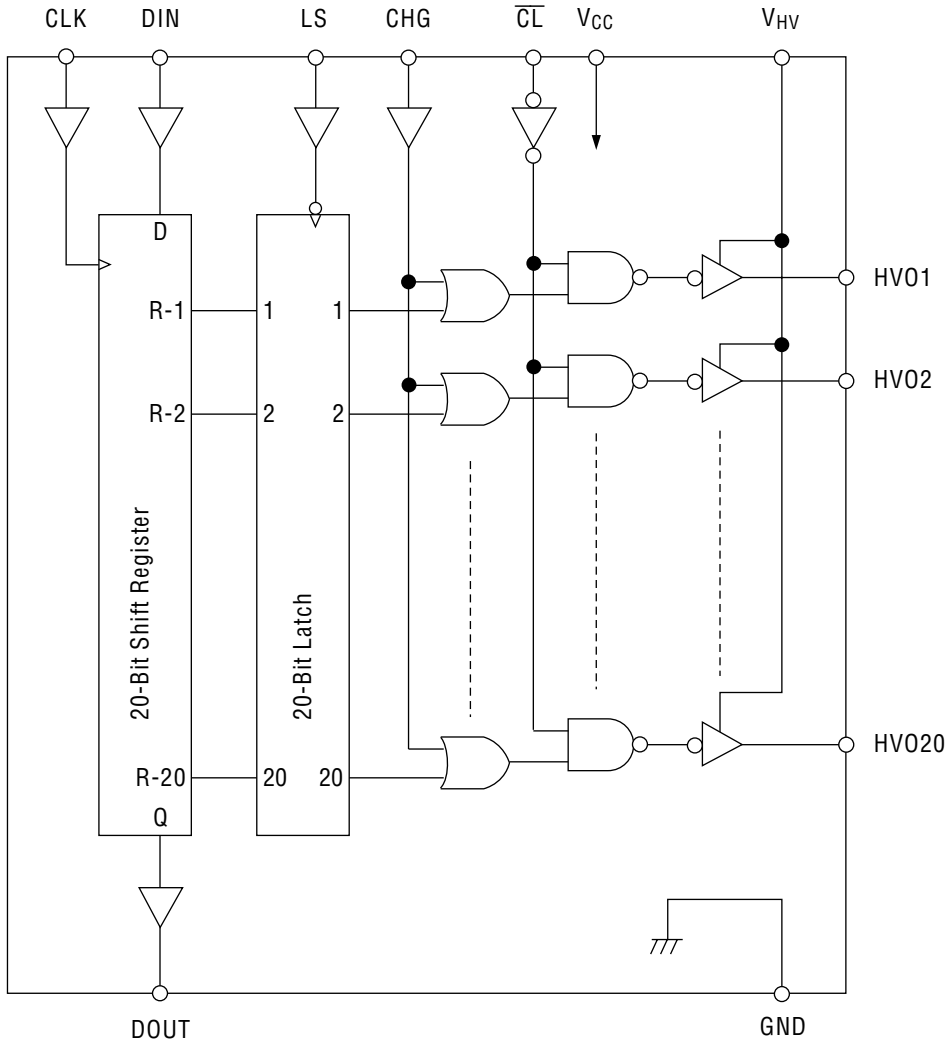
Since a 32-pin plastic SSOP package is used, the display unit size can be reduced.

FEATURES

The MSC1164 is designed as a VFD grid/anode driver with emitter-follower force output with 20-bit active pull-down and built-in 20-bit shift register and latch.

- Logic Supply Voltage (V_{CC}) : 5V
- Driver Supply Voltage (V_{HV}) : 65V
- Driver Output Current
  I_{OHVH1} :–40mA (Only one driver output: "H")
  I_{OHVH2} :–2mA (All driver outputs: "H")
  I_{OHVL} :2mA
- 20-bit output (with latch circuit)
- 20-bit shift register
- Clock frequency : 4MHz
- Package options:
  32-pin plastic SSOP (SSOP32-P-430-1.00-K) (Product name: MSC1164GS-K)

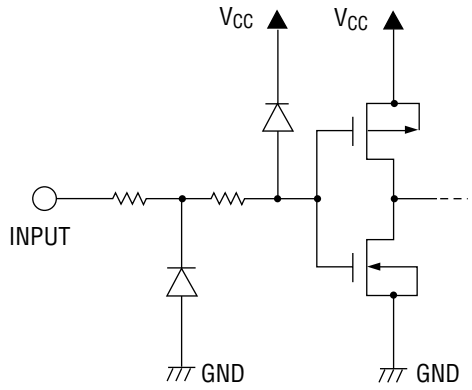
BLOCK DIAGRAM



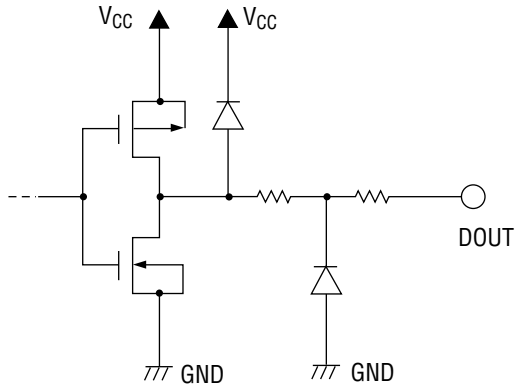
INPUT AND OUTPUT CONFIGURATION

Schematic Diagrams of Logic Portion Input and Output Circuits

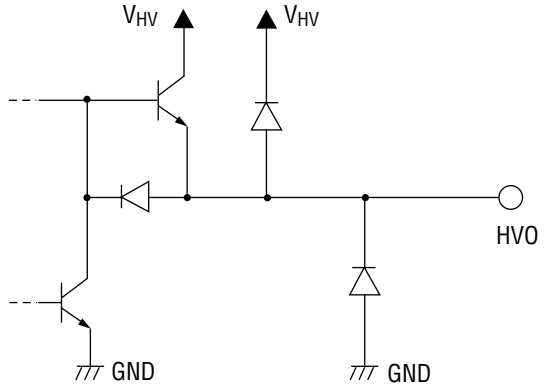
Input Pin



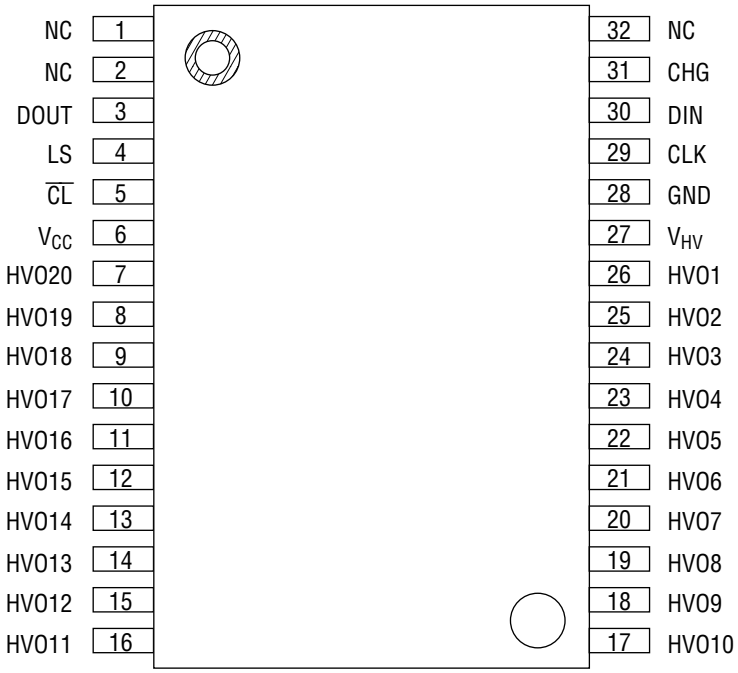
Output Pin



Schematic Diagram of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



NC: No-connection pin

32-Pin Plastic SSOP

PIN DESCRIPTION

Function	Pin	Symbol	Description
Driver Output	26 - 7	HVO1 - HVO20	Driver output pin, applicable to each bit of shift register.
Driver Power Supply	27	V_{HV}	Power supply pin for driver circuit.
Driver GND Logic GND	28	GND	GND pin for the driver circuit. GND pin for the logic circuit.
Clear Input	5	$\overline{CL}$	Clear input pin with pull-up resistor. Normally "H" level. In this condition, the driver outputs "H" or "L" according to the corresponding latch output level. Setting this pin to "L" enables the driver output to be fixed at "L" irrespective of latch output.
Latch Strobe Input	4	LS	Latch strobe input pin with neither pull-up nor pull-down resistor. When LS is "H", the output of the shift register becomes that of the latch circuit. When LS is "L", the latch circuit holds the contents of the shift register that are immediately before LS goes "L".
Data Input	30	DIN	Shift register input pin with neither pull-up nor pull-down resistor. Display data is input in synchronization with clock. (Positive Logic)
Logic Power Supply	6	V_{CC}	Power supply pin for logic (except driver). V_{CC} should be 4.5V to 5.5V.
Data Output	3	DOUT	Serial output pin for shift register.
Clock Input	29	CLK	Clock input pin. Data of shift register is shifted from one stage to the next at the rising edge of clock.
Test Input	31	CHG	Test input pin with a pull-down resistor. Normally "L". If $\overline{CL}$ = "H" in this condition, the driver outputs "H" or "L" according to the corresponding latch output.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Note
Logic Supply Voltage	V_{CC}	Applicable to logic supply voltage pin	–0.3 to +65	V	1
Driver Supply Voltage	V_{HV}	Applicable to driver supply voltage pin	V_{CC} to 70	V	1, 2
Input Voltage	V_{IN}	Applicable to all input pins	–0.3 to V_{CC} +0.3	V	1
Data Output Voltage	V_{OD}	Applicable to data output pin	–0.3 to V_{CC} +0.3	V	1
Driver Driving Frequency	f_{DRV}	Duty cycle 50% max	0 to 15	kHz	—
Power Dissipation	P_D	Ta ≤ 25°C	790	mW	—
Thermal Resistance of Package	R_{j-a}	—	158	°C/W	3
Storage Temperature	T_{STG}	—	–55 to +150	°C	—

Notes: 1) Maximum Supply Voltage with respect to GND
2) Stresses beyond "Absolute Maximum Rating" may cause permanent damage to the device.
3) Thermal resistance of the package (between junction and atmosphere)
The junction temperature (Tj) expressed by the equation below must not exceed 150˚C.
Tj=P × Rj–a+Ta (P: Maximum power consumption)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Max.	Unit
Logic Supply Voltage	V_{CC}	Applicable to logic supply voltage pin		4.5	5.5	V
Driver Supply Voltage	V_{HV}	Applicable to driver supply voltage pin		10	65	V
High Level Input Voltage	V_{IH}	Applicable to all input pins	V_{CC}=4.5V	3.6	—	V
			V_{CC}=5.5V	4.4	—	V
Low Level Input Voltage	V_{IL}	Applicable to all input pins	V_{CC}=4.5V	—	0.9	V
			V_{CC}=5.5V	—	1.1	V
High Level Driver Output Current	I_{OHVH1}	Only one driver output is High Other driver outputs are High		—	–40	mA
High Level Driver Output Current	I_{OHVH2}	All driver output pins are High		—	–2	mA
Low Level Driver Output Current	I_{OHVL}	Applicable to all driver output pins		—	2	mA
CLK Frequency	f_{ϕ}	See timing diagram		—	4	MHz
CLK Pulse Width	t_{WCLK}	See timing diagram		75	—	ns
Data in Setup Time	t_{DS}	See timing diagram		50	—	ns
Data in Hold Time	t_{DH}	See timing diagram		50	—	ns
LS Pulse Width	t_{WLS}	See timing diagram		80	—	ns
CLK-LS Delay Time	t_{DCL}	See timing diagram		50	—	ns
LS-CLK Delay Time	t_{DLC}	See timing diagram		0	—	ns
LS-CHG Delay Time	t_{DLCG}	See timing diagram		0	—	µs
LS-$\overline{CL}$ Delay Time	$t_{DL\overline{CL}}$	See timing diagram		0	—	µs
CHG Pulse Width	t_{WCHG}	See timing diagram		2	—	µs
$\overline{CL}$ Pulse Width	$t_{W\overline{CL}}$	See timing diagram		2	—	µs
Operating Temperature	T_{op}	—		–40	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC}=5V±10%, V_{HV}=10V to 65V, Ta=–40°C to +85°C)

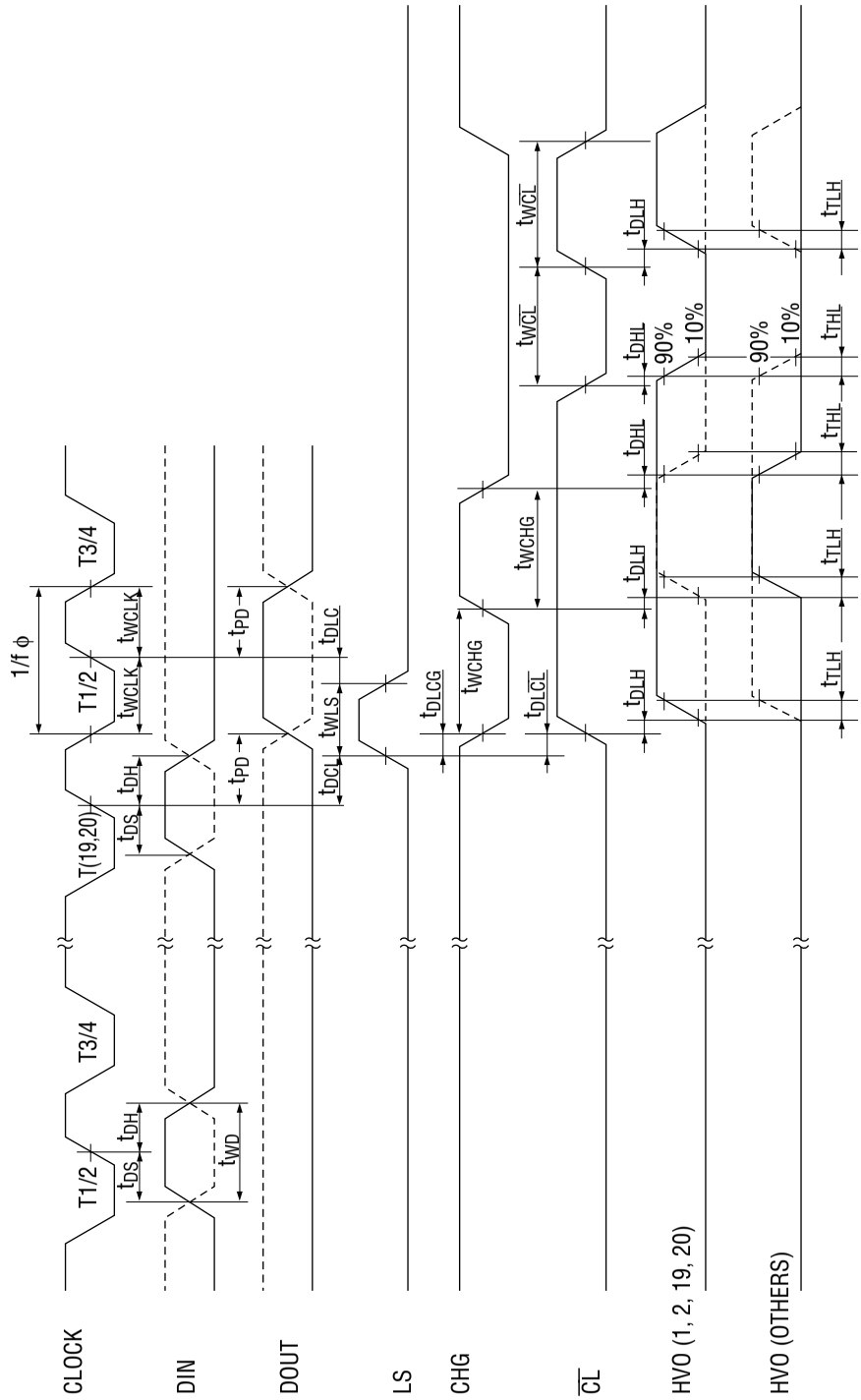
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Logic Supply Current	I_{CC1}	No load V_{CC}=5.5V	All input: Low	—	2.3	3.4	mA
	I_{CC2}		All input: High, All driver output: High, Ta=25°C	—	0.5	1.0	
Driver Supply Current	I_{HV1}	No load V_{CC}=5.5V	All driver output: Low	—	—	1	µA
	I_{HV2}		All driver output: High, Ta=25°C	—	1.3	2.0	mA
High Level Input Voltage	V_{IH}	—	V_{CC}=4.5V	3.15	—	—	V
			V_{CC}=5.5V	3.85	—	—	V
Low Level Input Voltage	V_{IL}	—	V_{CC}=4.5V	—	—	1.35	V
			V_{CC}=5.5V	—	—	1.65	V
Input Leakage Current	I_{IN}	Ta=25°C		—	—	±1	µA
Input Capacitance	C_{IN}	Ta=25°C		—	15	—	pF
High Level Data Output Voltage	V_{ODH1}	I_O=–20µA	V_{CC}=4.5V	4.2	—	—	V
			V_{CC}=5.5V	5.2	—	—	V
Low Level Data Output Voltage	V_{ODL1}	I_O=20µA	V_{CC}=4.5V	—	—	0.2	V
			V_{CC}=5.5V	—	—	0.2	V
High Level Data Output Voltage	V_{ODH2}	I_O=–0.1mA	V_{CC}=4.5V	3.5	—	—	V
			V_{CC}=5.5V	4.5	—	—	V
Low Level Data Output Voltage	V_{ODL2}	I_O=0.1mA	V_{CC}=4.5V	—	—	1.1	V
			V_{CC}=5.5V	—	—	1.1	V
High Level Driver Output Voltage	V_{OHVH}	I_{OHV}=–40mA		V_{HV}–4	—	—	V
Low Level Driver Output Voltage	V_{OHVL}	I_{OHV}=2mA		—	—	3.0	V

AC Characteristics

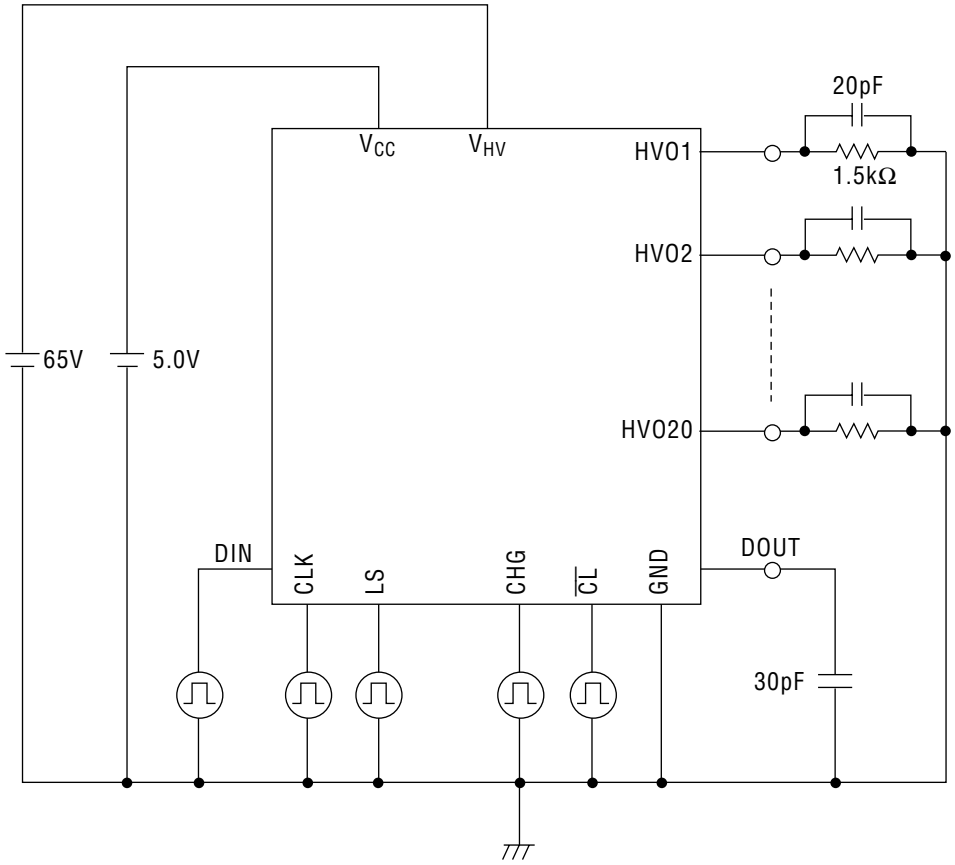
(V_{CC}=5V, V_{HV}=65V, Ta=25°C)

Parameter	Symbol	Remarks	Min.	Typ.	Max.	Unit
CLK-DOUT Delay Time	t_{PD}	See timing diagram and test circuit	—	100	150	ns
Delay Time Low to High	t_{DLH}	See timing diagram and test circuit	—	0.3	1	µs
Transit Time Low to High	t_{TLH}	See timing diagram and test circuit	—	2	5	µs
Delay Time High to Low	t_{DHL}	See timing diagram and test circuit	—	0.3	1	µs
Transit Time High to Low	t_{THL}	See timing diagram and test circuit	—	2	5	µs

TIMING DIAGRAM



Test circuit



FUNCTIONAL DESCRIPTION

Function Table

CLK	DIN	R-1	R-2	R-3	R-4	.....	R-20	DOUT
↑	H	H	R1n	R2n	R3n		R19n	R19n
↑	L	L	R1n	R2n	R3n		R19n	R19n

$\overline{CL}$	CHG	LS	R.X	HVO.X
L	X	X	X	L
H	H	X	X	H
H	L	H	H	H
H	L	H	L	L
H	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: Change

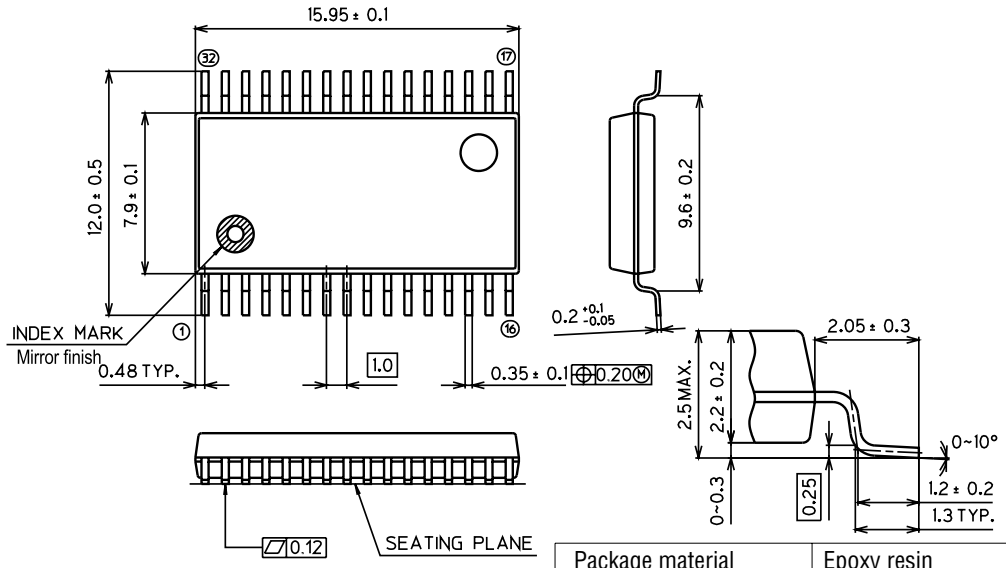
NOTES ON USE

1. The MSC1164 is designed as a grid/anode driver of VFD.
   The data applied to the data input pin is read into the shift register at the rising edge of the clock and shifted sequencially to the shift register synchronizing with the clock.
   The shift register output drives the output driver, passing through the latch and the NOR circuit.
   Setting the $\overline{CL}$ pin to "L" makes all driver outputs go into "L". This function can be used for setting display blanking.
2. The contents of the shift register are undefined after power is turned on.
   Therefore, two or more driver outputs may go into "H" at the same time after power-on. (If it happens, an overloading beyond the power dissipation limit may occur to cause a device break-down.)
   To avoid this, take the following procedure:
   1) Turn on the power of the logic portion while holding the $\overline{CL}$ pin to "L".
   2) Turn on the power of the driver portion.
   3) Apply a "L" level signal to the DIN pin and send clock pulses by the specified number of grids to reset ("L") the entire contents of the shift register.
   4) Initialize the driver outputs to "L".

PACKAGE DIMENSIONS

(Unit : mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.60 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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