OKI

ML63326
User's Manual

CMOS 4-bit microcontroller

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Preface

This manual describes the hardware of Oki's original CMOS 4-bit microcontroller ML63326.

Refer to the "nX-4/250 Core Instruction Manual" for details of the 4-bit CPU core nX-4/250 which is built in the ML63326.

The manuals related to the ML63326 are shown below.

- nX-4/250 Core Instruction Manual:
    Describes the base architecture and instruction set of nX-4/250 core.

- SASM63K User's Manual:
    Describes the structured assembler operation and assembler language specification.

- Dr. 63326 User's Manual:
    Describes the hardware of the emulator.

- DT63K Debugger User's Manual:
    Describes the debugger commands.

> This document is subject to change without notice.

Notation

Classification	Notation	Description
■ Numeric value	xxh, xxH	Represents a hexadecimal number.
	xxb	Represents a binary number.
■ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 2 nibbles = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
	KB	1 KB = 1 kilobyte = 1024 bytes
	MB	1 MB = 1 megabyte = 2^{20} bytes = 1,048,576 bytes
■ Symbol	⚠ Note:	Gives more information about mistakable items.
■ Terminology	"H" level	Indicates high side voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low side voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

■ Register description

Invalid bit	:	When read, a value of "1" is always obtained. Write operations are invalid.
R/W attribute	:	"R" indicates data can be read and "W" indicates data can be written.

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Overview

Chapter 1 Overview

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1.1 Overview

The ML63326 is a 4-bit microcontroller with built-in voice synthesis section and 1024-segment dot matrix LCD driver.

The ML63326 is ideal for applications such as game machines, toys, and clocks, that have LCD displays and synthesized voice outputs.

The ML63326 is a mask ROM product belonging to the M633xx series of the OLMS-63K family with Oki's original nX-4/250 CPU core.

The ML63326 contains a 24K-word program memory, a 1536-nibble data memory, one 4-bit input port, four 4-bit output ports, five 4-bit and one 2-bit I/O ports, a shift register, an LCD driver capable of driving a maximum of 1024 segments, and a voice synthesis section.

The voice synthesis section has a 12-bit D/A converter and a low-pass filter.

1.2 Features

The ML63326 has the following features.

- a. Extensive instruction set
  - 439 instructions
    Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, jump, conditional branch, call/return, control
- b. Wide variety of addressing modes
  - Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
  - Data memory bank internal direct addressing mode
- c. Processing speed
  - 2 clocks per machine cycle, with most instructions executed in 1 machine cycle
  - Minimum instruction execution time: 61 µs (@ 32.768 kHz system clock)
    0.976 µs (@ 2.048 MHz system clock)
- d. Clock generation circuit
  - Low-speed clock:
    Crystal oscillation or RC oscillation selected with mask option (30 kHz to 80 kHz)
  - High-speed clock:
    Crystal oscillation (4.096 MHz max.) or RC oscillation (2.048 MHz max.) selected with software (During the crystal oscillation mode, the device operates outputting the 1/2 frequency waveform of the source oscillation clock.)
- e. Program memory space
  - 24K words
  - The basic instruction length is 16 bits per word.
- f. Data memory space
  - 1536 nibbles
- g. External data memory space
  - 64 Kbytes (expandable by using I/O port)

h. Stack level

Call stack level	Register stack level
16	16

i. Ports
- Input ports:
  Selectable as input with pull-up resistor, input with pull-down resistor or high impedance input.
  Output ports:
  Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output.
- I/O ports:
  Selectable as input with pull-up resistor, input with pull-down resistor or high impedance input.
  Selectable as p-channel open drain output, n-channel open drain output, high impedance output or CMOS output.
- Can be interfaced to external devices having different power supplies.
- Number of ports:

Input port	Output ports	I/O ports
1 port $\times$ 4 bits	4 ports $\times$ 4 bits	5 ports $\times$ 4 bits
		1 port $\times$ 2 bits

j. Voice synthesis section
- Algorithm: 4-bit ADPCM method/non-linear 8-bit PCM method/ straight 8-bit PCM method
- Voice synthesis data area
  Internal ROM: 1-Mbit mask ROM (128 Kbytes)
  Stores voice data and character data, etc.
  External ROM: 4-Mbit ROM (512 Kbytes max.)
- Sampling frequencies
  With a source oscillator of 4.096 MHz: 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, and 16.0 kHz
- Built-in 12-bit D/A converter
- Built-in low-pass filter
- Built-in melody circuit (MELODY)
- Voice output duration
  voice output duration = voice ROM capacity/bit rate
  $\qquad\qquad\qquad\qquad$ = voice ROM capacity/(sampling frequency $\times$ bit length)

<Example>
When algorithm = 4-bit ADPCM method,
voice ROM capacity = 512 Kbits, and
sampling frequency = 4.0 kHz,
then the voice output duration = approx. 32.8 sec.

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k. Melody output (MELODY63K)
- Melody frequency: 529 Hz to 2979 Hz
- Tone length: 63 varieties
- Tempo: 15 varieties
- Melody data: Stored in program memory
- Buzzer driver signal output: 4 kHz

l. LCD driver
- Number of segments: 1024 segments max. (64 seg. $\times$ 16 com.)
- 1/1 to 1/16 duty
- 1/4 or 1/5 bias (internal regulator)
- Selectable as all-ON mode, all-OFF mode, power down mode, and normal display mode
- Adjustable contrast (16 levels @ V_{DD} = 2.4 V or more)

m. System reset function
- System reset by RESET pin
- System reset by power-on detection
- System reset by detection that low-speed clock has stopped oscillation

n. Battery check
- Function that detects battery low voltage
- Selection of judgment voltage by software (LD1 and LD0 bit settings of BLDCON)

LD1	LD0	Judgment voltage (V)	Remarks
0	0	—	Undefined
0	1	2.00 ±0.10	Ta = 25°C
1	0	2.20 ±0.10	Ta = 25°C
1	1	2.40 ±0.10	Ta = 25°C

o. Timers, counters
- 8-bit timer: 4 channels
  Selectable as auto-reload mode, capture mode, clock frequency measurement mode
- Watchdog timer: 1 channel
- 100 Hz timer: 1 channel
  1/100 sec. measurement possible
- 15-bit TBC: 1 channel
  1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz,128 Hz signals can be read

p. Shift register
- Shift clock: System clock $\times$1 or $\times$1/2, Timer 1 overflow, external clock
- Data length: 8 bits

q. Interrupt factors

External factors	Internal factors
4	13

r. Shipping products

Package	Product
• Chip (159 pads)	ML63326-xxx
• 176-pin flat package (176LQFP) LQFP176-P-2424-0.50-BK	ML63326-xxxTC

xxx indicates the ROM code number.

s. Operating temperature
- −20 to +70°C

t. Power supply voltage
- 2.0 to 5.5 V (30 kHz to 2.048 MHz operating frequency: internal clock)

1.3 Function List

Table 1-1 shows a list of the ML63326 functions. The solid black circles within the chart indicate that the product has the particular function.

Table 1-1 Function List

Function		Symbol	ML63326	Reference page
ROM (× 16 bits)		ROM	24576	→2-7
RAM (× 4 bits)		RAM	1536	→2-8
STACK RAM	Call	STACK	16 levels	→2-5
	Register		16 levels	→2-6
System reset generation circuit		RST	●	→3-2
Interrupt		INT326	●	→4-1
Clock generator circuit		OSC	●	→5-1
Time base counter		TBC	●	→6-1
Timers		TIMER	●	→7-1
100 Hz timer counter		100HzTC	●	→8-1
Watchdog timer		WDT	●	→9-1
Input port		INPUT PORT	1 port × 4 bits	—
	Port 0	P0	●	→10-2
Output port		OUTPUT PORT	4 ports × 4 bits	—
	Port 4	P4	●	→10-7
	Port 5	P5	●	
	Port 6	P6	●	
	Port 7	P7	●	
I/O port		I/O PORT	5 ports × 4 bits 1 port × 2 bits	—
	Port 8	P8	●	→10-15
	Port 9	P9	●	
	Port A	PA	●	
	Port B	PB	●	→10-24
	Port E	PE	●	→10-30
	Port F	PF	●	→10-35
External memory transfer		EXTMEM	●	→11-1
Melody driver		MELODY63K	●	→12-1
Voice synthesis		VOICE SYNTHESIS	●	→13-1
Shift register		SFT	●	→14-1
LCD driver	COM	LCD	16 lines	→15-1
	SEG		64 lines	
Display register (× 4 bits)		DSPR	256	→15-4
Bias generator		BIAS	●	→15-6
Battery low detect circuit		BLD	●	→16-1
Power supply circuit		POWER	●	→17-1

1.4 Block Diagram

Figure 1-1 is the block diagram of the ML63326.
Asterisks (*) indicate the secondary function of each port. Signal names enclosed by chain lines (.—.) indicate interface signals of the V_{DDI} power supply system.
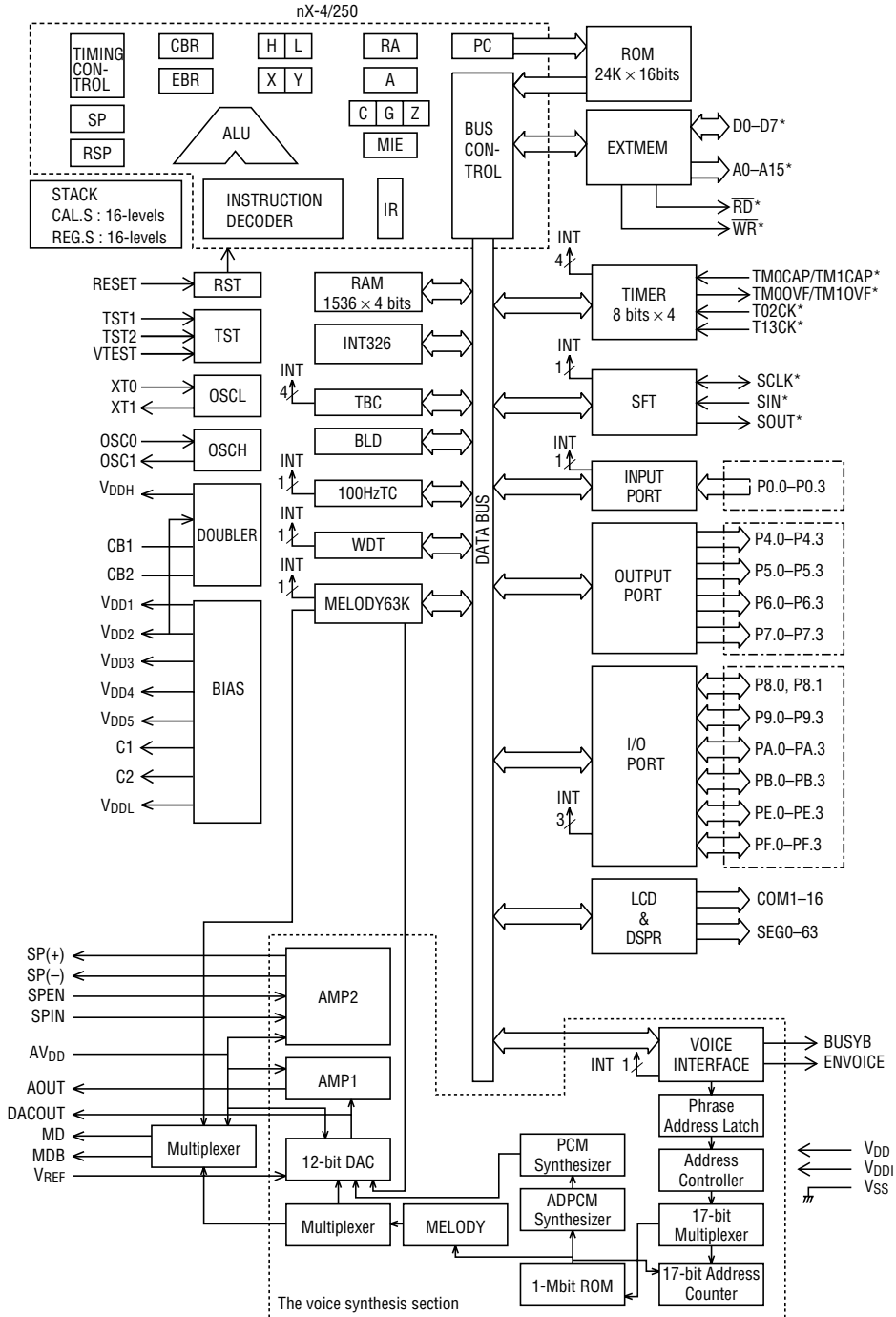
Figure 1-1 ML63326 Block Diagram

1.5 Pin Configuration

The ML63326 pin configuration, chip pin configuration, and pad coordinates are shown in Figures 1-2, 1-3, and Table 1-2, respectively.

NC (not connected) indicates an unused pin that is left unconnected (open).
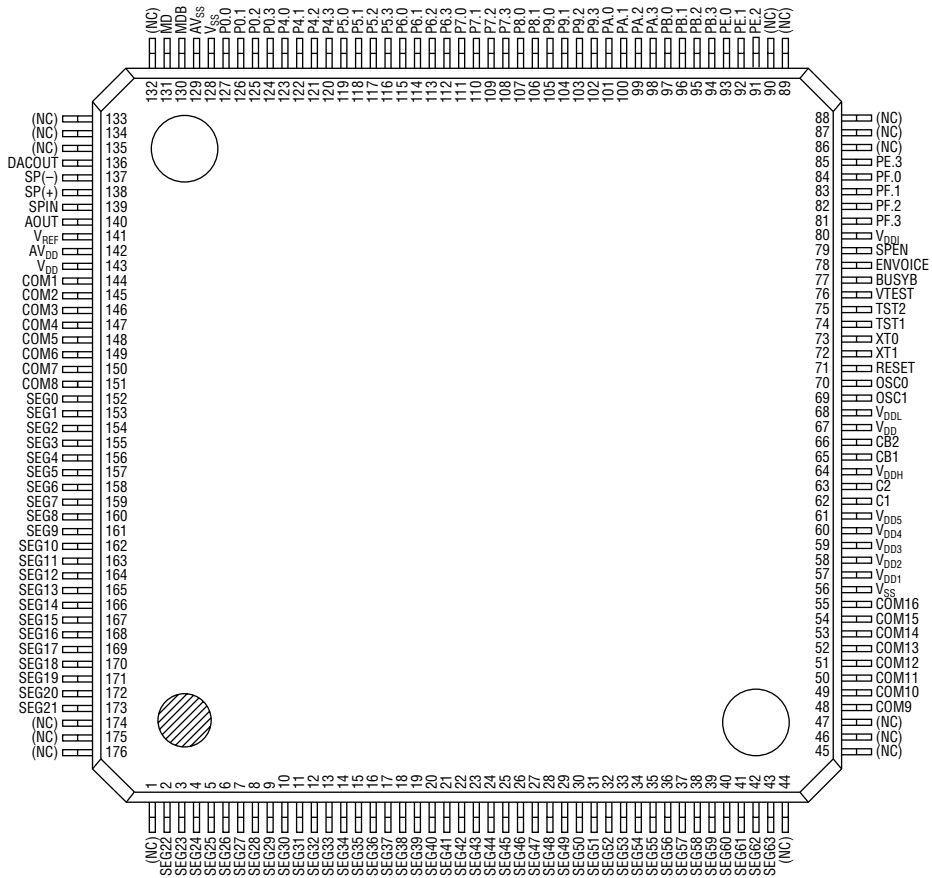
Figure 1-2 ML63326 176-Pin LQFP Pin Configuration (Top View)

Top pins (left to right, 118 to 81):
PE.3 118, PF.0 117, PF.1 116, PF.2 115, PF.3 114, V$_{DDI}$ 113, SPEN 112, ENVOICE 111, BUSYB 110, VTEST 109, TST2 108, TST1 107, XT0 106, XT1 105, RESET 104, OSC0 103, OSC1 102, V$_{DDL}$ 101, V$_{DD}$ 100, CB2 99, CB1 98, V$_{DDH}$ 97, C2 96, C1 95, V$_{DD5}$ 94, V$_{DD4}$ 93, V$_{DD3}$ 92, V$_{DD2}$ 91, V$_{DD1}$ 90, V$_{SS}$ 89, COM16 88, COM15 87, COM14 86, COM13 85, COM12 84, COM11 83, COM10 82, COM9 81

Left pins (top to bottom):
PE.2 119, PE.1 120, PE.0 121, PB.3 122, PB.2 123, PB.1 124, PB.0 125, PA.3 126, PA.2 127, PA.1 128, PA.0 129, P9.3 130, P9.2 131, P9.1 132, P9.0 133, P8.1 134, P8.0 135, P7.3 136, P7.2 137, P7.1 138, P7.0 139, P6.3 140, P6.2 141, P6.1 142, P6.0 143, P5.3 144, P5.2 145, P5.1 146, P5.0 147, P4.3 148, P4.2 149, P4.1 150, P4.0 151, P0.3 152, P0.2 153, P0.1 154, P0.0 155, V$_{SS}$ 156, AV$_{SS}$ 157, MDB 158, MD 159

Right pins (top to bottom):
80 SEG63, 79 SEG62, 78 SEG61, 77 SEG60, 76 SEG59, 75 SEG58, 74 SEG57, 73 SEG56, 72 SEG55, 71 SEG54, 70 SEG53, 69 SEG52, 68 SEG51, 67 SEG50, 66 SEG49, 65 SEG48, 64 SEG47, 63 SEG46, 62 SEG45, 61 SEG44, 60 SEG43, 59 SEG42, 58 SEG41, 57 SEG40, 56 SEG39, 55 SEG38, 54 SEG37, 53 SEG36, 52 SEG35, 51 SEG34, 50 SEG33, 49 SEG32, 48 SEG31, 47 SEG30, 46 SEG29, 45 SEG28, 44 SEG27, 43 SEG26, 42 SEG25, 41 SEG24, 40 SEG23, 39 SEG22

Bottom pins (left to right, 1 to 38):
DACOUT 1, SP(−) 2, SP(+) 3, SPIN 4, AOUT 5, V$_{REF}$ 6, AV$_{DD}$ 7, V$_{DD}$ 8, COM1 9, COM2 10, COM3 11, COM4 12, COM5 13, COM6 14, COM7 15, COM8 16, SEG0 17, SEG1 18, SEG2 19, SEG3 20, SEG4 21, SEG5 22, SEG6 23, SEG7 24, SEG8 25, SEG9 26, SEG10 27, SEG11 28, SEG12 29, SEG13 30, SEG14 31, SEG15 32, SEG16 33, SEG17 34, SEG18 35, SEG19 36, SEG20 37, SEG21 38

- Chip size   : 5.824 mm $\times$ 6.370 mm
- Chip thickness   : 350 μm (280 μm: available as required)
- Coordinate origin : center of chip
- Pad hole size   : 100 μm $\times$ 100 μm
- Pad size   : 110 μm $\times$ 110 μm
- Minimum pad pitch : 140 μm

⚠ Note: The chip substrate voltage is V$_{SS}$.

Figure 1-3 ML63326 Chip Pin Configuration (Top View)

Table 1-2 ML63326 Pad Coordinates

Center of chip: x = 0, y = 0

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Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
1	DACOUT	−2582	−3039	41	SEG24	2766	−2617
2	SP(−)	−2442	−3039	42	SEG25	2766	−2476
3	SP(+)	−2302	−3039	43	SEG26	2766	−2336
4	SPIN	−2162	−3039	44	SEG27	2766	−2196
5	AOUT	−2022	−3039	45	SEG28	2766	−2056
6	V_{REF}	−1882	−3039	46	SEG29	2766	−1916
7	AV_{DD}	−1742	−3039	47	SEG30	2766	−1776
8	V_{DD}	−1592	−3039	48	SEG31	2766	−1636
9	COM1	−1447	−3039	49	SEG32	2766	−1496
10	COM2	−1306	−3039	50	SEG33	2766	−1356
11	COM3	−1166	−3039	51	SEG34	2766	−1216
12	COM4	−1026	−3039	52	SEG35	2766	−1076
13	COM5	−886	−3039	53	SEG36	2766	−936
14	COM6	−746	−3039	54	SEG37	2766	−796
15	COM7	−606	−3039	55	SEG38	2766	−656
16	COM8	−466	−3039	56	SEG39	2766	−515
17	SEG0	−326	−3039	57	SEG40	2766	−375
18	SEG1	−186	−3039	58	SEG41	2766	−235
19	SEG2	−46	−3039	59	SEG42	2766	−95
20	SEG3	94	−3039	60	SEG43	2766	45
21	SEG4	234	−3039	61	SEG44	2766	185
22	SEG5	374	−3039	62	SEG45	2766	325
23	SEG6	514	−3039	63	SEG46	2766	465
24	SEG7	655	−3039	64	SEG47	2766	605
25	SEG8	795	−3039	65	SEG48	2766	745
26	SEG9	935	−3039	66	SEG49	2766	885
27	SEG10	1075	−3039	67	SEG50	2766	1025
28	SEG11	1215	−3039	68	SEG51	2766	1165
29	SEG12	1355	−3039	69	SEG52	2766	1306
30	SEG13	1495	−3039	70	SEG53	2766	1446
31	SEG14	1635	−3039	71	SEG54	2766	1586
32	SEG15	1775	−3039	72	SEG55	2766	1726
33	SEG16	1915	−3039	73	SEG56	2766	1866
34	SEG17	2055	−3039	74	SEG57	2766	2006
35	SEG18	2195	−3039	75	SEG58	2766	2146
36	SEG19	2335	−3039	76	SEG59	2766	2286
37	SEG20	2476	−3039	77	SEG60	2766	2426
38	SEG21	2616	−3039	78	SEG61	2766	2566
39	SEG22	2766	−2897	79	SEG62	2766	2706
40	SEG23	2766	−2757	80	SEG63	2766	2846

Table 1-2 ML63326 Pad Coordinates (continued)

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
81	COM9	2609	3039	121	PE.0	−2766	2492
82	COM10	2469	3039	122	PB.3	−2766	2352
83	COM11	2329	3039	123	PB.2	−2766	2212
84	COM12	2189	3039	124	PB.1	−2766	2072
85	COM13	2048	3039	125	PB.0	−2766	1932
86	COM14	1908	3039	126	PA.3	−2766	1792
87	COM15	1768	3039	127	PA.2	−2766	1652
88	COM16	1628	3039	128	PA.1	−2766	1512
89	V_{SS}	1488	3039	129	PA.0	−2766	1372
90	V_{DD1}	1348	3039	130	P9.3	−2766	1231
91	V_{DD2}	1208	3039	131	P9.2	−2766	1091
92	V_{DD3}	1068	3039	132	P9.1	−2766	951
93	V_{DD4}	928	3039	133	P9.0	−2766	811
94	V_{DD5}	788	3039	134	P8.1	−2766	671
95	C1	648	3039	135	P8.0	−2766	531
96	C2	508	3039	136	P7.3	−2766	391
97	V_{DDH}	368	3039	137	P7.2	−2766	251
98	CB1	227	3039	138	P7.1	−2766	111
99	CB2	87	3039	139	P7.0	−2766	−29
100	V_{DD}	−53	3039	140	P6.3	−2766	−169
101	V_{DDL}	−193	3039	141	P6.2	−2766	−309
102	OSC1	−333	3039	142	P6.1	−2766	−449
103	OSC0	−473	3039	143	P6.0	−2766	−590
104	RESET	−613	3039	144	P5.3	−2766	−730
105	XT1	−753	3039	145	P5.2	−2766	−870
106	XT0	−893	3039	146	P5.1	−2766	−1010
107	TST1	−1033	3039	147	P5.0	−2766	−1150
108	TST2	−1173	3039	148	P4.3	−2766	−1290
109	VTEST	−1313	3039	149	P4.2	−2766	−1430
110	BUSYB	−1453	3039	150	P4.1	−2766	−1570
111	ENVOICE	−1593	3039	151	P4.0	−2766	−1710
112	SPEN	−1734	3039	152	P0.3	−2766	−1850
113	V_{DDI}	−1874	3039	153	P0.2	−2766	−1990
114	PF.3	−2014	3039	154	P0.1	−2766	−2130
115	PF.2	−2154	3039	155	P0.0	−2766	−2270
116	PF.1	−2294	3039	156	V_{SS}	−2766	−2411
117	PF.0	−2434	3039	157	AV_{SS}	−2766	−2551
118	PE.3	−2574	3039	158	MDB	−2766	−2691
119	PE.2	−2766	2772	159	MD	−2766	−2831
120	PE.1	−2766	2632				

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1.6 Pin Descriptions

1.6.1 Descriptions of the Basic Pin Functions

The basic functions of the ML63326 pins are listed in Table 1-3. Use of a slash ("/") in a pin name indicates that the pin has a secondary function. Refer to section 1.6.2, "Descriptions of the Secondary Pin Functions."

In the I/O column, "—" indicates a power supply pin, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an input/output pin.

Table 1-3 Pin Description (Basic Functions)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Power Supply	V_{DD}	67, 143	8, 100	—	Postive power supply pin
	V_{SS}	56, 128	89, 156	—	Negative power supply pin
	V_{DD1}	57	90	—	Power supply pins for LCD bias (internally generated): Connect capacitors (0.1 μF) between these pins and V_{SS}.
	V_{DD2}	58	91		
	V_{DD3}	59	92		
	V_{DD4}	60	93		
	V_{DD5}	61	94		
	C1	62	95	—	Capacitor connection pins for LCD bias generation: Connect a capacitor (0.1 μF) between C1 and C2.
	C2	63	96		
	V_{DDI}	80	113	—	Positive power supply pin for external interface (Power supply for input, output and I/O ports)
	V_{DDL}	68	101	—	Positive power supply pin for internal logic (internally generated): Connect a capacitor (0.1 μF) between pin and V_{SS}.
	V_{DDH}	64	97	—	Power supply pin for the high-speed clock generator circuit: Connect a capacitor (1.0 μF) between pin and V_{SS}.
	CB1	65	98	—	Capacitor connection pins for V_{DDH} generation: Connect a capacitor (1.0 μF) between CB1 and CB2.
	CB2	66	99		
	V_{REF}	141	6	—	Pin for volume adjustment
	AV_{DD}	142	7	—	Positive power supply pin for analog circuits
	AV_{SS}	129	157	—	Negative power supply pin for analog circuits
Oscillator	XT0	73	106	I	Low-speed clock oscillation pins: Crystal oscillation or RC oscillation is selected by the mask option. If crystal oscillation is selected, connect a crystal between XT0 and XT1, and connect capacitor (C_G) between XT0 and V_{SS}. If RC oscillation is selected, connect external oscillation resistor (R_{OSL}) between XT0 and XT1.
	XT1	72	105	O	
	OSC0	70	103	I	High-speed clock oscillation pins: Connect a crystal and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OSH}) to these pins.
	OSC1	69	102	O	
Test	TST1	74	107	I	Input pins for testing: Pull-down resistors are built-in.
	TST2	75	108		
	VTEST	76	109		
Reset	RESET	71	104	I	Reset input pin: Setting this pin to a "H" level causes internal circuitry settings and values to be initialized. Next, if this pin is set to a "L" level, the execution of instructions will begin from address 0000H. A pull-down resistor is built-in.

Table 1-4 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
Melody	MD	131	159	O	Melody output pin (positive phase)
	MDB	130	158	O	Melody output pin (reversed phase)
Voice	DACOUT	136	1	O	Voice output pin (12-bit DAC output)
	AOUT	140	5	O	Voice output pin (amplifier output using DACOUT as input)
	SPIN	139	4	I	Amplifier input pin for driving a piezoelectric speaker
	SP(−)	137	2	O	Output pin for driving a piezoelectric speaker (negative side)
	SP(+)	138	3	O	Output pin for driving a piezoelectric speaker (positive side)
	SPEN	79	112	I	Enable signal of the amplifier for driving a piezoelectric speaker
	BUSYB	77	110	O	Voice synthesis section output monitor pin
	ENVOICE	78	111	O	Voice synthesis section enable monitor pin
Port	P0.0/INT5	127	155	I	4-bit input port: Each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input
	P0.1/INT5	126	154		
	P0.2/INT5	125	153		
	P0.3/INT5	124	152		
	P4.0/A0	123	151	O	4-bit output port: Each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P4.1/A1	122	150		
	P4.2/A2	121	149		
	P4.3/A3	120	148		
	P5.0/A4	119	147	O	
	P5.1/A5	118	146		
	P5.2/A6	117	145		
	P5.3/A7	116	144		
	P6.0/A8	115	143	O	
	P6.1/A9	114	142		
	P6.2/A10	113	141		
	P6.3/A11	112	140		
	P7.0/A12	111	139	O	
	P7.1/A13	110	138		
	P7.2/A14	109	137		
	P7.3/A15	108	136		
	P8.0/$\overline{\text{RD}}$	107	135	I/O	2-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P8.1/$\overline{\text{WR}}$	106	134		

1

Table 1-3 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function

Port	P9.0	105	133	I/O	4-bit I/O port:
					  During the input mode, each bit can be selected as the following.
					• Input with pull-up resistor
					• Input with pull-down resistor
					• High-impedance input
					  During the output mode, each bit can be selected as the following.
					• P-channel open drain output
					• N-channel open drain output
					• CMOS output
					• High-impedance output

	P9.1	104	132		
	P9.2	103	131		
	P9.3	102	130		

	PA.0	101	129	I/O	4-bit I/O port:
					  During the input mode, each bit can be selected as the following.
					• Input with pull-up resistor
					• Input with pull-down resistor
					• High-impedance input
					  During the output mode, each bit can be selected as the following.
					• P-channel open drain output
					• N-channel open drain output
					• CMOS output
					• High-impedance output

	PA.1	100	128		
	PA.2	99	127		
	PA.3	98	126		

	PB.0/INT0/
	TM0CAP/
	TM0OVF/
		97	125	I/O	4-bit I/O port:
					  During the input mode, each bit can be selected as the following.
					• Input with pull-up resistor
					• Input with pull-down resistor
					• High-impedance input
					  During the output mode, each bit can be selected as the following.
					• P-channel open drain output
					• N-channel open drain output
					• CMOS output
					• High-impedance output

	PB.1/INT0/ TM1CAP/ TM1OVF	96	124		
	PB.2/INT0/ T02CK	95	123		
	PB.3/INT0/ T13CK	94	122		

	PE.0/SIN	93	121	I/O	4-bit I/O port:
					  During the input mode, each bit can be selected as the following.
					• Input with pull-up resistor
					• Input with pull-down resistor
					• High-impedance input
					  During the output mode, each bit can be selected as the following.
					• P-channel open drain output
					• N-channel open drain output
					• CMOS output
					• High-impedance output

	PE.1/SOUT	92	120		
	PE.2/SCLK	91	119		
	PE.3/INT2	85	118		
	PF.0/INT3	84	117	I/O	
	PF.1/INT3	83	116		
	PF.2/INT3	82	115		
	PF.3/INT3	81	114		

Table 1-3 Pin Description (Basic Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
LCD	COM1	144	9	O	LCD common signal output pins (COM1 to COM16)
	COM2	145	10		
	COM3	146	11		
	COM4	147	12		
	COM5	148	13		
	COM6	149	14		
	COM7	150	15		
	COM8	151	16		
	COM9	48	81		
	COM10	49	82		
	COM11	50	83		
	COM12	51	84		
	COM13	52	85		
	COM14	53	86		
	COM15	54	87		
	COM16	55	88		
	SEG0	152	17	O	LCD segment signal output pins (SEG0 to SEG26)
	SEG1	153	18		
	SEG2	154	19		
	SEG3	155	20		
	SEG4	156	21		
	SEG5	157	22		
	SEG6	158	23		
	SEG7	159	24		
	SEG8	160	25		
	SEG9	161	26		
	SEG10	162	27		
	SEG11	163	28		
	SEG12	164	29		
	SEG13	165	30		
	SEG14	166	31		
	SEG15	167	32		
	SEG16	168	33		
	SEG17	169	34		
	SEG18	170	35		
	SEG19	171	36		
	SEG20	172	37		
	SEG21	173	38		
	SEG22	2	39		
	SEG23	3	40		
	SEG24	4	41		
	SEG25	5	42		
	SEG26	6	43		

Table 1-3 Pin Description (Basic Functions) (continued)

1

Classification	Pin name	Pin No.	Pad No.	I/O	Function
LCD	SEG27	7	44	O	LCD segment signal output pins (SEG27 to SEG63)
	SEG28	8	45		
	SEG29	9	46		
	SEG30	10	47		
	SEG31	11	48		
	SEG32	12	49		
	SEG33	13	50		
	SEG34	14	51		
	SEG35	15	52		
	SEG36	16	53		
	SEG37	17	54		
	SEG38	18	55		
	SEG39	19	56		
	SEG40	20	57		
	SEG41	21	58		
	SEG42	22	59		
	SEG43	23	60		
	SEG44	24	61		
	SEG45	25	62		
	SEG46	26	63		
	SEG47	27	64		
	SEG48	28	65		
	SEG49	29	66		
	SEG50	30	67		
	SEG51	31	68		
	SEG52	32	69		
	SEG53	33	70		
	SEG54	34	71		
	SEG55	35	72		
	SEG56	36	73		
	SEG57	37	74		
	SEG58	38	75		
	SEG59	39	76		
	SEG60	40	77		
	SEG61	41	78		
	SEG62	42	79		
	SEG63	43	80		

1.6.2 Descriptions of the Secondary Pin Functions

The secondary functions of the ML63326 pins are listed in Table 1-4.

Table 1-4 Pin Description (Secondary Functions)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
External interrupt	PB.0/INT0	97	125	I	External interrupt 0 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port B interrupt enable register (PBIE).
	PB.1/INT0	96	124		
	PB.2/INT0	95	123		
	PB.3/INT0	94	122		
	PE.3/INT2	85	118	I	External interrupt 2 input pin: Changes in the input signal level cause interrupts to be generated.
	PF.0/INT3	84	117	I	External interrupt 3 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port F interrupt enable register (PFIE).
	PF.1/INT3	83	116		
	PF.2/INT3	82	115		
	PF.3/INT3	81	114		
	P0.0/INT5	127	155	I	External interrupt 5 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port 0 interrupt enable register (P0IE).
	P0.1/INT5	126	154		
	P0.2/INT5	125	153		
	P0.3/INT5	124	152		
Capture	PB.0/ TM0CAP	97	125	I	Timer 0 capture trigger input pin
	PB.1/ TM1CAP	96	124	I	Timer 1 capture trigger input pin
Timer	PB.0/ TM0OVF	97	125	O	Timer 0 overflow flag output pin
	PB.1/ TM1OVF	96	124	O	Timer 1 overflow flag output pin
	PB.2/ T02CK	95	123	I	Timer 0, timer 2 external clock input pin
	PB.3/ T13CK	94	122	I	Timer 1, timer 3 external clock input pin
Shift register	PE.0/SIN	93	121	I	Shift register receive data input pin
	PE.1/SOUT	92	120	O	Shift register transmit data output pin
	PE.2/SCLK	91	119	I/O	Shift register clock input/output pin: This pin should be configured as the clock output when this device is used as the master processor, or as the clock input when used as a slave.

Table 1-4 Pin Description (Secondary Functions) (continued)

Classification	Pin name	Pin No.	Pad No.	I/O	Function
External memory	P4.0/A0	123	151	O	P4, P5, P6, P7 secondary functions: Address bus signals for external memory access.
	P4.1/A1	122	150		
	P4.2/A2	121	149		
	P4.3/A3	120	148		
	P5.0/A4	119	147		
	P5.1/A5	118	146		
	P5.2/A6	117	145		
	P5.3/A7	116	144		
	P6.0/A8	115	143		
	P6.1/A9	114	142		
	P6.2/A10	113	141		
	P6.3/A11	112	140		
	P7.0/A12	111	139		
	P7.1/A13	110	138		
	P7.2/A14	109	137		
	P7.3/A15	108	136		
	P9.0/D0	105	133	I/O	P9, PA secondary functions: Data bus signals for external memory access.
	P9.1/D1	104	132		
	P9.2/D2	103	131		
	P9.3/D3	102	130		
	PA.0/D4	101	129		
	PA.1/D5	100	128		
	PA.2/D6	99	127		
	PA.3/D7	98	126		
	P8.0/$\overline{\text{RD}}$	107	135	O	P8.0 secondary function: Read signal (negative logic) for external memory access.
	P8.1/$\overline{\text{WR}}$	106	134	O	P8.1 secondary function: Write signal (negative logic) for external memory access.

1.6.3 Unused Pin Processing

Table 1-5 lists the handling of unused pins.

Table 1-5 Unused Pin Handling

Pin	Recommended pin handling
OSC0, OSC1	Open
CB1, CB2	Open
V_{DDH}	Open
C1, C2	Open
V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5}	Open
TST1, TST2, VTEST	Open or V_{SS}
P0.0–P0.3	Open
P4.0–P4.3	Open
P5.0–P5.3	Open
P6.0–P6.3	Open
P7.0–P7.3	Open
P8.0, P8.1	Open
P9.0–P9.3	Open
PA.0–PA.3	Open
PB.0–PB.3	Open
PE.0–PE.3	Open
PF.0–PF3	Open
MD, MDB	Open
V_{REF}	Open
DACOUT, AOUT	Open
SPIN	V_{SS}
SPEN	Open
SP(−), SP(+)	Open
AV_{DD}	V_{DD}
AV_{SS}	V_{SS}
BUSYB, ENVOICE	Open
COM1–COM16	Open
SEG0–SEG63	Open

⚠ Notes:

1. If a pin set as a high impedance input is left unconnected, the supply current may become excessive. Therefore, it is recommended that unused input ports and input/output ports be set as inputs with either a pull-down or pull-up resistor.

2. When test pins TST1 and TST2 are left unconnected, malfunction may result if there is a large amount of external noise. Therefore, it is recommended to permanently connect TST1 and TST2 to V_{SS}.

3. Connect a capacitor (0.1 μF) between the V_{DD2} pin and the V_{SS} pin when the LCD drivers are not used.

1.7 Basic Timing

1.7.1 Basic Timing of CPU Operation

The system clock (CLK) uses the low-speed oscillation clock using the XT0 and XT1 pins or the high-speed oscillation clock using the OSC0 and OSC1 pins (1/2 frequency waveform when a crystal oscillator is used, no frequency division when an RC oscillator is used).The system clock signal is in phase with the signal from the XT1 pin or the OSC1 pin.

As shown in Figure 1-4, a single machine cycle is composed of two states, S1 and S2. One state is the interval from a falling edge of CLK to the falling edge of the next CLK.

Instructions are processed in machine cycle units and each instruction is executed in 1 to 3 machine cycles. Instructions are classified according to the number of machine cycles: 1 machine cycle instructions (M1), 2 machine cycle instructions (M1 + M2), and 3 machine cycle instructions (M1 + M2 + M3).

Most instructions are executed in 1 machine cycle.
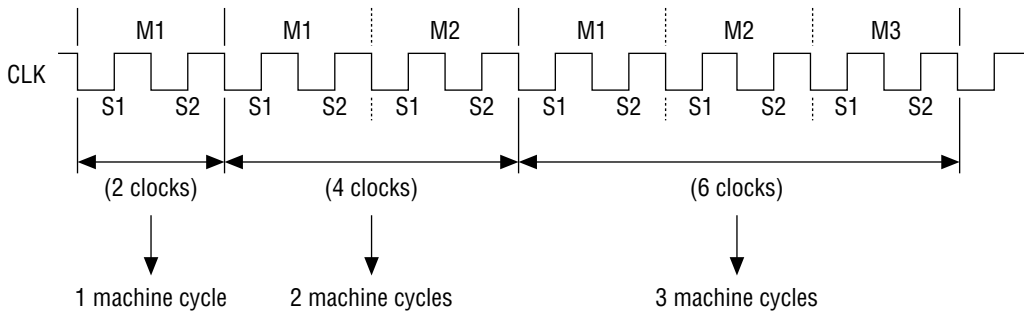
Figure 1-4 Clock Configuration of Each Machine Cycle

1.7.2 Port I/O Basic Timing

Figure 1-5 shows the basic I/O timing.

During the execution of an instruction that outputs data to a port, setting data (data A) is output at the rising edge of the clock in the S2 state during the machine cycle of that instruction.

During the execution of an instruction that inputs data from a port, data at the input pin (data B) is captured internally while the clock is at a "H" level in the S1 state during the machine cycle of that instruction. That data is transferred to the accumulator at the start of the next machine cycle.
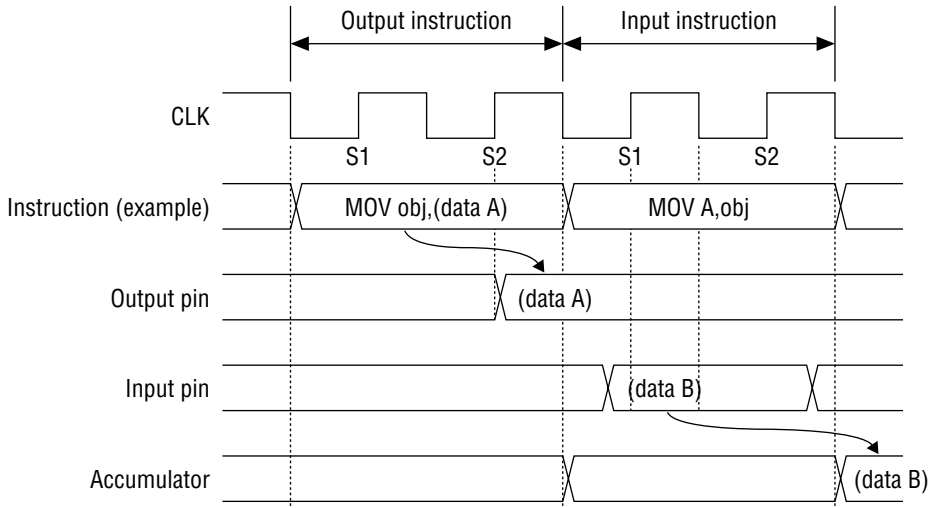
Figure 1-5 Port I/O Basic Timing

⚠ Note:

Regarding input signals

"0" will be captured in the internal register if a "L" level is input to the input pin even once (① of Figure 1-6) during the data capture interval.

"1" will be captured in the internal register only if a "H" level is maintained (② of Figure 1-6) throughout the data capture interval.

Therefore, if noise occurs in the input data, implement noise reduction measures with the program and peripheral devices.
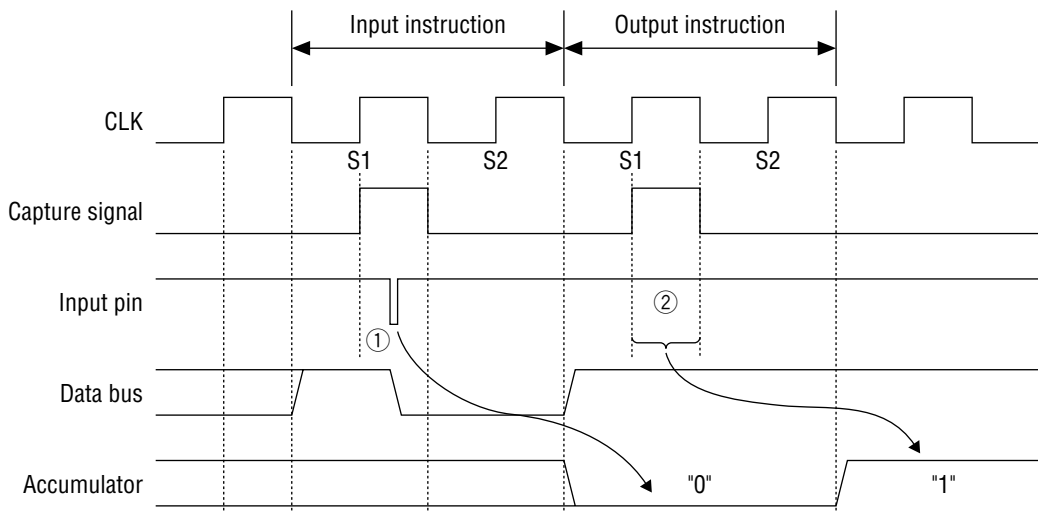
Figure 1-6 Input Data Example

1

1.7.3 Interrupt Basic Timing

Figure 1-7 shows the basic interrupt timing.

As shown in the figure, when an interrupt factor is generated, the interrupt factor is sampled at the falling edge of CLK and an interrupt request (IRQ) is set at the first half of S1.

When an interrupt condition is established and the CPU receives an interrupt, the interrupt routine will start beginning from the next machine cycle.
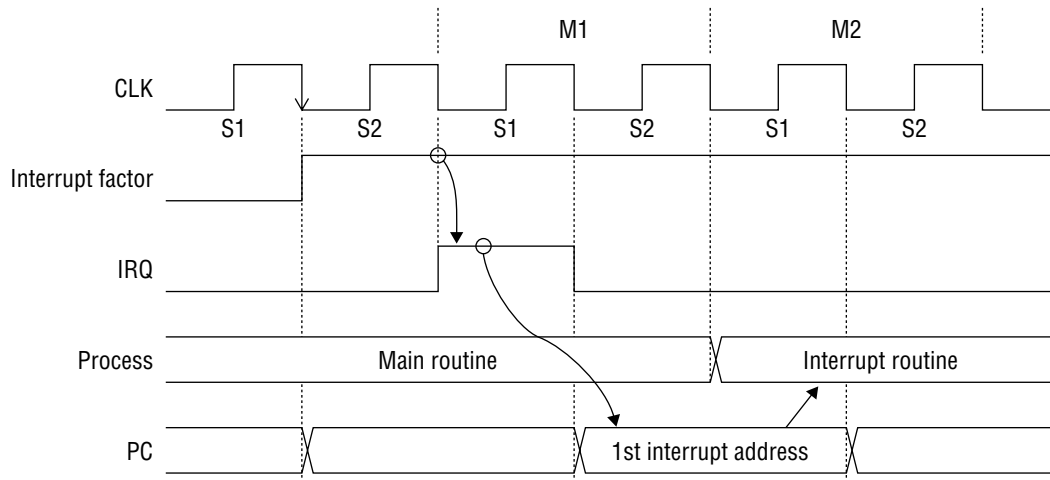
Figure 1-7 Interrupt Basic Timing

Chapter 2

CPU and Memory Spaces

Chapter 2 CPU and Memory Spaces

2.1 Overview

The ML63326 is equipped with an Oki's original CPU core nX-4/250.

The instruction set of the nX-4/250 core consists of 439 types of instructions.

The memory space consists of a 16-bit wide program memory space, a 4-bit wide data memory space, and an 8-bit wide memory space for storing voice synthesis and character data. Further, it is possible to add an 8-bit wide memory space for voice synthesis and for storing character data. A stack for saving the program counter during a subroutine call or interrupt (call stack) and a stack for saving registers during a PUSH instruction (register stack) are provided separately from the memory space.

The program memory space is used for program data, ROM table data and melody note data.

In the data memory space, special function registers (SFRs) are located in BANK 0, the LCD display register (DSPR) in BANK 1, and data RAM in BANKS 2 to 7.

2.2 Registers

The nX-4/250 core processes data mainly with the accumulator and register set.

The register set is a programming model consisting of the HL and XY registers that store data memory addresses, the current bank register (CBR), the extra bank register (EBR), the RA register that stores program memory addresses, registers that control program flow, and registers that control flags and memory.

2.2.1 Accumulator (A)

The accumulator (A) is the central register for various arithmetic operations.

At system reset, the accumulator is initialized to "0". When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the accumulator on the register stack. The accumulator can be restored with a "POP HL" instruction.

```
  3  2  1  0
 ┌──────────┐
 │    A     │
 └──────────┘
 Accumulator
```
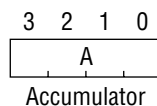
2.2.2 Flag Register

The flag register consists of 3 flags: the carry flag (C), the zero flag (Z) and the G flag (G). When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the flag register on the register stack. The flag register can be restored with a "POP HL" instruction.

```
 ┌───┬───┬───┐
 │ G │ C │ Z │
 └───┴───┴───┘
  Flag register
```
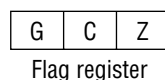
2.2.2.1 Carry Flag (C)

The carry flag (C) is a 1-bit flag that is loaded with a carry during addition or a borrow during subtraction. At system reset, the carry flag is initialized to "0".

2.2.2.2 Zero Flag (Z)

The zero flag (Z) is a 1-bit flag that is set to "1" when the contents of the accumulator (A) are loaded with "0H". The zero flag is set to "0" when the contents of the accumulator (A) are loaded with a value other than "0H". However, the XCH instruction does not change the zero flag. At system reset, the zero flag is initialized to "0".

2.2.2.3 G Flag (G)

The G flag (G) changes to "1" when the HL, XY or RA registers overflow as the result of execution of a post-increment register indirect addressing instruction or as the result of an increment instruction for the HL, XY or RA registers. At system reset, the G flag is initialized to "0".

2.2.3 Master Interrupt Enable Flag (MIE)

MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt. MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute a RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.

	bit 3	bit 2	bit 1	bit 0
MIEF (0FFH) (R)	—	—	—	MIE

Master Interrupt Enable Flag
0: Interrupts disabled (initial value)
1: Interrupts enabled
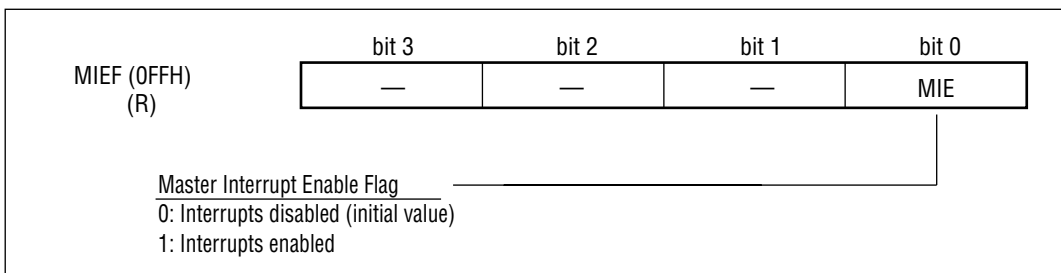
⚠ Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

2.2.4 Current Bank Register (CBR), Extra Bank Register (EBR), HL Register (HL), XY Register (XY)

The CBR, EBR, HL, and XY registers are used for indirect addressing of data memory.

2

The CBR and EBR registers indicate the data memory bank. The HL and XY registers indicate addresses in the bank. CBR is also used in combination with 8-bit data in the instruction code for direct addressing within the current bank.

Figure 2-1 shows the various register combinations.

CBR	+	H	L
CBR	+	X	Y
EBR	+	H	L
EBR	+	X	Y
CBR	+	Instruction code 8-bit data	
A11–A8		A7–A4	A3–A0
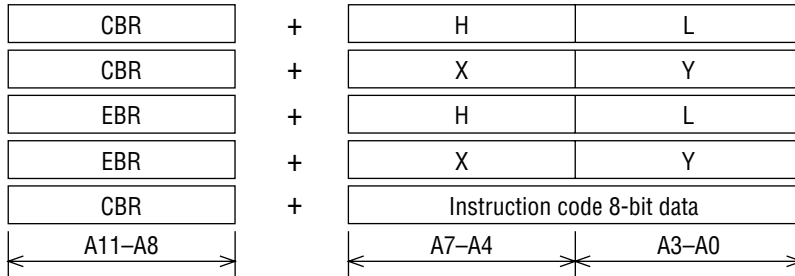
Figure 2-1 Various Register Combinations

A11 to A0 in Figure 2-1 indicate data memory addresses (4K nibbles max.).

At system reset, the CBR, EBR, HL, and XY registers are initialized to "0".

When an interrupt occurs, a "PUSH HL" or "PUSH XY" instruction can be used if necessary to save the CBR, EBR, HL, and XY registers on the register stack. These registers can be restored with a "POP HL" or "POP XY" instruction.

The CBR, EBR, HL, and XY registers are assigned to special function register (SFR) addresses 0F9H to 0FEH.

		bit 3	bit 2	bit 1	bit 0
EBR	(0FEH) (R/W)	e_3	e_2	e_1	e_0
CBR	(0FDH) (R/W)	c_3	c_2	c_1	c_0
H	(0FCH) (R/W)	h_3	h_2	h_1	h_0
L	(0FBH) (R/W)	l_3	l_2	l_1	l_0
X	(0FAH) (R/W)	x_3	x_2	x_1	x_0
Y	(0F9H) (R/W)	y_3	y_2	y_1	y_0

2.2.5 Program Counter (PC)

The program counter (PC) is a counter with 16 valid bits that specifies the program memory space.

2.2.6 RA Registers (RA3, RA2, RA1, RA0)

The RA registers are used for indirect program memory addressing (ROM table reference instructions).

Figure 2-2 shows the address configuration of the RA registers.

RA3	RA2	RA1	RA0
A15–A12	A11–A8	A7–A4	A3–A0

Figure 2-2 Address Configuration of RA3 to RA0 Registers

Within the A15 to A0 of Figure 2-2, A14 to A0 indicate program memory addresses (32K words max.).

RA3 to RA0 are assigned to special function register (SFR) addresses 0F2H to 0F5H.

		bit 3	bit 2	bit 1	bit 0
RA3	(0F5H) (R/W)	a_{15}	a_{14}	a_{13}	a_{12}
RA2	(0F4H) (R/W)	a_{11}	a_{10}	a_9	a_8
RA1	(0F3H) (R/W)	a_7	a_6	a_5	a_4
RA0	(0F2H) (R/W)	a_3	a_2	a_1	a_0

At system reset, RA3 to RA0 are initialized to "0".

⚠ Note:

When executing a ROM table reference instruction that uses RA registers, do not use addresses located in the SFR area to transfer ROM table data to RA registers, otherwise indirect addressing of program memory will not operate properly.

2.2.7 Stack Pointer (SP) and Call Stack

The stack pointer (SP) is a pointer that indicates the call stack address where the program counter is saved when a subroutine call or interrupt occurs.

The SP is a 4-bit up/down counter that is incremented during stack saves and is decremented during stack restores.

The call stack has 16 levels from address 0H to address 0FH. Because the hardware requires 1 level of the call stack during program execution, only 15 levels can be used for stack saves. The contents of the call stack cannot be read or written by the program.

Figure 2-3 shows the relation between SP and the call stack.
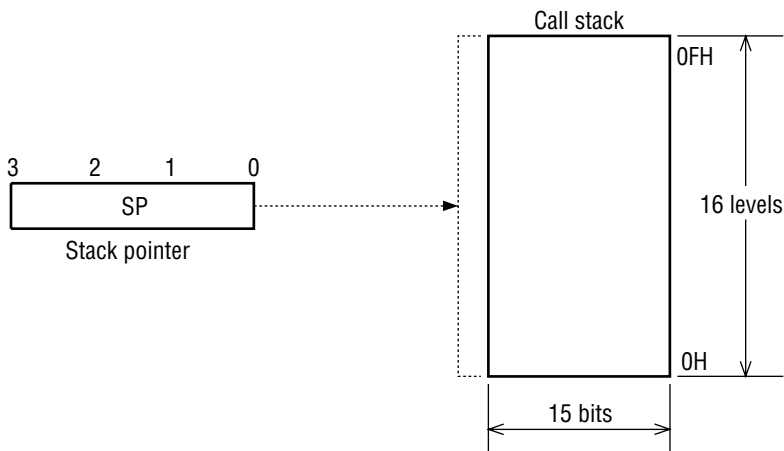
Figure 2-3 Relation Between SP and Call Stack

SP is assigned to special function register (SFR) address 0F7H.

	bit 3	bit 2	bit 1	bit 0
SP (0F7H) (R)	SP3	SP2	SP1	SP0
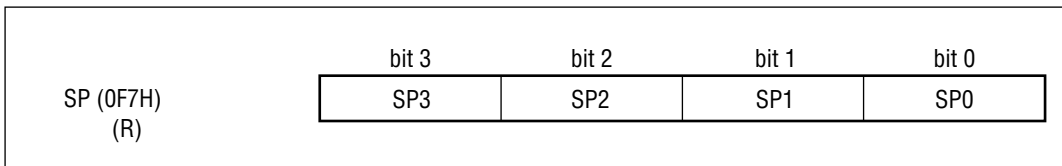
At system reset, SP is initialized to "0" and points to address "0H" of the call stack. SP is a read-only register and writes are invalid.

2.2.8 Register Stack Pointer (RSP) and Register Stack

The register stack pointer (RSP) is a pointer that indicates the register stack address for saving various registers.

RSP is a 4-bit up/down counter that is incremented during stack saves (execution of PUSH instructions) and is decremented during stack restores (execution of POP instructions).

The register stack has 16 levels from address 0H to address 0FH. The contents of the register stack cannot be read or written by the program.

Figure 2-4 shows the relation between RSP and the register stack.
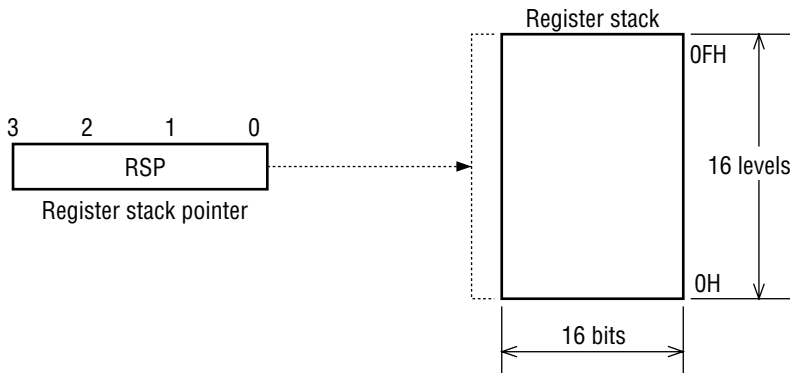
Figure 2-4 Relation Between RSP and Register Stack

The various registers shown in Figure 2-5 are saved onto and restored from the register stack by PUSH and POP instructions.

"PUSH HL" and "POP HL" instruction execution

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	G	C	Z		A				H				L		

Register stack

"PUSH XY" and "POP XY" instruction execution

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EBR				CBR				X				Y		
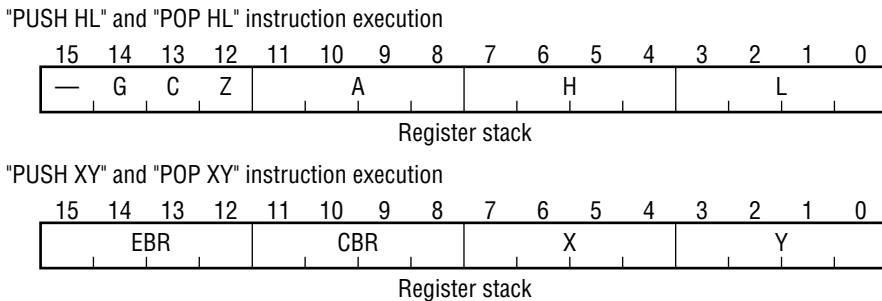
Register stack

Figure 2-5 Register Save/Restore by Execution of PUSH/POP Instructions

RSP is assigned to special function register (SFR) address 0F6H.

	bit 3	bit 2	bit 1	bit 0
RSP (0F6H) (R/W)	rsp3	rsp2	rsp1	rsp0
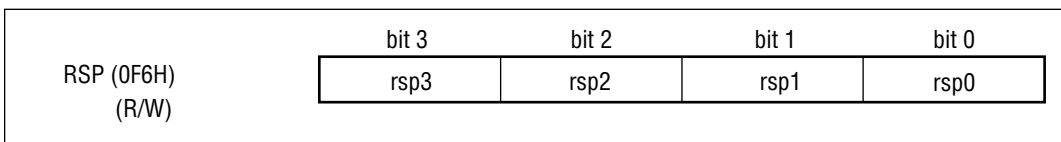
At system reset, RSP is initialized to "0" and points to address "0H" of the register stack.

2.3 Memory Spaces

2.3.1 Program Memory Space

The program memory space is the read-only memory that stores program data.

The program memory space has a data length of 16 bits and extends from address 0000H to address 5FFFH in the ML63326.

In addition to program data, the program memory can also store ROM table data and the melody data. Figure 2-6 shows the configuration of the program memory space.

```
5FFFH ┌──────────────┐   ↕ 32 words
5FDFH │ Test data area│
      ├──────────────┤   ↑
   ≈  │              │ ≈
      │ Program data  │
      │     or        │   24,544 words
      │ ROM table data│
      │     or        │
      │  Melody data  │
0037H ├- - - - - - - -┤   ↑
      │              │
      │ Interrupt area│   40 words
      │              │
0010H ├- - - - - - - -┤   ↓
      │              │
0000H └──────────────┘   ↓
```
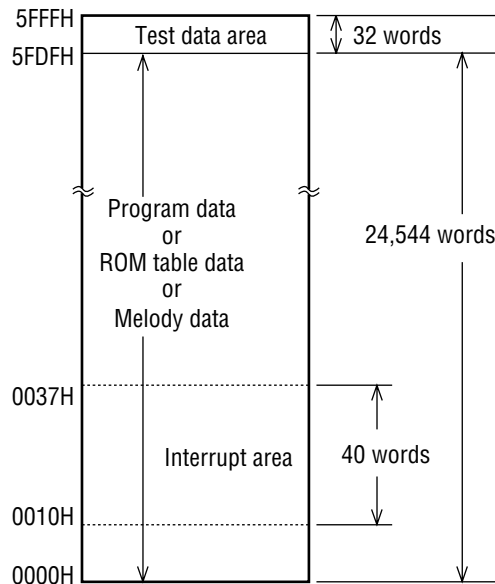
Figure 2-6 Program Memory Space Configuration

After system reset, instruction execution begins at address 0000H. The interrupt area from address 0010H to address 0037H contains starting addresses of the interrupt processing routines that are executed when interrupts are generated. (Refer to Chapter 4, "Interrupt.")

ROM table data is transferred to data memory by ROM table reference instructions.

The melody data defines the tone, tone length, and end tone used in the melody circuit (MELODY63K) of the ML63326. After an MSA instruction specifies the starting address, the melody data is automatically transferred to the melody circuit when a melody data interrupt occurs. (Refer to Chapter 12, "Melody Driver.")

Because the test data area contains program data for testing, it cannot be used as a program data area.

2.3.2 Data Memory Space

The data memory space contains data RAM and special function registers (SFRs).

The data memory consists of 8 banks. One bank unit is 256 nibbles. BANK 0 is allocated as a SFR area, BANK 1 as the LCD display register, and BANK 2 and the following BANKS are data RAM.

Figure 2-7 shows the configuration of the data memory space.

```
7FFH ┌─────────────────┐          ▲
      │                 │          │
      │     BANK7       │          │
      │                 │          │
700H  ├╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌┤          │
6FFH  │                 │          │
      │     BANK6       │          │
      │                 │          │
600H  ├╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌┤          │
5FFH  │                 │          │
      │     BANK5       │          │
      │                 │          │
500H  ├╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌┤   Data RAM area
4FFH  │                 │   (1536 nibbles)
      │     BANK4       │          │
      │                 │          │
400H  ├╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌┤          │
3FFH  │                 │          │
      │     BANK3       │          │
      │                 │          │
300H  ├╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌╌┤          │
2FFH  │                 │          │
      │     BANK2       │          │
      │                 │          │
200H  ├─────────────────┤          ▼
1FFH  │                 │          ▲
      │     BANK1       │  Display register
      │                 │   (256 nibbles)
100H  ├─────────────────┤          ▼
0FFH  │                 │          ▲
      │     BANK0       │      SFR area
      │                 │   (256 nibbles)
000H  └─────────────────┘          ▼
```
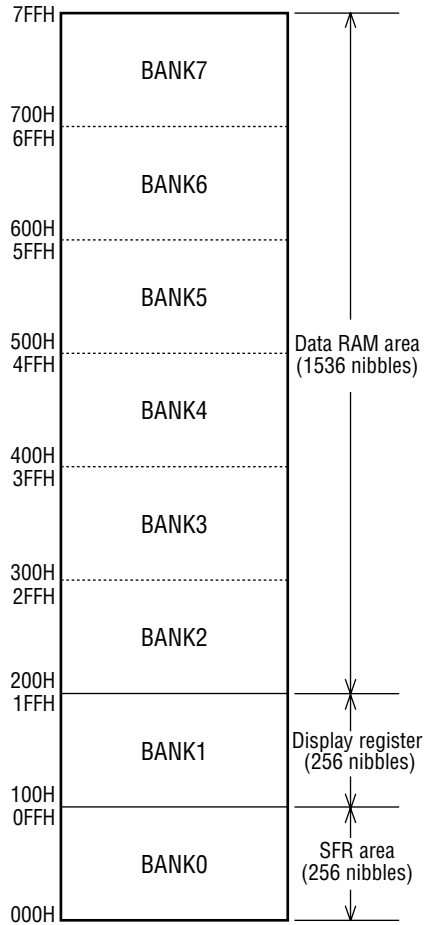
Figure 2-7 Data Memory Space Configuration

2.3.3 Memory Space for Voice Synthesis and Character Data

The memory space for voice synthesis and character data is configured by a mask ROM that stores the voice data necessary for the built-in voice synthesis function and the character data used for the LCD display.

2
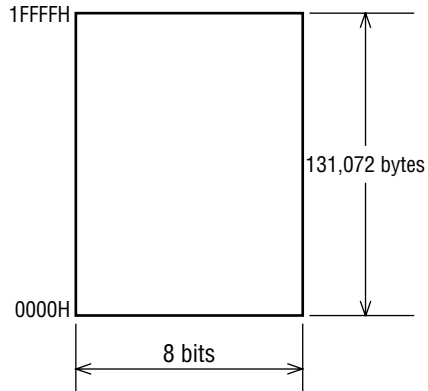
Figure 2-8 Memory Space Configuration

2.3.4 External Memory Space

The external memory space is one for storing the voice data necessary for the built-in voice synthesis function and the character data used for the LCD display, and is accessed via a port.

The external memory space configuration is shown in Figure 2-9.
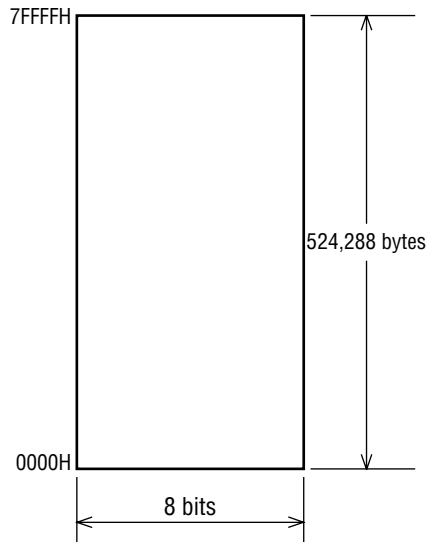
Figure 2-9 External Memory Space Configuration

CPU Control Functions

Chapter 3 CPU Control Functions

3.1 Overview

Operating states, including system reset, are classified as follows.

- Normal operation mode
- System reset mode
- Halt mode

Figure 3-1 shows the CPU operating state transition diagram.
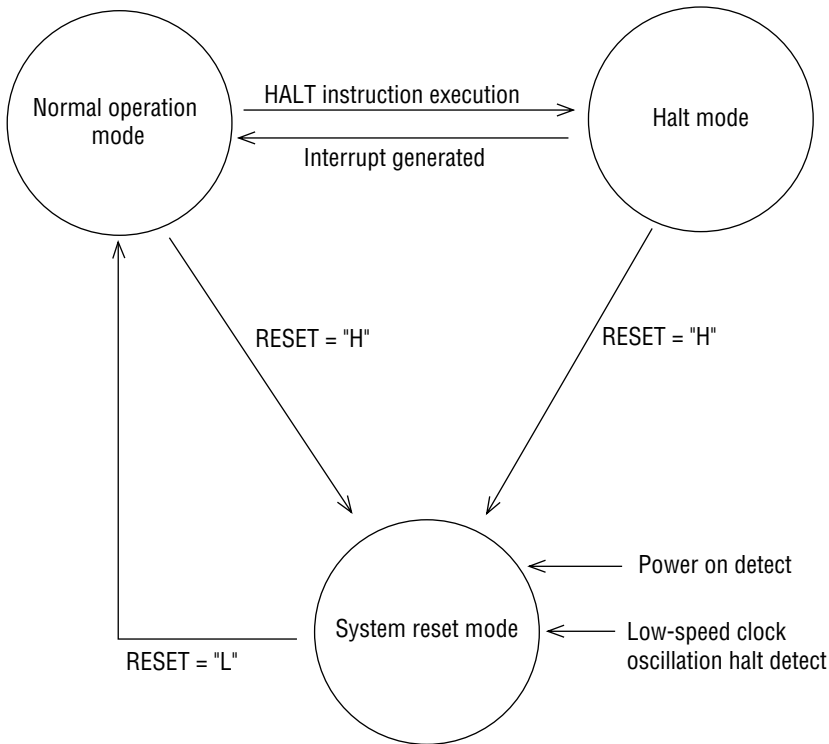
Figure 3-1 Operating State Transition Diagram

The normal operation mode is the state in which the CPU executes instructions sequentially.

The system reset mode begins when a reset input causes the CPU to begin system reset processing where registers and pins are initialized. The CPU remains in this state until instruction execution begins. After system reset processing, instruction execution begins from address 0000H.

The halt mode is the state in which the CPU is halted (instruction execution suspended) but internal peripheral functions continue to operate. During the halt mode, the PC is not incremented. Even upon entering the halt mode, port and peripheral functions will not change. Transfer to the halt mode is accomplished by executing a "HALT" instruction.

3.2 System Reset Mode (RST)

3.2.1 Transfer to and State of System Reset Mode

The following three factors cause a transfer to the system reset mode.

- Setting the RESET pin to a "H" level (for 1 ms or more)
- Detection of power on
- Detection that low-speed clock oscillation is halted

The following operations are performed in the system reset mode.

(1) CPU is initialized.

(2) Backup flag changes to "1" and backup circuit changes to ON state.

(3) Bias reference voltage supply (VR) is energized.

(4) All LCD driver outputs are turned OFF and the outputs change to the V_{SS} level.

(5) All special function registers (SFRs) are initialized. However, data RAM and display registers are not initialized.

After system reset processing, instruction execution begins from address 0000H.

Figures 3-2 and 3-3 show the system reset generator circuit and signals when a system reset is generated.
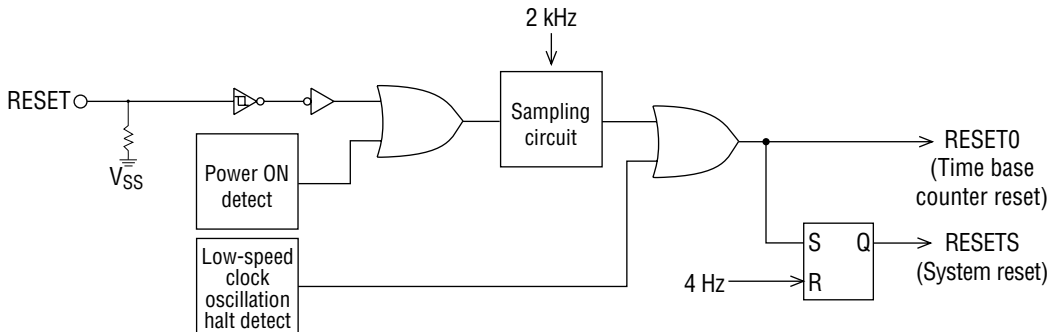
Figure 3-2 System Reset Generator Circuit
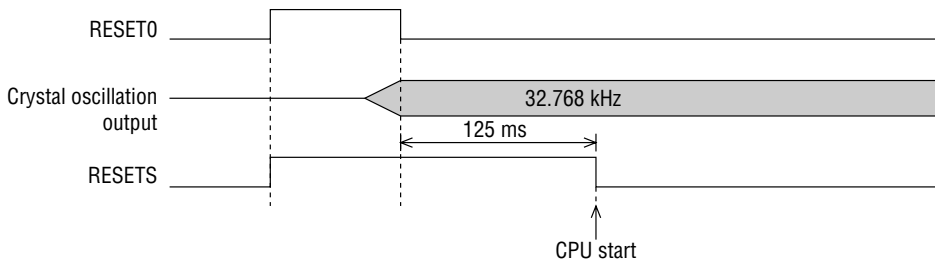
Figure 3-3 Signals When System Reset is Generated

⚠ Note:

- System reset takes priority over all other processing and terminates all processing up to that point in time. Therefore, the contents of RAM and display registers, which are not initialized, cannot be guaranteed after a system reset.

- When performing transfer to the system reset mode by setting the RESET pin to a "H" level, set the RESET pulse width to 1 ms or more.

3.3 Halt Mode

3.3.1 Transfer to and State of Halt Mode

Transfer to the halt mode is performed by the software when a HALT instruction is executed.

When a HALT instruction is executed, the CPU enters the HALT mode at the S2 state of the HALT instruction.

Oscillation and time base counter operation continue while in the halt mode.

If an interrupt request occurs at the same time as execution of a HALT instruction, interrupt processing has priority and the HALT instruction will not be executed. After the HALT instruction performs the equivalent operation of a NOP instruction, the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the instruction immediately following the HALT instruction.

Figure 3-4 shows the timing when a HALT instruction and interrupt request occur simultaneously.

n : HALT instruction address
(INT) : Starting address of interrupt routine
(RTI) : RTI instruction address
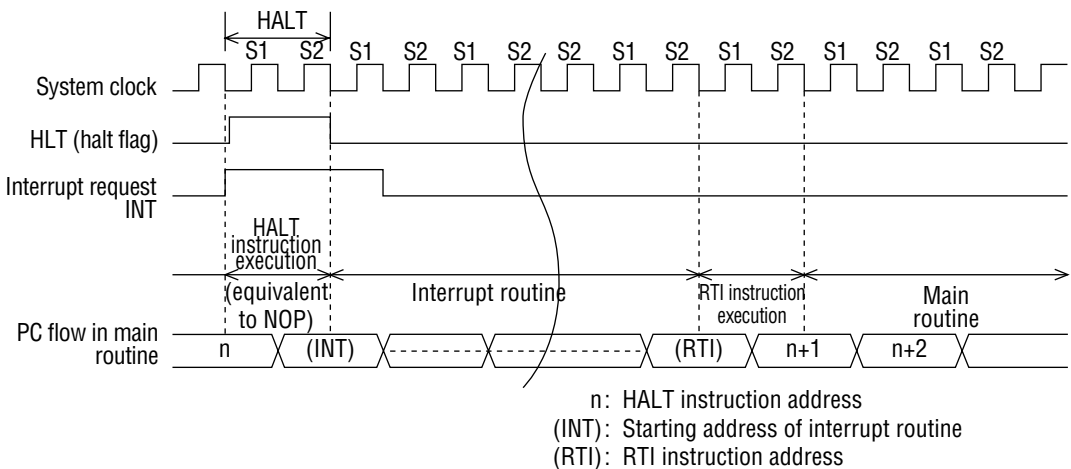
Figure 3-4 Timing of Simultaneous HALT Instruction and Interrupt Request

⚠ Note:

While an interrupt request is generated, execution of a HALT instruction will not transfer operation to the halt mode.

3.3.2 Halt Mode Release

The following two methods are available to release the halt mode.

- Release by interrupt generation (transfer to normal operation mode)
- Release by RESET pin (transfer to system reset mode)

3.3.2.1 Release of Halt Mode by Interrupt

If the halt mode is to be released by an interrupt, the enable flag of the interrupt used for release must be set to "1" prior to entering the halt mode. When the halt mode is released by an interrupt, operation transfers to the normal operation mode.

Figure 3-5 shows the timing of transferring to the halt mode by execution of a HALT instruction and of releasing the halt mode by an interrupt.

When the halt mode is released by an interrupt request, the first instruction immediately following the HALT instruction is executed and then the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the second instruction after the HALT instruction.
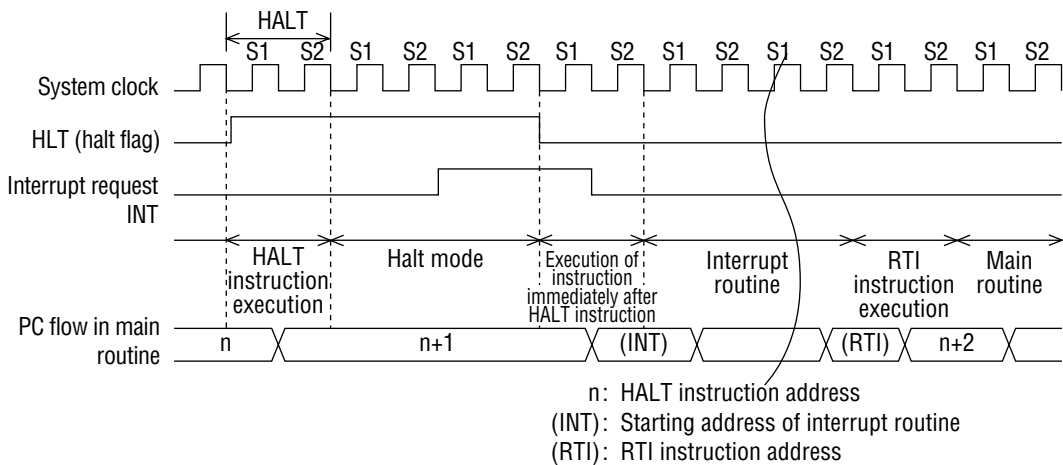
Figure 3-5 Timing of Transfer to Halt Mode and Release of Halt Mode by Interrupt

! Note:

If the halt mode is to be released, set individual interrupt enable flags to "1". If an individual interrupt enable flag is "0", the corresponding interrupt request signal cannot reset the HLT flag, regardless of whether the master interrupt enable flag (MIE) is "0" or "1".

3.3.2.2 Release of Halt Mode by RESET Pin

If a high-level is input to the RESET pin, the CPU is released from the halt mode and transfers to the system reset mode.

3.3.3 Melody Data Interrupt and Halt Mode Release

The halt mode is not released by a melody data interrupt.

The melody data interrupt is different from a conventional interrupt in that the melody data interrupt is a hardware processing interrupt used for transfer of melody data to the melody circuit. It is not dependent on the program.

When this interrupt is generated, the instruction immediately after the HALT instruction is executed, then the melody data is transferred to the melody circuit, and the HALT instruction is executed again. This sequence is indicated in Figure 3-6.
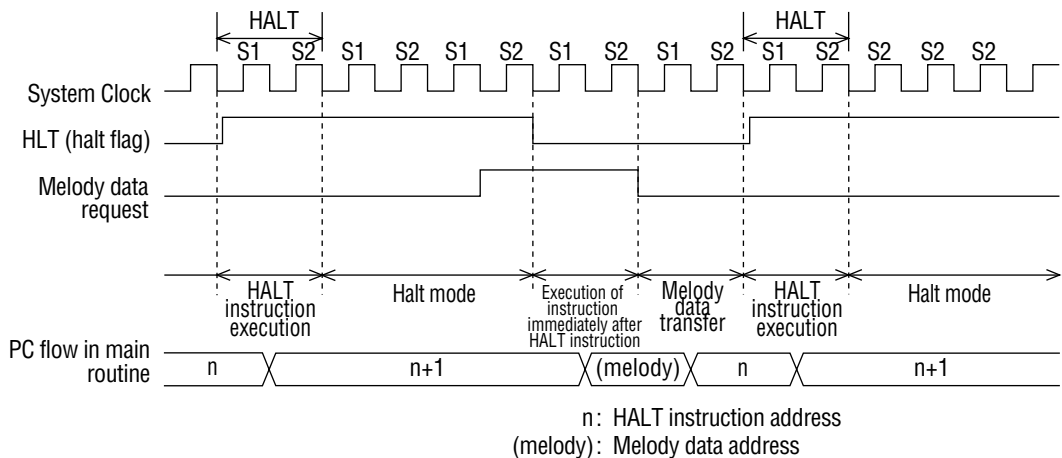
Figure 3-6 Melody Data Request Interrupt Operation

3.3.4 Note Concerning HALT Instruction

As described above, the instruction immediately after the HALT instruction may be executed any number of times. For this reason, always place an NOP instruction immediately after the HALT instruction.

```
(Example)      •

               •

               •

            HALT
            NOP
               •

               •

               •
```

Interrupt (INT326)

Chapter 4 Interrupt (INT326)

4.1 Overview

The ML63326 supports 17 interrupt factors: 4 external interrupts and 13 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). Watchdog timer interrupt is a non-maskable interrupt.

When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 4-1 indicates a list of interrupt factors, and Figure 4-1 shows the interrupt control equivalent circuit.

Table 4-1 List of Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External interrupt 0 (PB 4-bit OR input)	XI0INT	0014H
4	Voice synthesis interrupt	VOINT	0016H
5	External interrupt 2 (PE.3)	XI2INT	0018H
6	External interrupt 3 (PF 4-bit OR input)	XI3INT	001AH
7	External interrupt 5 (P0 4-bit OR input)	XI5INT	001EH
8	Timer 0 interrupt	TM0INT	0020H
9	Timer 1 interrupt	TM1INT	0022H
10	Timer 2 interrupt	TM2INT	0024H
11	Timer 3 interrupt	TM3INT	0026H
12	Shift register interrupt	SFTINT	002CH
13	T10 Hz interrupt	T10HzINT	002EH
14	32 Hz interrupt	32HzINT	0030H
15	16 Hz interrupt	16HzINT	0032H
16	4 Hz interrupt	4HzINT	0034H
17	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 6 (Time Base Counter), Chapter 7 (Timers), Chapter 8 (100 Hz Timer Counter), Chapter 9 (Watchdog Timer), Chapter 10 (Ports), Chapter 12 (Melody Driver), Chapter 13 (Voice Synthesis), and Chapter 14 (Shift Register).
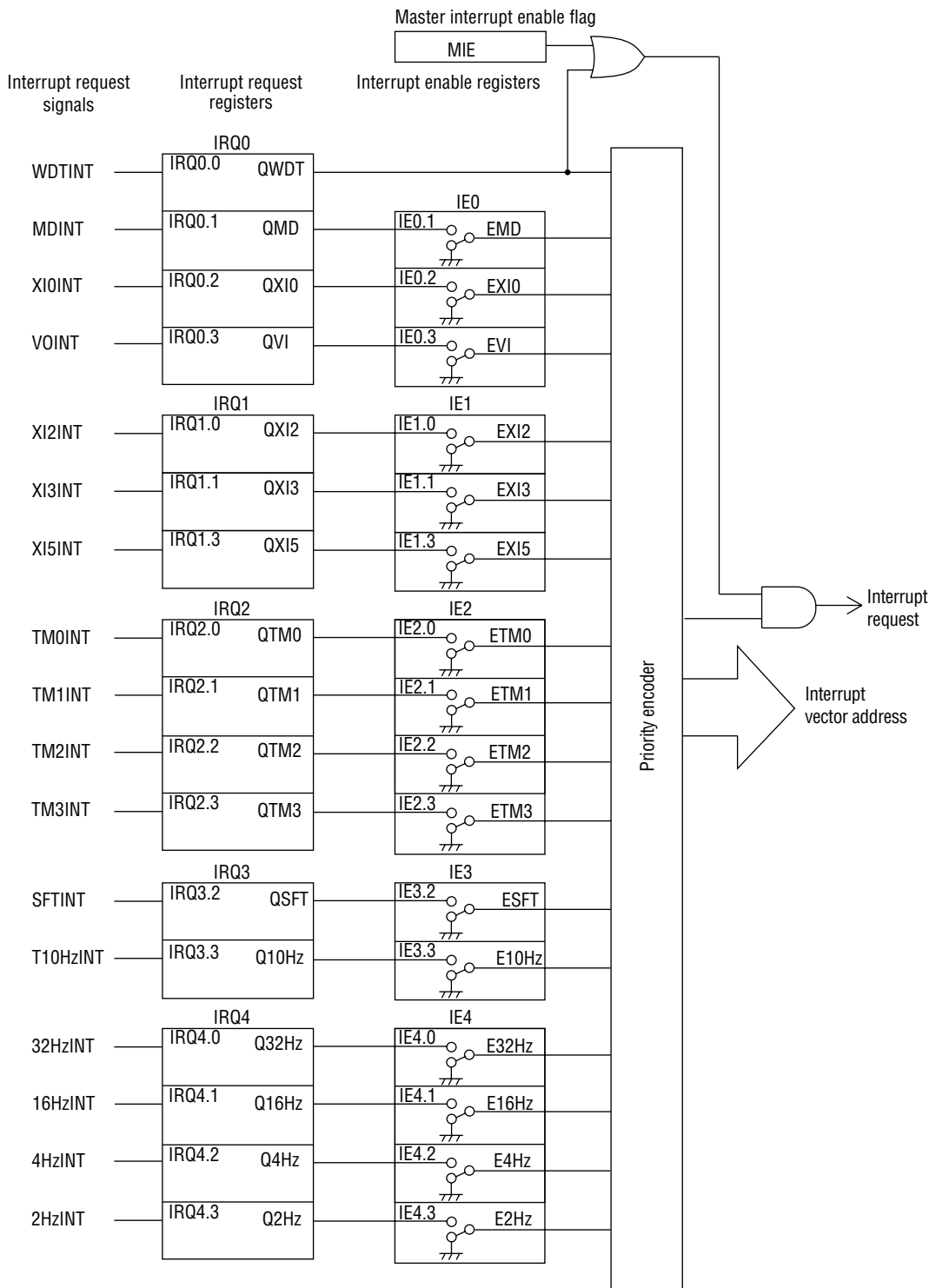
Figure 4-1 ML63326 Interrupt Control Equivalent Circuit

4.2 Interrupt Registers

The following three types of registers are used to control interrupts.

(1) Master interrupt enable register (MIEF)

(2) Interrupt enable registers (IE0 to IE4)

(3) Interrupt request registers (IRQ0 to IRQ4)

These registers are described below.

4

(1) Master interrupt enable register (MIEF)

MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt.

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute a RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.

	bit 3	bit 2	bit 1	bit 0
MIEF (0FFH) (R)	—	—	—	MIE

Master Interrupt Enable Flag
0: Interrupts disabled (initial value)
1: Interrupts enabled
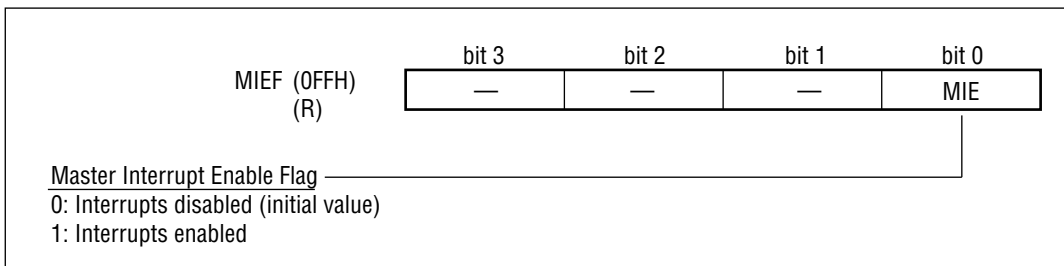
⚠ Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

(2) Interrupt enable registers (IE0 to IE4)

IE0, IE1, IE2, IE3, and IE4 are registers that consist of 4 bits each.

A logical AND of the corresponding bits of an interrupt enable register (IE0 to IE4) and an interrupt request register (IRQ0 to IRQ4) determines whether or not each interrupt request is issued to the CPU. The watchdog timer interrupt is non-maskable, and is therefore not dependent upon the interrupt enable registers (IE0 to IE4) and the master interrupt enable register (MIEF).

If multiple interrupts request the CPU at the same time, as shown in Table 5-1, the interrupts are accepted in order of highest priority and low priority interrupts are placed on hold.

When an interrupt is received, the master interrupt enable flag (MIE) is cleared to "0". The corresponding bits in the interrupt enable registers (IE0 to IE4) do not change.

At system reset, each bit of IE0 through IE4 is initialized to "0".

	bit 3	bit 2	bit 1	bit 0
IE0 (050H) (R/W)	EVI	EXI0	EMD	—

Voice synthesis interrupt enable flag ———
0: Disable (initial value)
1: Enable
External interrupt 0 enable flag ———
0: Disable (initial value)
1: Enable
Melody end interrupt enable flag———
0: Disable (initial value)
1: Enable

	bit 3	bit 2	bit 1	bit 0
IE1 (051H) (R/W)	EXI5	—	EXI3	EXI2

External interrupt 5 enable flag ———
0: Disable (initial value)
1: Enable
External interrupt 3 enable flag ———
0: Disable (initial value)
1: Enable
External interrupt 2 enable flag ———
0: Disable (initial value)
1: Enable

4

IE2 (052H)
(R/W)

	bit 3	bit 2	bit 1	bit 0
	ETM3	ETM2	ETM1	ETM0

Timer 3 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 2 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 1 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 0 interrupt enable flag
0: Disable (initial value)
1: Enable

IE3 (053H)
(R/W)

	bit 3	bit 2	bit 1	bit 0
	E10Hz	ESFT	—	—

10 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

Shift register interrupt enable flag
0: Disable (initial value)
1: Enable

IE4 (054H)
(R/W)

	bit 3	bit 2	bit 1	bit 0
	E2Hz	E4Hz	E16Hz	E32Hz

2 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

4 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

16 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

32 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

(3) Interrupt request registers (IRQ0 to IRQ4)

IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 are registers that consist of 4 bits each.

When an interrupt request is generated, the corresponding bit of the interrupt request register is set to "1" in the first half of the S1 state of the next instruction. So that the CPU can receive interrupt requests, set the master interrupt enable flag (MIE) to "1" and set the appropriate flag of the corresponding interrupt enable register (IE0 to IE4) to "1".

The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable register or the master interrupt enable register (MIEF).

Setting the appropriate bits of an interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is received, the corresponding bits of IRQ0 to IRQ4 are cleared to "0".

At system reset, each bit of IRQ0 through IRQ4 is initialized to "0".

	bit 3	bit 2	bit 1	bit 0
IRQ0 (055H) (R/W)	QVI	QXI0	QMD	QWDT

Voice synthesis interrupt request flag
0: No request (initial value)
1: Request
External interrupt 0 request flag
0: No request (initial value)
1: Request
Melody end interrupt request flag
0: No request (initial value)
1: Request
Watchdog timer interrupt request flag
0: No request (initial value)
1: Request
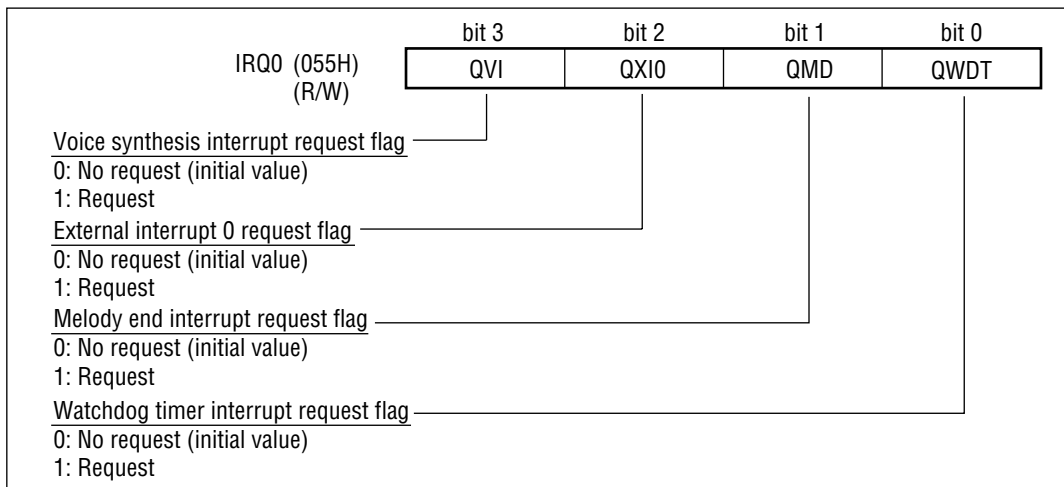
bit 3: QVI (reQuest Voice synthesis Interrupt)

This is the interrupt request signal from the voice synthesis section.

An interrupt request is generated when the setting of one voice phrase is completed and the setting of the next voice phrase is enabled by the voice synthesis section.

bit 2: QXI0 (reQuest eXternal Interrupt 0)

The external interrupt 0 request flag.

The external interrupt 0 is assigned as the secondary function of each bit of port B (PB.0 to PB.3). External interrupt 0 requests are generated by a 4-bit ORed input.

bit 1: QMD (reQuest Melody Driver)

Melody end interrupt request flag.

Melody end interrupts are generated when the melody driver outputs the end note data (END bit = "1").

bit 0: QWDT (reQuest WatchDog Timer)

Watchdog timer interrupt request flag.

When the watchdog timer is started and then overflow occurs, an interrupt is requested. The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable registers or the master interrupt enable register (MIE).

	bit 3	bit 2	bit 1	bit 0
IRQ1 (056H) (R/W)	QXI5	—	QXI3	QXI2

External interrupt 5 request flag
0: No request (initial value)
1: Request

External interrupt 3 request flag
0: No request (initial value)
1: Request

External interrupt 2 request flag
0: No request (initial value)
1: Request
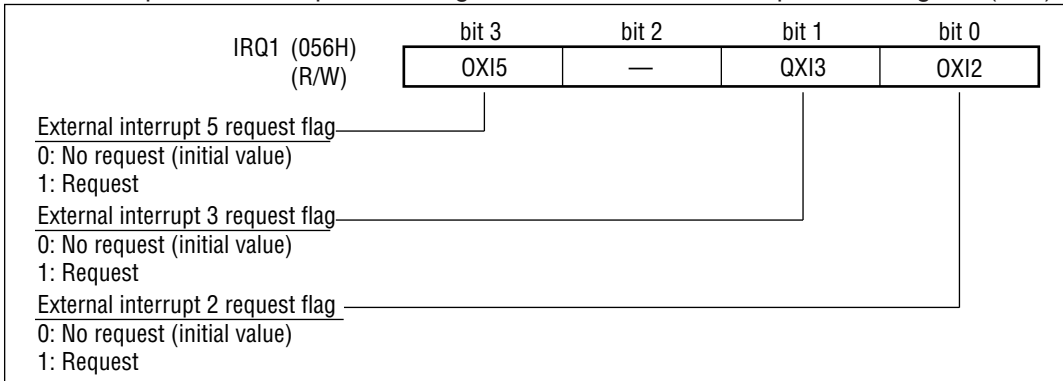
bit 3: QXI5 (reQuest eXternal Interrupt 5)
External interrupt 5 request flag.
The external interrupt 5 is assigned as a secondary function to each bit (P0.0 to 0.3) of port 0.
An external interrupt 5 request is generated through the 4-bit ORed input.

bit 1: QXI3 (reQuest eXternal Interrupt 3)
External interrupt 3 request flag.
The external interrupt 3 is assigned as a secondary function to each bit (PF.0 to PF.3) of port F.
An external interrupt 3 request is generated through the 4-bit ORed input.

bit 0: QXI2 (reQuest eXternal Interrupt 2)
External interrupt 2 request flag.
The external interrupt 2 is assigned as a secondary function of port E.3 (PE.3).
Generation of the external interrupt 2 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.

	bit 3	bit 2	bit 1	bit 0
IRQ2 (057H) (R/W)	QTM3	QTM2	QTM1	QTM0

Timer 3 interrupt request flag
0: No request (initial value)
1: Request

Timer 2 interrupt request flag
0: No request (initial value)
1: Request

Timer 1 interrupt request flag
0: No request (initial value)
1: Request

Timer 0 interrupt request flag
0: No request (initial value)
1: Request
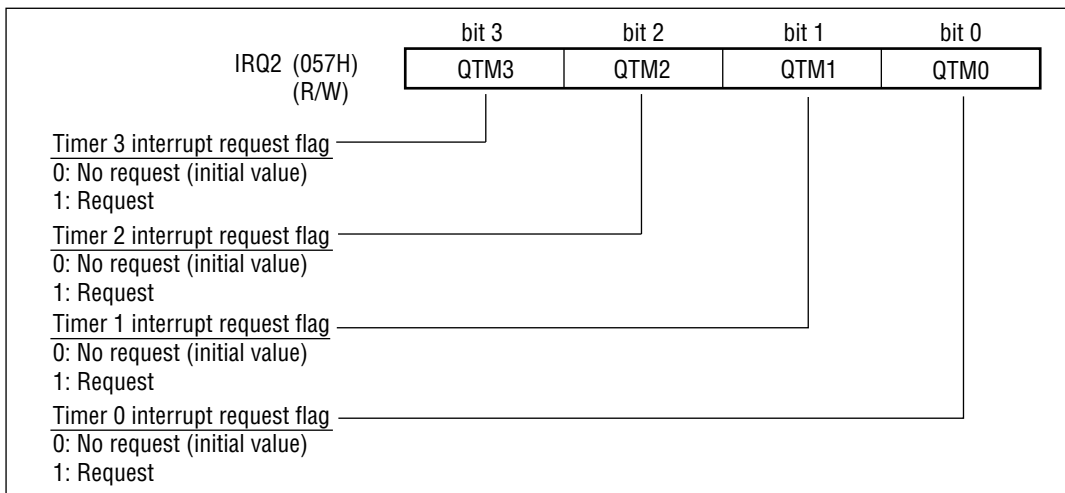
bit 3: QTM3 (reQuest TiMer 3)
   Timer 3 interrupt request flag.
   A timer 3 interrupt request is generated whenever timer 3 overflows.

bit 2: QTM2 (reQuest TiMer 2)
   Timer 2 interrupt request flag.
   A timer 2 interrupt request is generated whenever timer 2 overflows.

bit 1: QTM1 (reQuest TiMer 1)
   Timer 1 interrupt request flag.
   A timer 1 interrupt request is generated whenever timer 1 overflows.

bit 0: QTM0 (reQuest TiMer 0)
   Timer 0 interrupt request flag.
   A timer 0 interrupt request is generated whenever timer 0 overflows.

	bit 3	bit 2	bit 1	bit 0
IRQ3 (058H) (R/W)	Q10Hz	QSFT	—	—

10 Hz interrupt request flag
0: No request (initial value)
1: Request

Shift register interrupt request flag
0: No request (initial value)
1: Request
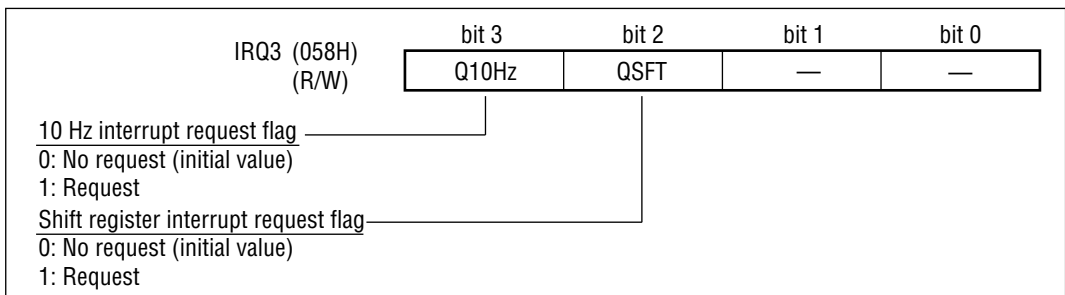
bit 3: Q10Hz (reQuest 10 Hz)
   10 Hz interrupt request flag.
   A 10 Hz interrupt request is generated whenever the 10 Hz carry generated by the 100 Hz timer counter is output.

bit 2: QSFT (reQuest ShiFT register)
   Shift register interrupt request flag.
   A shift register interrupt is generated when the 8-bit data transfer for the shift register is completed.

	bit 3	bit 2	bit 1	bit 0
IRQ4 (059H) (R/W)	Q2Hz	Q4Hz	Q16Hz	Q32Hz

2 Hz interrupt request flag
0: No request (initial value)
1: Request

4 Hz interrupt request flag
0: No request (initial value)
1: Request

16 Hz interrupt request flag
0: No request (initial value)
1: Request

32 Hz interrupt request flag
0: No request (initial value)
1: Request

4
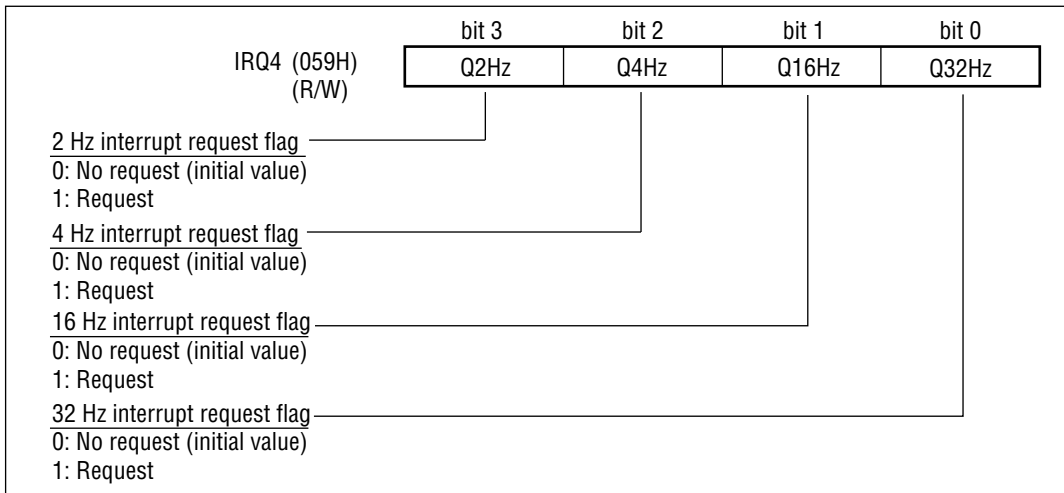
bit 3: Q2Hz (reQuest 2 Hz)

2 Hz interrupt request flag.

A 2 Hz interrupt request is generated at every falling edge of the 2 Hz output of the time base counter.

bit 2: Q4Hz (reQuest 4 Hz)

4 Hz interrupt request flag.

A 4 Hz interrupt request is generated at every falling edge of the 4 Hz output of the time base counter.

bit1: Q16Hz (reQuest 16 Hz)

16 Hz interrupt request flag.

A 16 Hz interrupt request is generated at every falling edge of the 16 Hz output of the time base counter.

bit 0: Q32Hz (reQuest 32 Hz)

32 Hz interrupt request flag.

A 32 Hz interrupt request is generated at every falling edge of the 32 Hz output of the time base counter.

4.3 Interrupt Sequence

4.3.1 Interrupt Processing

While MIE is "1", operation transfers to interrupt processing when individual interrupt factors are generated.

The watchdog timer interrupt is non-maskable and regardless of the MIE flag status, operation will shift to interrupt processing when the watchdog timer interrupt factor is generated.

The following processes are performed when an interrupt is generated.

(1) MIE and the corresponding interrupt request flag are cleared to "0".

(2) The program counter (PC) is saved on the call stack.

(3) The call stack pointer (SP) is incremented by 1. (SP←SP+1)

(4) The starting address of the interrupt routine is loaded into the program counter (PC).

Interrupt processing is performed in 0 machine cycles.

Figure 4-2 shows the stack contents after an interrupt is generated.
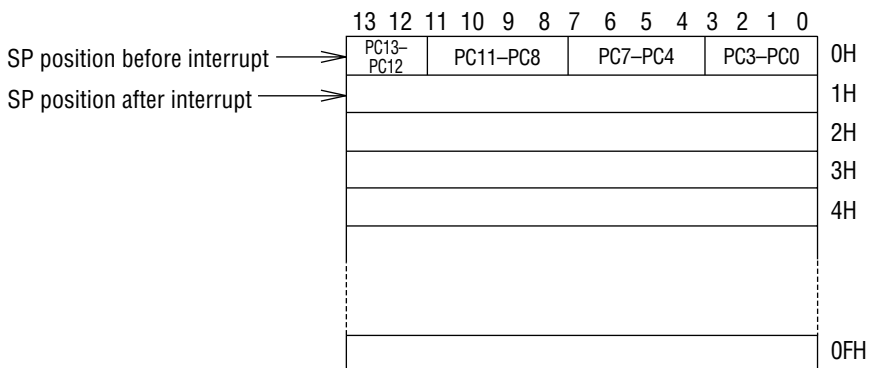
Figure 4-2 Call Stack Contents after Interrupt Generation

4.3.2 Return from an Interrupt Routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

4

(1) The call stack pointer (SP) is decremented by 1. (SP←SP−1)

(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).

(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

⚠ Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.

- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

4.3.3 Interrupt Hold Instructions

Interrupt requests are not received during execution of the following instructions. These instructions are processed with priority, and interrupt processing is delayed until completion of the instruction.

- ROM table reference instructions

- External memory transfer instruction

- Stack operation instructions

- Jump instructions

- Conditional branch instructions

- Call/return instructions

- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr15" (start melody output) instructions within control instructions

⚠ Note:

If the above instructions are used consecutively, even if an interrupt is generated, that interrupt may be put on hold for a considerable amount of time before the interrupt routine begins.

Clock Generator Circuit (OSC)

Chapter 5 Clock Generator Circuit (OSC)

5.1 Overview

The clock generator circuit (OSC) consists of a low-speed clock generator circuit, a high-speed clock generator circuit and a clock controller unit. The clock generator circuit generates the system clock (CLK), time base clock (TBCCLK) and the high-speed clock (HSCLK).

The following modes can be selected for the low-speed clock generator circuit and the high-speed clock generator circuit.

- Low-speed clock generator circuit: crystal oscillation mode or RC oscillation mode (mask option selection)
- High-speed clock generator circuit: crystal oscillation mode or RC oscillation mode (software selection)

The system clock is the basic operation clock for the CPU. The time base clock is the basic operation clock for the time base counter.

Depending on the contents of the frequency control register (FCON), the system clock frequency is switched to either the output of the low-speed clock generator circuit (TBCCLK) or the output of the high-speed clock generator circuit (HSCLK).

The frequency control register (FCON) also controls modes of the high-speed clock generator circuit.

5.2 Clock Generator Circuit Configuration

Figure 5-1 shows a block diagram of the clock generator circuit.
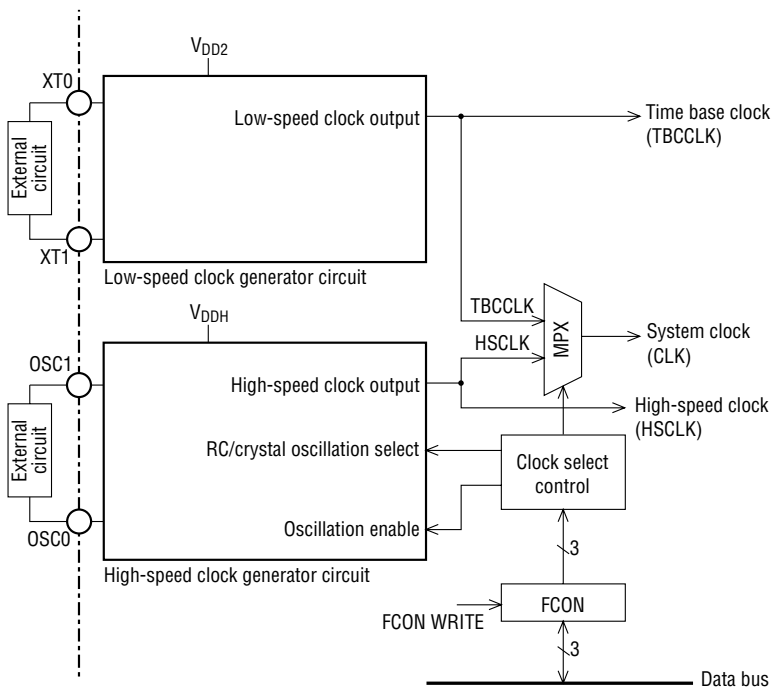
Figure 5-1 Clock Generator Circuit Configuration

5.3 Low-Speed Clock Generator Circuit

The low-speed clock generator circuit has two modes that are selected by the mask option, the RC oscillation mode and crystal oscillation mode. The oscillation frequency is 30 to 80 kHz.

For the RC oscillation mode, attach an external resistor, R_{OSL}, as shown in Figure 5-2(a).

For the crystal oscillation mode, attach an external crystal unit and capacitor, C_G, as shown in Figure 5-2(b).

(a) External Circuit for RC Oscillation Mode

(b) External Circuit for Crystal Oscillation Mode
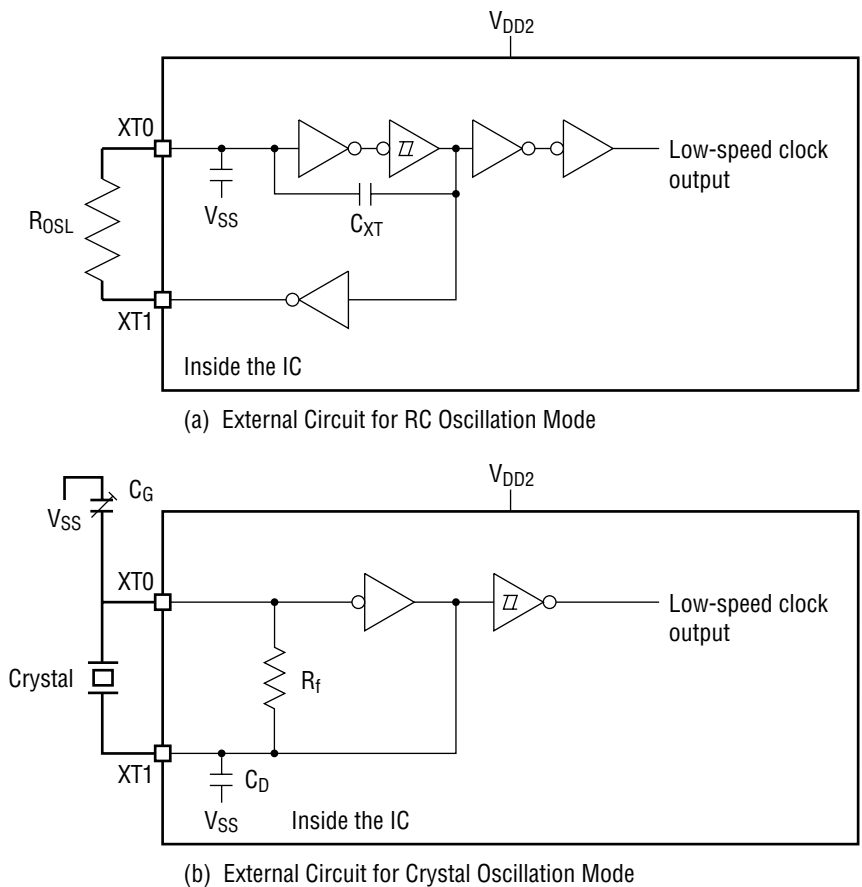
Figure 5-2 External Circuits for Low-Speed Clock Oscillation

⚠ Note:

For convenience, the descriptions of this manual assume that a 32.768 kHz crystal unit is used in the low-speed clock generator circuit.

For the method of specifying mask options for the low-speed clock generator circuit, see "Appendix G: Mask Option."

Table 5-1 lists typical values of oscillation frequency when the low-speed side RC oscillation mode is selected. Table 5-2 shows an example external component to be attached when the low-speed side crystal oscillation mode is selected.

Table 5-1 Typical Oscillation Frequencies for the Low-Speed Side RC Oscillation Mode (Typ.)

R_{OSL}	f_{ROSL}
1.5 MΩ	32 kHz ±30%
700 kΩ	60 kHz ±30%
400 kΩ	80 kHz ±30%

Table 5-2 Example External Component for the Low-Speed Side Crystal Oscillation Mode

C_G	f_{XT}
12 pF	32.768 kHz

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5.4 High-Speed Clock Generator Circuit

The high-speed clock generator circuit has two modes, the RC oscillation mode and crystal oscillation mode. Oscillation modes are set by OSCSEL (bit 2 of FCON).

- OSCSEL = "0" : RC oscillation mode
- OSCSEL = "1" : crystal oscillation mode

During the RC oscillation mode, the source oscillation clock is output as the high-speed clock. The maximum frequency in this case is 2.048 MHz.

During the crystal oscillation mode, the half frequency waveform of the source oscillations is output as the high-speed clock. The maximum frequency of the source oscillations in this case is 4.096 MHz.

If the high-speed clock is not to be used, leave the OSC0 and OSC1 pins open (unconnected).

For the RC oscillation mode, attach an external resistor, R_{OSH}, as shown in Figure 5-3(a).

For the crystal oscillation mode, attach an external crystal unit and capacitors as shown in Figure 5-3(b).

(a) External Circuit for RC Oscillation Mode

(b) External Circuit for Crystal Oscillation Mode
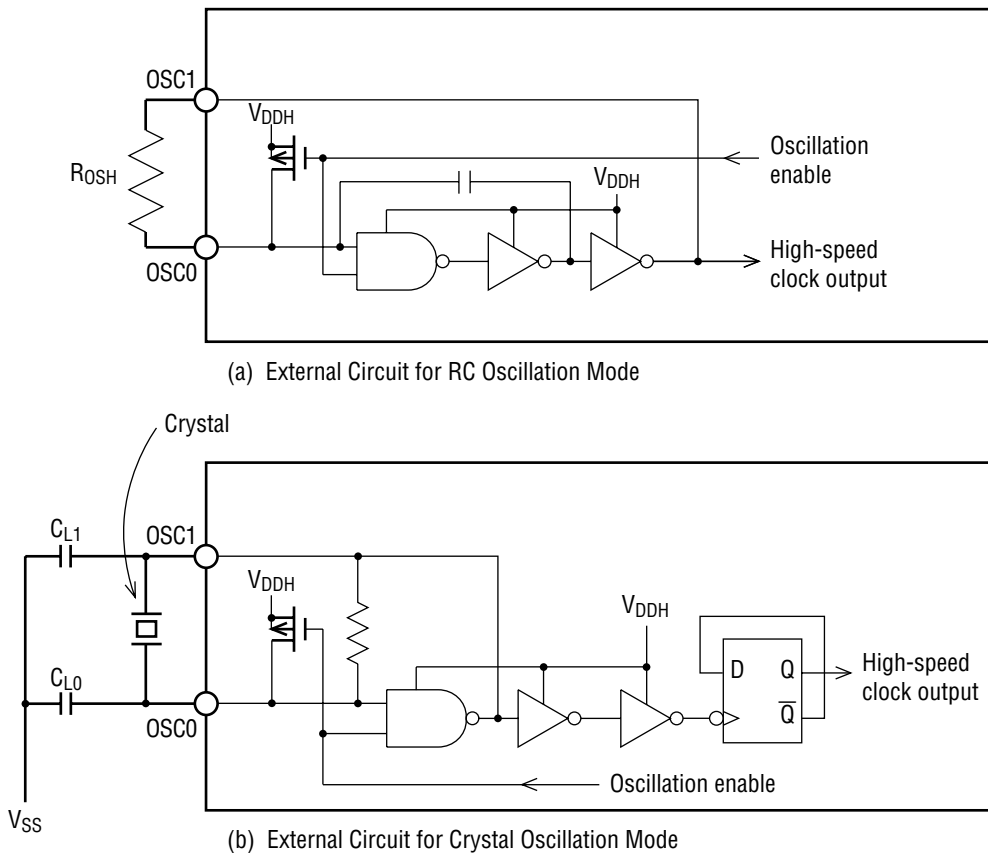
Figure 5-3 External Circuits for High-Speed Clock Oscillation

Table 5-3 lists typical values of oscillation frequency when the high-speed side RC oscillation mode is selected. Table 5-4 lists example external components to be attached when the high-speed side crystal oscillation mode is selected.

Table 5-3 Typical Oscillation Frequencies for the High-Speed Side RC Oscillation Mode (Typ.)

R_{OSH}	V_{DDH}*	f_{ROSH}
39 kΩ	3.6 V	1.9 MHz ±30%
	4.2 V	2.1 MHz ±30%
	4.8 V	2.2 MHz ±30%
47 kΩ	3.6 V	1.6 MHz ±30%
	4.2 V	1.7 MHz ±30%
	4.8 V	1.8 MHz ±30%

⚠ Note:

*: The power supply voltage V_{DDH} of the high-speed clock generator circuit is a voltage obtained by doubling the voltage V_{DD2} used in the LCD bias generator section. Take care because V_{DD2} can be varied from 1.8 V to 2.4 V using the display contrast register (DSPCNT). For details, see Chapter 15, "LCD Driver" and Chapter 17, "Power Supply Circuit."

Table 5-4 Example External Components for the High-Speed Side Crystal Oscillation Mode

C_{L0}	C_{L1}	Crystal unit
8 pF	8 pF	AT-49 (4.096 MHz)*

*: Manufactured by Daishinku Corp.

5.5 System Clock Control

The system clock is the basic operation clock of the CPU.

The clock can be selected as follows with the CPUCLK (bit 0 of FCON) setting.

- CPUCLK = "0" (initial value)

  The output of the low-speed clock generator circuit (TBCCLK) is the system clock.

- CPUCLK = "1"

  The output of the high-speed clock generator circuit (HSCLK) is the system clock.

When HSCLK is selected as the system clock, the high-speed clock must be in the oscillating state (ENOSC = "1"). The low-speed generator circuit will continue to oscillate even when the high-speed generator circuit is selected.

To reduce the total power consumption in applications that use the high-speed clock generator circuit, the following clock controls are generally implemented in software.

- During normal operation, the output of the low-speed clock generator circuit (CPUCLK = "0") should be the system clock.

- Only when high-speed operation is necessary should the high-speed clock oscillate (ENOSC = "1") and output of the high-speed clock generator circuit (CPUCLK = "1") should be selected.

For details of the system clock select timing, refer to section 5.7, "System Clock Select Timing."

5.6 Frequency Control Register (FCON)

FCON is a special function register (SFR) that selects the system clock.

	bit 3	bit 2	bit 1	bit 0
FCON (062H) (R/W)	—	OSCSEL	ENOSC	CPUCLK

RC oscillation/ceramic oscillation mode select
0: RC oscillation mode (initial value)
1: Crystal oscillation mode

High-speed clock oscillation start/stop select
0: Oscillation stop (initial value)
1: Oscillation start

System clock select
0: Low-speed clock oscillation output (initial value)
1: High-speed clock oscillation output

5

bit 2: OSCSEL

This bit selects the RC oscillation mode or the crystal oscillation mode of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", selecting the RC oscillation mode.

bit 1: ENOSC

This bit starts and stops oscillation of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", stopping oscillation of the high-speed clock generator circuit.

bit 0: CPUCLK

This bit selects the system clock, the basic operation clock of the CPU. At system reset, this bit is cleared to "0", selecting output of the low-speed clock generator circuit (TBCCLK).

5.7 System Clock Select Timing

After system reset, the system clock is TBCCLK.

When high-speed operation is necessary, switch the system clock to HSCLK.

A flowchart of system clock operation is shown below.

System clock status

TBCCLK
(Low-speed clock generator circuit output)

After system reset, the low-speed clock generator output is the system clock.

Software processing

Software processing

(1) High-speed clock oscillation mode select

OSCSEL (bit 2 of FCON) setting

OSCSEL = "0" : RC oscillation mode
                     (initial value)
OSCSEL = "1" : Crystal oscillation mode

(2) High-speed clock oscillation stop

ENOSC (bit 1 of FCON) = "0"

ENOSC = "0" : Stop high-speed clock oscillation
                     (initial value)
ENOSC = "1" : Start high-speed clock oscillation

(1) Low-speed clock oscillation output select

CPUCLK (bit 0 of FCON) = "0"

CPUCLK = "0" : Low-speed clock oscillation output
                      (initial value)
CPUCLK = "1" : High-speed clock oscillation output

(2) High-speed clock oscillation start

ENOSC (bit 1 of FCON) = "1"

ENOSC = "0" : Stop high-speed clock oscillation
                     (initial value)
ENOSC = "1" : Start high-speed clock oscillation

Wait:
When RC oscillation mode selected:
5 ms or more
When crystal oscillation mode selected:
10 ms or more

(3) High-speed clock oscillation output select

CPUCLK (bit 0 of FCON) = "1"

CPUCLK = "0" : Low-speed clock oscillation output
                      (initial value)
CPUCLK = "1" : High-speed clock oscillation output

HSCLK
(High-speed clock generator circuit output)

When ENOSC (bit 1 of FCON) is set to "1", the voltage doubler circuit that doubles V_{DD2} starts operating and outputs the power supply voltage (V_{DDH}) for high speed oscillation. The oscillations are started in the mode set by OSCSEL. At the same time, the internal logic power supply voltage (V_{DDL}) switches from the constant voltage circuit output level (approx. 1.7 V) to the V_{DDH} level. Next, if CPUCLK is set to "1", the system clock switches from crystal oscillation output (TBCCLK) to high-speed clock output (HSCLK).

Figure 5-4 shows the system clock select timing and status of the power supply voltage for high-speed oscillation (V_{DDH}) and the internal logic power supply voltage (V_{DDL}).
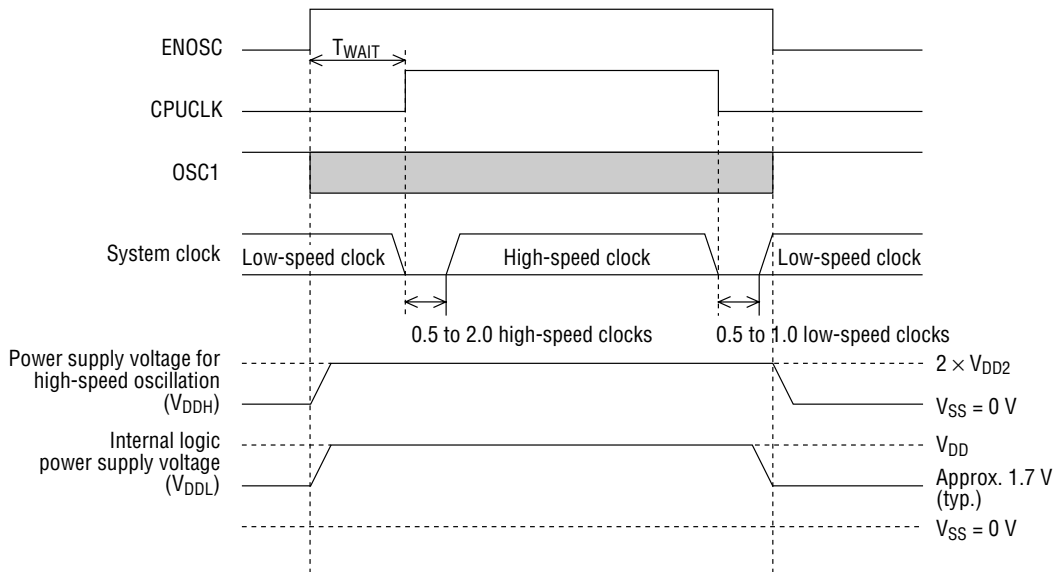
Figure 5-4 System Clock Select Timing

In the crystal oscillation mode, 10 ms are required from the time when ENOSC is set to "1" until the high-speed clock generator circuit enters the oscillating state. Therefore, in this mode, when switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 10 ms after the rising edge of ENOSC.

In the CR oscillation mode, oscillation begins soon after setting ENOSC to "1". However, it takes about 5 ms for the power supply voltage for high-speed oscillation (V_{DDH}) to stabilize. Therefore, when switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 5 ms after the rising edge of ENOSC.

When switching from the high-speed mode to the low-speed mode, set the CPUCLK bit to "0", and sometime after the next instruction, set the ENOSC bit to "0".

For details regarding the power supply for high-speed oscillation and the constant voltage circuit for the internal logic power supply, refer to Chapter 17, "Power Supply Circuit."

Time Base Counter (TBC)

Chapter 6 Time Base Counter (TBC)

6.1 Overview

The time base counter (TBC) is a 15-bit internal counter, which generates the clock supplied to internal peripheral functions.

The TBC clock is a time base clock (TBCCLK).

TBC outputs are used for functions such as time base interrupts and various other circuits. TBC8–11 and TBC12–15 can be read/reset by software.

The TBC generates an interrupt request at the falling edge of 32 Hz/16 Hz/4 Hz/2 Hz output.

The TBC is initialized to 0000H at system reset.

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6.2 Time Base Counter Configuration

The configuration of the time base counter (TBC) is shown in Figure 6-1.
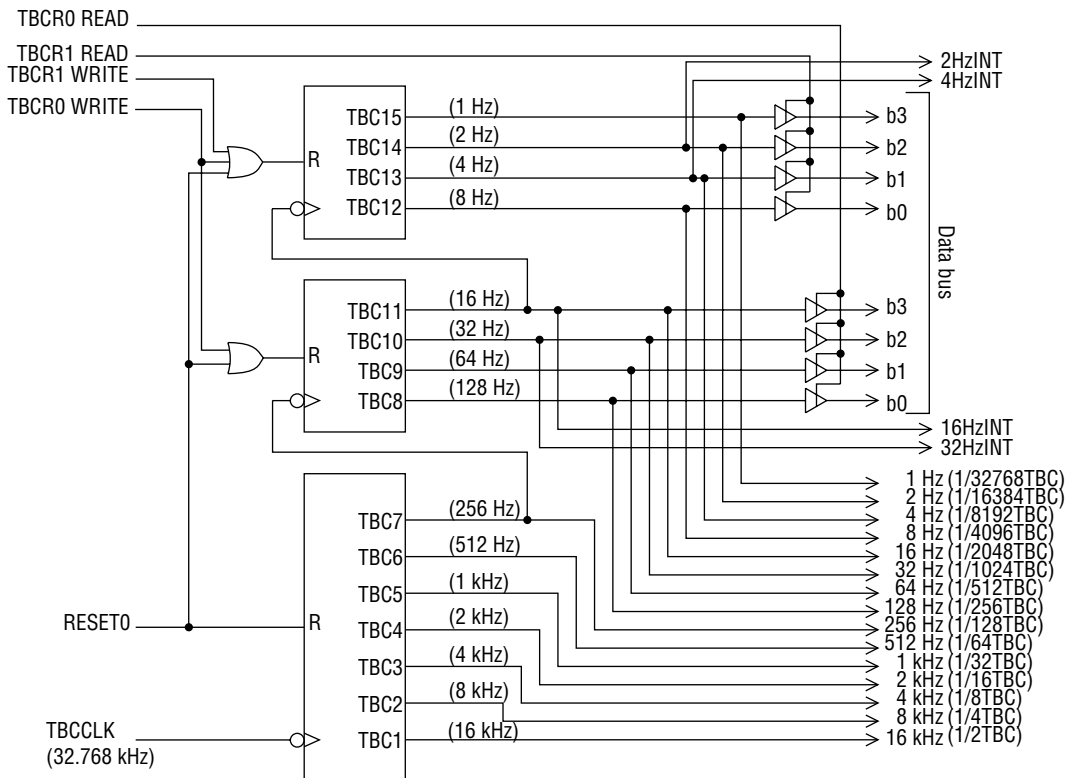
Figure 6-1 Time Base Counter (TBC) Configuration

(when a 32.768 kHz crystal is used for low-speed clock oscillation)

6.3 Time Base Counter Registers

Time base counter register 0 (TBCR0), time base counter register 1 (TBCR1)

These 4-bit special function registers (SFRs) are used to read the 1 to 8 Hz and 16 to 128 Hz outputs of the time base counter.

A write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz outputs to "0", and a write operation to TBCR1 sets the 1 to 8 Hz output to "0".

	bit 3	bit 2	bit 1	bit 0
TBCR0 (060H) (R/W)	16 Hz	32 Hz	64 Hz	128 Hz

	bit 3	bit 2	bit 1	bit 0
TBCR1 (061H) (R/W)	1 Hz	2 Hz	4 Hz	8 Hz

6.4 Time Base Counter Operation

After system reset the time base counter (TBC) begins to count up from 0000H. The count is incremented at the falling edge of the TBCCLK.

TBC 32 Hz/16 Hz/4 Hz/2 Hz outputs are used as time base interrupts. At each output falling edge, four bits of interrupt request register 4 (IRQ4) are set to "1", namely bit 3 (Q32Hz), bit 2 (Q16Hz), bit 1 (Q4Hz) and bit 0 (Q2Hz), requesting an interrupt to the CPU. TBC outputs are also used as clocks for various circuits.

TBC 1 to 8 Hz output and 16 to 128 Hz output can be read through the time base counter register 0/1 (TBCR0/TBCR1).

A write operation to TBCR1 sets the 1 to 8 Hz output counter to "0", and a write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz output counters to "0". The write data in these write operations has no significance. For example, the "MOV TBCR0, A" instruction can be used to write, but is not dependent on accumulator content in any way. When write is executed to TBCR0 and TBCR1 and the 1 to 8 Hz and 16 to 128 Hz counters reset, interrupt requests are generated if 32 Hz/16 Hz/4 Hz/2 Hz outputs have been set to "1". To disable these interrupts, first set the master interrupt enable flag (MIE) or interrupt enable register 4 (IE4) to "0", execute the write operation to TBCR 0/1, and set the interrupt request flag 4 (IRQ4) to "0".

Figure 6-2 shows interrupt generation timing and time base counter output reset timing by writing "1" to TBCR0 and TBCR1.

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$1^{+0}_{-1/16}$ second

$1^{+0}_{-1/256}$ second

Shows interrupt timing
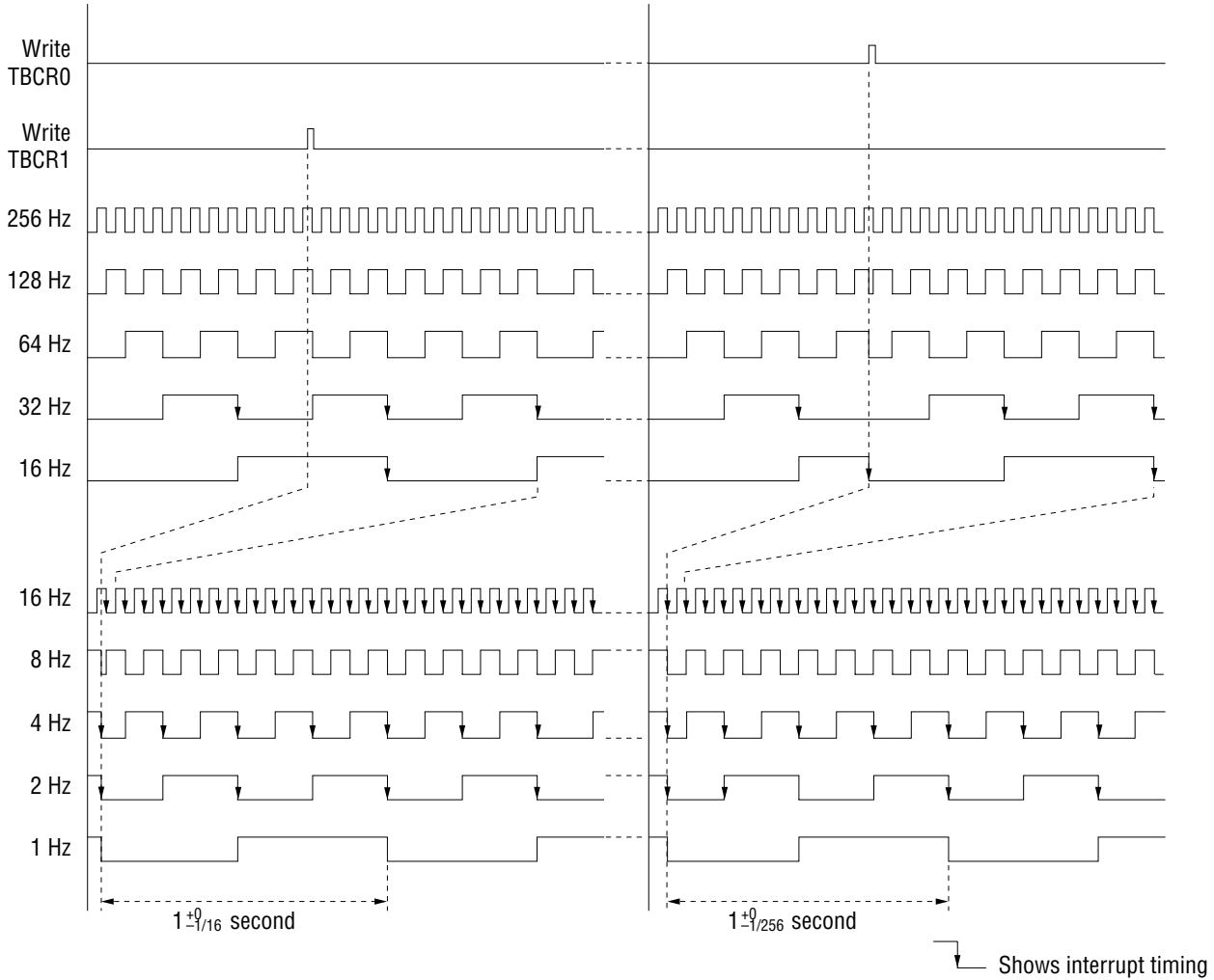
Figure 6-2 Interrupt Timing and Reset Timing by Writing "1" to TBCR0, TBCR1

Timers (TIMER)

Chapter 7 Timers (TIMER)

7.1 Overview

The ML63326 has four internal 8-bit timers (0 to 3). Timers 0 and 1, or timers 2 and 3, can be used in tandem as a 16-bit timer.

Timers 0 and 1 have three operation modes: auto-reload mode, capture mode and frequency measurement mode. Timers 2 and 3 have two modes: auto-reload and frequency measurement. Timer clock may be set to the time base clock (TBCCLK: 32.768 kHz), the high-speed clock (HSCLK), or an external clock. When using the timers as a 16-bit timer, the overflow signals of timers 0 and 2 are used as the clocks for timers 1 and 3, respectively.

In addition to pulse generation and time measurement, timers can also be used.

	Timer 0	Timer 1	Timer 2	Timer 3
8-bit timer	●	●	●	●
16-bit timer	●		●	
	(Timer 0 overflow signal is used as clock for timer 1)		(Timer 2 overflow signal is used as clock for timer 3)	
Clock	TBCCLK / HSCLK / External clock (T02CK, T13CK)			
Auto-reload mode	●	●	●	●
Capture mode	●	●	—	—
Frequency measurement mode	●	●	●	●

7.2 Timer Configuration

Figures 7-1 through 7-4 show the configuration of timers 0 to 3.
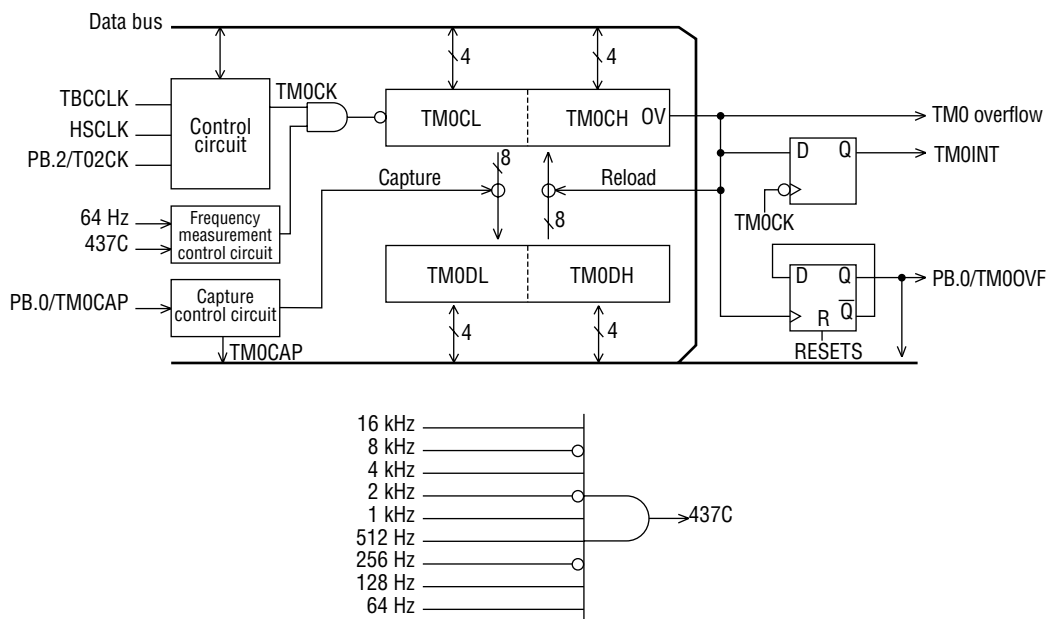
Figure 7-1 Timer 0 Configuration
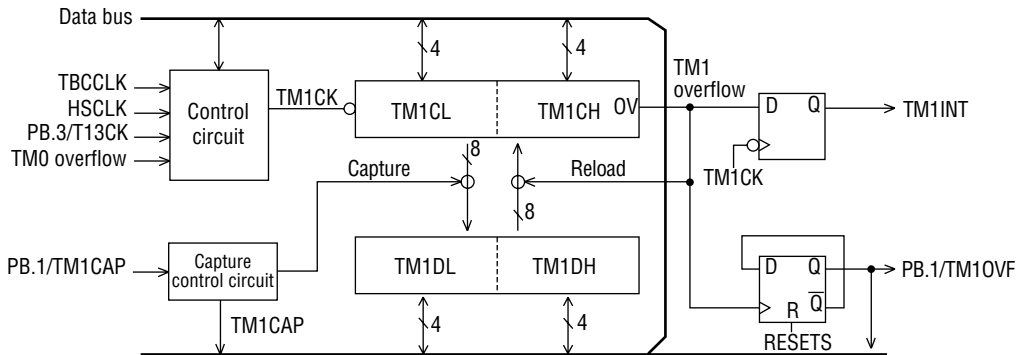
Figure 7-2 Timer 1 Configuration
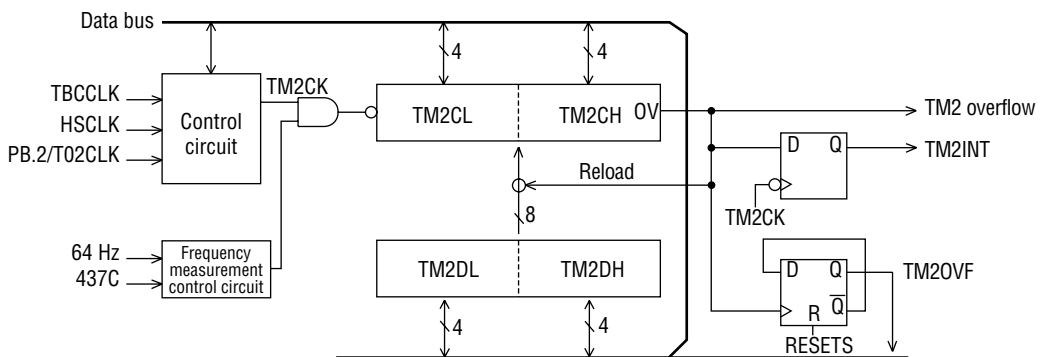
Figure 7-3 Timer 2 Configuration
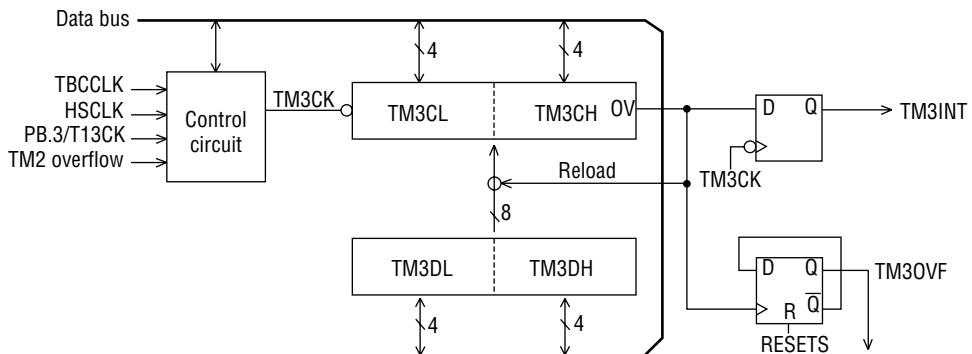
Figure 7-4 Timer 3 Configuration

7.3 Timer Registers

The following four registers are used for timer control.

(1) Timer data registers
    (TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL, TM3DH)
(2) Timer counter registers
    (TM0CL, TM0CH, TM1CL, TM1CH, TM2CL, TM2CH, TM3CL, TM3CH)
(3) Timer control registers
    (TM0CON0, TM0CON1, TM1CON0, TM1CON1, TM2CON0, TM2CON1, TM3CON0, TM3CON1)
(4) Timer status registers
    (TM0STAT, TM1STAT, TM2STAT, TM3STAT)

Each register is described below.

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(1) Timer data registers

(TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL, TM3DH)

- During the auto-reload mode, timer data registers store the reload values.
- During the capture mode, timer data registers store the capture data.
  Writing to a timer data register causes the contents of the timer counter register to be transferred to the timer data register.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

		bit 3	bit 2	bit 1	bit 0
TM0DL (Timer 0 lower)	(068H) (R/W)	T0D3	T0D2	T0D1	T0D0

		bit 3	bit 2	bit 1	bit 0
TM0DH (Timer 0 upper)	(069H) (R/W)	T0D7	T0D6	T0D5	T0D4

Timer 1 Registers

		bit 3	bit 2	bit 1	bit 0
TM1DL (Timer 1 lower)	(06AH) (R/W)	T1D3	T1D2	T1D1	T1D0

		bit 3	bit 2	bit 1	bit 0
TM1DH (Timer 1 upper)	(06BH) (R/W)	T1D7	T1D6	T1D5	T1D4

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2DL (076H) (Timer 2 lower) (R/W)		T2D3	T2D2	T2D1	T2D0

		bit 3	bit 2	bit 1	bit 0
TM2DH (077H) (Timer 2 upper) (R/W)		T2D7	T2D6	T2D5	T2D4

Timer 3 Registers

		bit 3	bit 2	bit 1	bit 0
TM3DL (078H) (Timer 3 lower) (R/W)		T3D3	T3D2	T3D1	T3D0

		bit 3	bit 2	bit 1	bit 0
TM3DH (079H) (Timer 3 upper) (R/W)		T3D7	T3D6	T3D5	T3D4

(2) Timer counter registers

(TM0CL, TM0CH, TM1CL, TM1CH, TM2CL, TM2CH, TM3CL, TM3CH)

- 8-bit binary counter operation
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:

  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

		bit 3	bit 2	bit 1	bit 0
TM0CL (06CH) (Timer 0 lower) (R/W)		T0C3	T0C2	T0C1	T0C0

		bit 3	bit 2	bit 1	bit 0
TM0CH (06DH) (Timer 0 upper) (R/W)		T0C7	T0C6	T0C5	T0C4

Timer 1 Registers

		bit 3	bit 2	bit 1	bit 0
TM1CL (Timer 1 lower)	(06EH) (R/W)	T1C3	T1C2	T1C1	T1C0

		bit 3	bit 2	bit 1	bit 0
TM1CH (Timer 1 upper)	(06FH) (R/W)	T1C7	T1C6	T1C5	T1C4

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2CL (Timer 2 lower)	(07AH) (R/W)	T2C3	T2C2	T2C1	T2C0

		bit 3	bit 2	bit 1	bit 0
TM2CH (Timer 2 upper)	(07BH) (R/W)	T2C7	T2C6	T2C5	T2C4

Timer 3 Registers

		bit 3	bit 2	bit 1	bit 0
TM3CL (Timer 3 lower)	(07CH) (R/W)	T3C3	T3C2	T3C1	T3C0

		bit 3	bit 2	bit 1	bit 0
TM3CH (Timer 3 upper)	(07DH) (R/W)	T3C7	T3C6	T3C5	T3C4

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(3) Timer control registers

(TM0CON0, TM0CON1, TM1CON0, TM1CON1, TM2CON0, TM2CON1, TM3CON0, TM3CON1)

- Timer control registers select the operation mode and clock for each timer.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

To use timer 1 in combination as a 16-bit timer, set timer 1 control registers TM1CON0 and TM1CON1.

	bit 3	bit 2	bit 1	bit 0
TM0CON0 (070H) (R/W)	—	FMEAS0	TM0ECAP	TM0RUN

Timer 0 mode select

bit 2	bit 1	bit 0		
0	0	0	:	Auto-reload mode stop (initial value)
0	0	1	:	Auto-reload mode operation
0	1	0	:	Capture mode stop
0	1	1	:	Capture mode operation
1	0	0	:	Frequency measurement mode operation
1	0	1	:	Not used
1	1	0	:	Not used
1	1	1	:	Not used
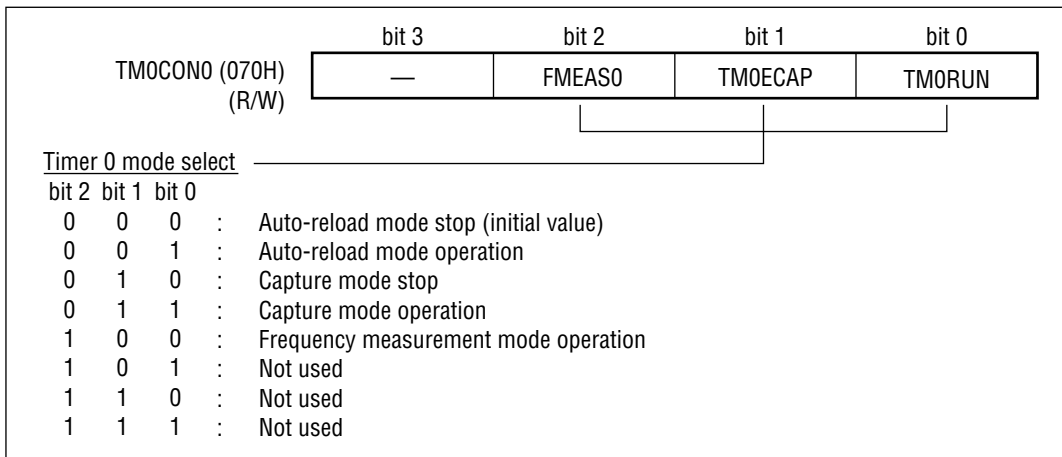
bit 2, 1, 0: FMEAS0, TM0ECAP, TM0RUN

These bits select the timer 0 operation mode.

The timer 0 operation mode can be selected as auto-reload mode, capture mode, or frequency measurement mode.

	bit 3	bit 2	bit 1	bit 0
TM0CON1 (071H) (R/W)	—	—	TM0CL1	TM0CL0

Timer 0 clock select

bit 1 bit 0
0   0   :   TBCCLK (initial value)
0   1   :   HSCLK (high-speed clock)
1   0   :   External clock
1   1   :   Not used
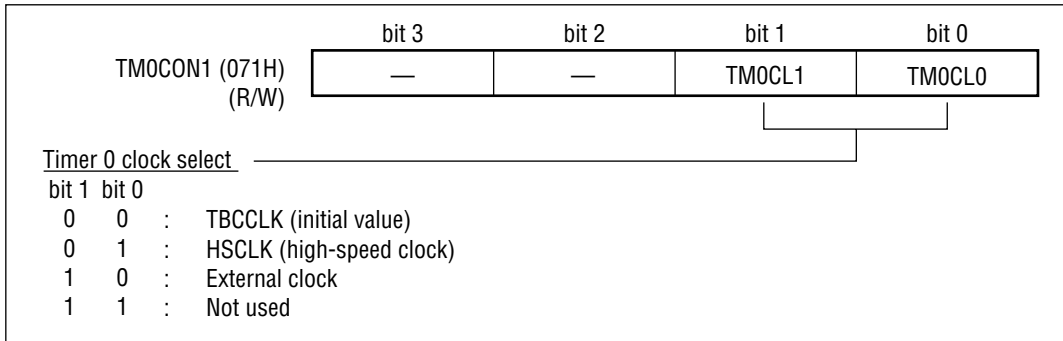
bit 1, 0: TM0CL1, TM0CL0

These bits select the timer 0 clock.

The timer 0 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), or external clock (T02CK: secondary function of PB.2).

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⚠ Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using crystal oscillation.
- Wait at least 5 ms when using RC oscillation.

Timer 1 Registers

	bit 3	bit 2	bit 1	bit 0
TM1CON0 (072H) (R/W)	—	—	TM1ECAP	TM1RUN

Timer 1 mode select

bit 1	bit 0		
0	0	:	Auto-reload mode stop or 16-bit timer mode (initial value)
0	1	:	Auto-reload mode operation
1	0	:	Capture mode stop
1	1	:	Capture mode operation
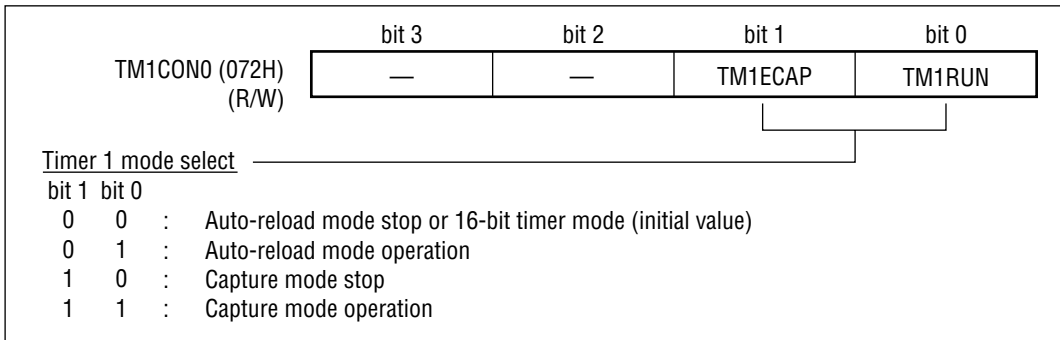
bit 1, 0: TM1ECAP, TM1RUN

These bits select the timer 1 operation mode.

The timer 1 operation mode can be selected as auto-reload mode, capture mode, or 16-bit timer mode.

	bit 3	bit 2	bit 1	bit 0
TM1CON1 (073H) (R/W)	—	—	TM1CL1	TM1CL0

Timer 1 clock select

bit 1	bit 0		
0	0	:	TBCCLK (initial value)
0	1	:	HSCLK
1	0	:	External clock
1	1	:	Timer 0 overflow (16-bit timer mode)
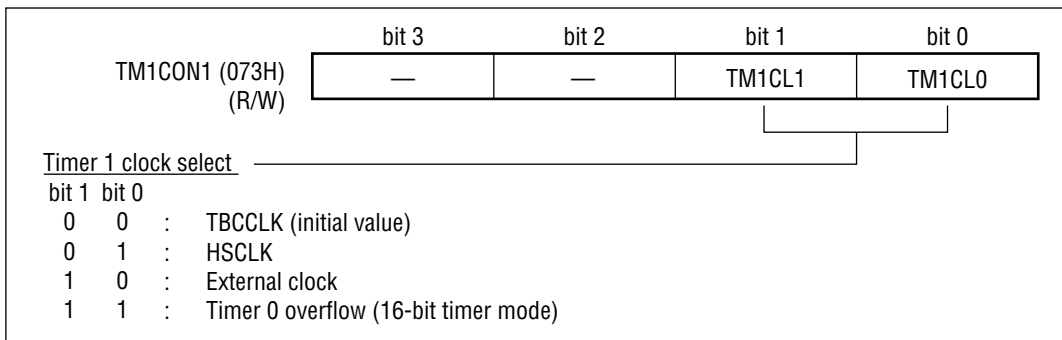
bit 1, 0: TM1CL1, TM1CL0

These bits select the timer 1 clock.

The timer 1 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), external clock (T13CK: secondary function of PB.2), or the timer 0 overflow flag.

When using as a 16-bit timer, select timer 0 overflow for the clock.

⚠ Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using crystal oscillation.
- Wait at least 5 ms when using RC oscillation.

Timer 2 Registers

To use timer 3 in combination as a 16-bit timer, set timer 3 control registers TM3CON0 and TM3CON1.

	bit 3	bit 2	bit 1	bit 0
TM2CON0 (07EH) (R/W)	—	FMEAS2	—	TM2RUN

Timer 2 mode select

bit 2	bit 0		
0	0	:	Auto-reload mode stop (initial value)
0	1	:	Auto-reload mode operation
1	0	:	Frequency measurement mode operation
1	1	:	Not used
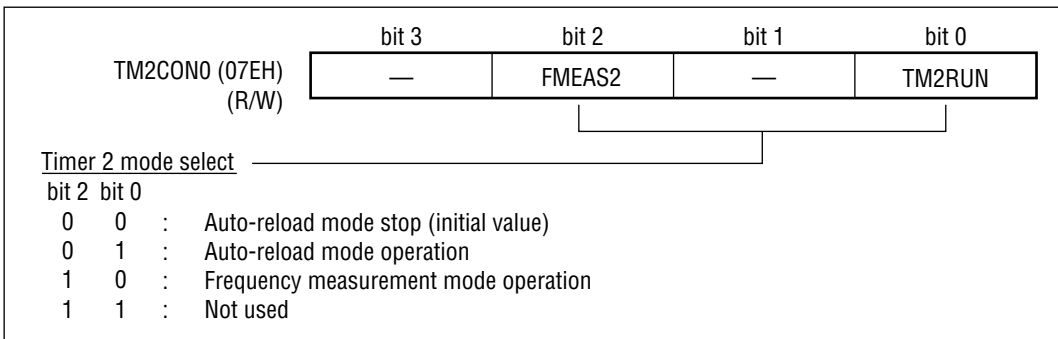
bit 2, 0: FMEAS2, TM2RUN

These bits select the timer 2 operation mode.

The timer 2 operation mode can be selected as auto-reload mode or frequency measurement mode.

	bit 3	bit 2	bit 1	bit 0
TM2CON1 (07FH) (R/W)	—	—	TM2CL1	TM2CL0

Timer 2 clock select

bit 1	bit 0		
0	0	:	TBCCLK (initial value)
0	1	:	HSCLK
1	0	:	External clock
1	1	:	Not used
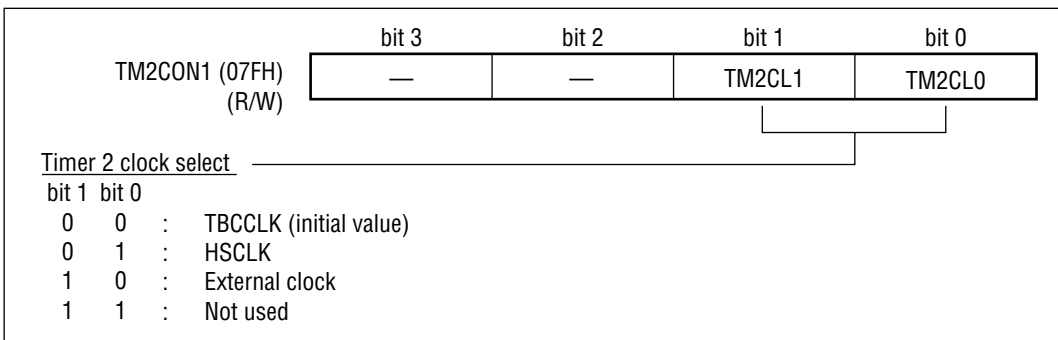
bit 1, 0: TM2CL1, TM2CL0

These bits select the timer 2 clock.

The timer 2 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), or external clock (T02CK: secondary function of PB.2).

⚠ Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using crystal oscillation.
- Wait at least 5 ms when using RC oscillation.

Timer 3 Registers

	bit 3	bit 2	bit 1	bit 0
TM3CON0 (080H) (R/W)	—	—	—	TM3RUN

Timer 3 mode select
  0 : Auto-reload mode stop or 16-bit timer mode (initial value)
  1 : Auto-reload mode operation
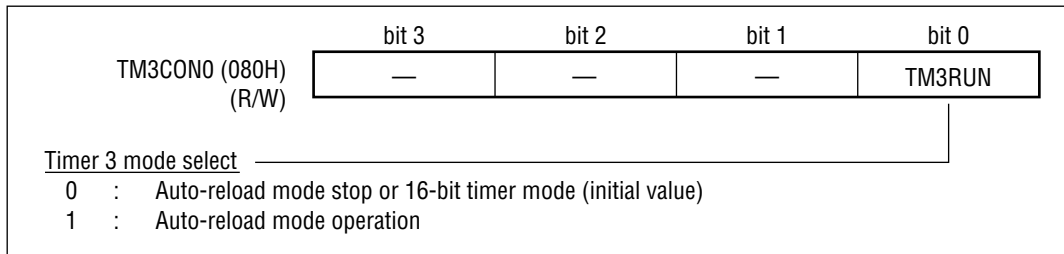
  bit 0: TM3RUN

  This bit selects the timer 3 operation mode.

  The timer 3 operation mode can be selected as auto-reload mode or 16-bit timer mode.

	bit 3	bit 2	bit 1	bit 0
TM3CON1 (081H) (R/W)	—	—	TM3CL1	TM3CL0

Timer 3 clock select
bit 1 bit 0
  0   0   :   TBCCLK (initial value)
  0   1   :   HSCLK
  1   0   :   External clock
  1   1   :   Timer 2 overflow (16-bit timer mode)
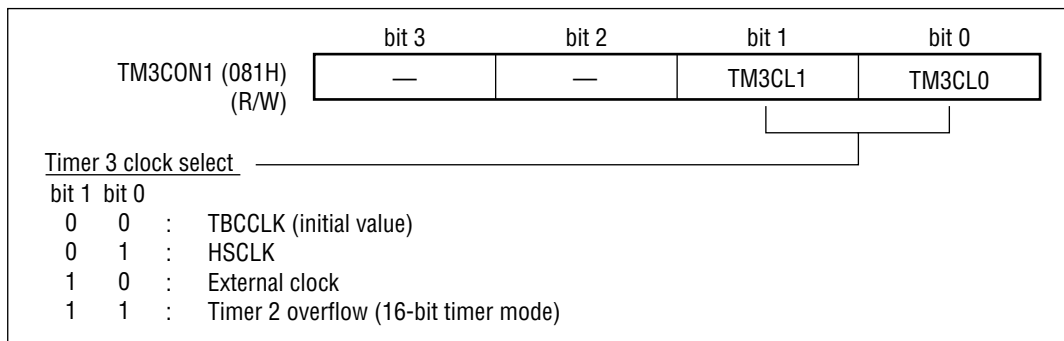
  bit 1, 0: TM3CL1, TM3CL0

  These bits select the timer 3 clock.

  The timer 3 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), external clock (T13CK: secondary function of PB.3), or the timer 2 overflow flag.

  When using as a 16-bit timer, select timer 2 overflow for the clock.

⚠ Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

  • Wait at least 10 ms when using crystal oscillation.
  • Wait at least 5 ms when using RC oscillation.

(4) Timer status registers (TM0STAT, TM1STAT, TM2STAT, TM3STAT)

- Timer status registers read the status of each timer.
- At system reset, all valid bits are cleared to "0".

Timer 0 Registers

	bit 3	bit 2	bit 1	bit 0
TM0STAT (074H) (R)	—	—	TM0CAP	TM0OVF

Timer 0 capture flag
 0: No new capture data (initial value)
 1: New capture data

Timer 0 overflow flag
 0: Initial value
 1: Toggles between 0 and 1 each time the timer 0 counter register overflows.
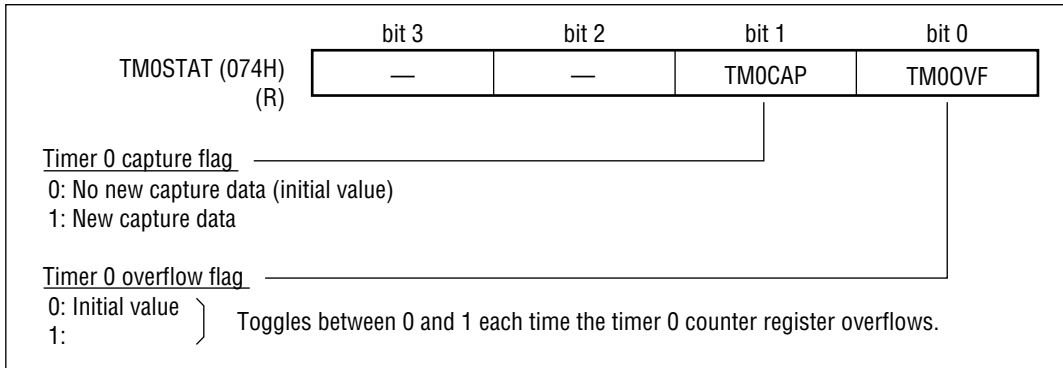
bit 1: TM0CAP (TiMer0 CAPture)

This bit indicates whether or not new capture data is present.
When TM0CAP = "0":
  A value of "0" indicates that there has been no new capture data since system reset or since the last time TM0CAP was read.
When TM0CAP = "1":
  A value of "1" indicates that there is new capture data since system reset or since the last time TM0CAP was read. Additional captures are disabled.
At system reset, TM0CAP is cleared to "0".
In the capture mode, if the level of the capture input pin (PB.0/TM0CAP) changes and a capture is generated, TM0CAP is automatically set to "1".
If TM0STAT is read, TM0CAP is automatically cleared to "0".

bit 0: TM0OVF (TiMer0 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM0OVF is cleared to "0".

Timer 1 Registers

	bit 3	bit 2	bit 1	bit 0
TM1STAT (075H) (R)	—	—	TM1CAP	TM1OVF

Timer 1 capture flag
 0: No new capture data (initial value)
 1: New capture data

Timer 1 overflow flag
 0: Initial value
 1: Toggles between 0 and 1 each time the timer 1 counter register overflows.
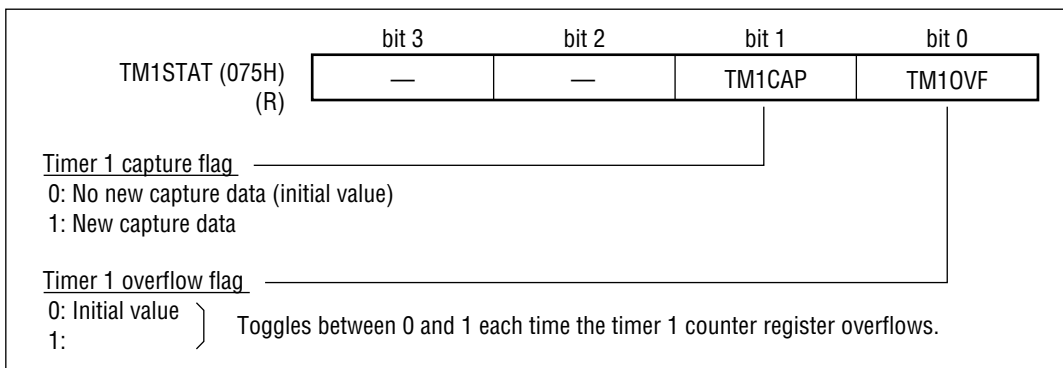
bit 1: TM1CAP (TiMer1 CAPture)

> This bit indicates whether or not new capture data is present.
> When TM1CAP = "0":
>> A value of "0" indicates that there has been no new capture data since
>> system reset or since the last time TM1CAP was read.
> When TM1CAP = "1":
>> A value of "1" indicates that there is new capture data since system reset
>> or since the last time TM0CAP was read. Additional captures are disabled.
> At system reset, TM1CAP is cleared to "0".
> In the capture mode, if the level of the capture input pin (PB.1/TM1CAP)
> changes and a capture is generated, TM1CAP is automatically set to "1".
> If TM1STAT is read, TM1CAP is automatically cleared to "0".

bit 0: TM1OVF (TiMer1 OVerFlow)

> This bit indicates that the timer counter register has overflowed.
> This bit toggles between "0" and "1" whenever overflow occurs.
> At system reset, TM1OVF is cleared to "0".

Timer 2 Register

	bit 3	bit 2	bit 1	bit 0
TM2STAT (082H) (R)	—	—	—	TM2OVF

Timer 2 overflow flag
0: Initial value
1: } Toggles between 0 and 1 each time the timer 2 counter register overflows.
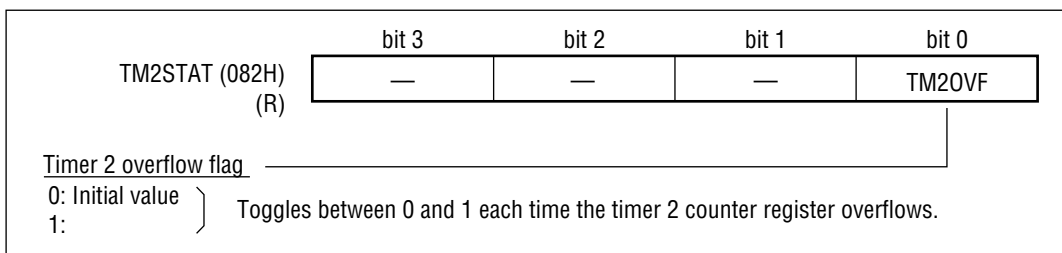
bit 0: TM2OVF (TiMer2 OVerFlow)

> This bit indicates that the timer counter register has overflowed.
> This bit toggles between "0" and "1" whenever overflow occurs.
> At system reset, TM2OVF is cleared to "0".

Timer 3 Register

	bit 3	bit 2	bit 1	bit 0
TM3STAT (083H) (R)	—	—	—	TM3OVF

Timer 3 overflow flag
0: Initial value
1: } Toggles between 0 and 1 each time the timer 3 counter register overflows.
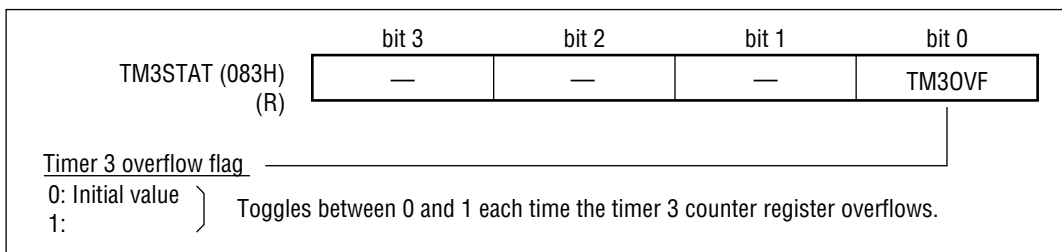
bit 0: TM3OVF (TiMer3 OVerFlow)

> This bit indicates that the timer counter register has overflowed.
> This bit toggles between "0" and "1" whenever overflow occurs.
> At system reset, TM3OVF is cleared to "0".

[Supplement] List of Timer Registers

Timer 0 Registers

Name	Symbol	Address	R/W	Initial value
Timer 0 data register L	TM0DL	068H	R/W	0H
Timer 0 data register H	TM0DH	069H		0H
Timer 0 counter register L	TM0CL	06CH	R/W	0H
Timer 0 counter register H	TM0CH	06DH		0H
Timer 0 control register 0	TM0CON0	070H	R/W	8H
Timer 0 control register 1	TM0CON1	071H		0CH
Timer 0 status register	TM0STAT	074H	R	0CH

Timer 1 Registers

Name	Symbol	Address	R/W	Initial value
Timer 1 data register L	TM1DL	06AH	R/W	0H
Timer 1 data register H	TM1DH	06BH		0H
Timer 1 counter register L	TM1CL	06EH	R/W	0H
Timer 1 counter register H	TM1CH	06FH		0H
Timer 1 control register 0	TM1CON0	072H	R/W	0CH
Timer 1 control register 1	TM1CON1	073H		0CH
Timer 1 status register	TM1STAT	075H	R	0CH

Timer 2 Registers

Name	Symbol	Address	R/W	Initial value
Timer 2 data register L	TM2DL	076H	R/W	0H
Timer 2 data register H	TM2DH	077H		0H
Timer 2 counter register L	TM2CL	07AH	R/W	0H
Timer 2 counter register H	TM2CH	07BH		0H
Timer 2 control register 0	TM2CON0	07EH	R/W	0AH
Timer 2 control register 1	TM2CON1	07FH		0CH
Timer 2 status register	TM2STAT	082H	R	0EH

Timer 3 Registers

Name	Symbol	Address	R/W	Initial value
Timer 3 data register L	TM3DL	078H	R/W	0H
Timer 3 data register H	TM3DH	079H		0H
Timer 3 counter register L	TM3CL	07CH	R/W	0H
Timer 3 counter register H	TM3CH	07DH		0H
Timer 3 control register 0	TM3CON0	080H	R/W	0EH
Timer 3 control register 1	TM3CON1	081H		0CH
Timer 3 status register	TM3STAT	083H	R	0EH

7

7.4 Timer Operation

7.4.1 Timer Clock

The timer clock can be selected as TBCCLK (low-speed clock: 32.768 kHz), HSCLK (high-speed clock), or an external clock. By using timer 0 and timer 2 overflow signals as clocks for timer 1 and timer 3, respectively, the timers can be used in pairs as 16-bit timers.

If the high-speed clock (HSCLK) is to be used, after setting bit 1 (ENOSC) of the frequency control register (FCON), wait at least 10 ms in the crystal oscillation mode or 5 ms in the RC oscillation mode before operating the timer.

The external clock is input to a port assigned as a secondary function port. In the case of timers 0 and 2, PB.2/T02CK is used as the input pin for the external clock. In the case of timers 1 and 3, PB.3/T13CK is used as the input pin for the external clock. Since the external clock is sampled by the system clock (CLK), the high- and low-levels of the external clock should be longer than 1 cycle of the system clock (CLK).

7.4.2 Timer Data Registers

TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL and TM3DH are 4-bit registers.

In the auto-reload mode, the timer data registers save values that are reloaded into the timer counter registers when the timer counter registers overflow.

In the capture mode, the timer data registers save the value of the timer counter registers when a capture signal is input. Each timer data register can be read/written by software. Writing to timer data registers does not change the contents of the timer counter registers.

7.4.3 Timer Counter Registers

TM0CL and TM0CH, TM1CL and TM1CH, TM2CL and TM2CH, and TM3CL and TM3CH are 8-bit binary counters that are incremented at the falling edge of the timer clock.

Each timer counter register can be read/written by software. However, if the CPU clock and timer clock are different, values that are read or written during the count operation cannot be guaranteed. If an external clock is used as the timer clock, reading/writing is always possible.

When a value is written to any timer counter register, the same value is also written to the corresponding timer data register.

7.4.4 Timer Interrupt Requests and Overflow Flags

Timers generate timer interrupt requests when the timer counter register overflows. The overflow flag toggles between "1" and "0" at each overflow. The output of the overflow flag of timers 0 and 1 can be output to secondary port functions PB.0/TM0OVF and PB.1/TM1OVF pins.

Figure 7-5 indicates the operation timing for timer counter register overflow. Table 7-1 lists timer interrupts.
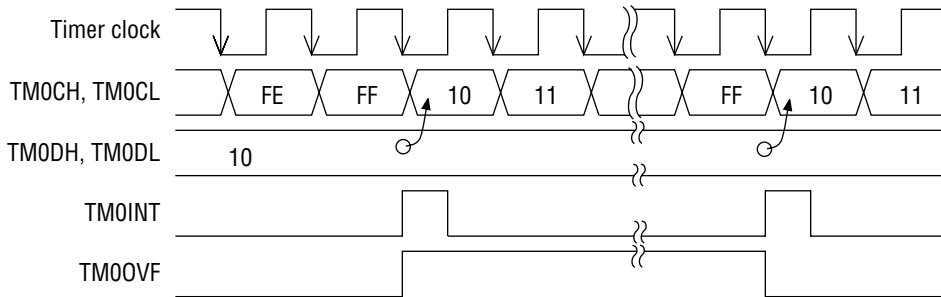
Figure 7-5 Timer Counter Register Overflow Timing (for Timer 0)

Table 7-1 List of Timer Interrupts

Interrupt factor	Symbol	IRQ flag (IRQ2)	IE flag (IE2)	Interrupt vector address
Timer 0 interrupt	TM0INT	QTM0	ETM0	0020H
Timer 1 interrupt	TM1INT	QTM1	ETM1	0022H
Timer 2 interrupt	TM2INT	QTM2	ETM2	0024H
Timer 3 interrupt	TM3INT	QTM3	ETM3	0026H

When the master interrupt enable flag (MIE) is set to "1" with the interrupt enable flags (ETM0–3) set to "1", and a timer overflow occurs, a CPU interrupt request is generated.

7.4.5 Auto-Reload Mode Operation

Timers 0 to 3 can be used as auto-reload mode timers. The setup method is as follows.

- Timer 0: Set FMEAS0 (bit 2 of TM0CON0) to "0", and set TM0ECAP (bit 1 of TM0CON0) to "0".
- Timer 1: Set TM1ECAP (bit 1 of TM1CON0) to "0".
- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "0".
- Timer 3: No setup needed.

In the auto-reload mode, each time the timer counter register overflows, the timer data register value is reloaded into the timer counter register, and counting begins from the value. Setting the RUN bits (TM0RUN, TM1RUN, TM2RUN, TM3RUN) for each timer control register to "1" will restart the count, and resetting to "0" stops the count.

In the 16-bit timer mode for timers 0 and 1 the TM1RUN bit is disabled, and start/stop is controlled with the TM0RUN bit. In the 16-bit timer mode for timers 2 and 3 the TM3RUN bit is disabled, and start/stop is controlled with the TM2RUN bit.

Figure 7-6 shows auto-reload mode timing for pulse generation when timers 0 and 1 are used as a 16-bit timer.
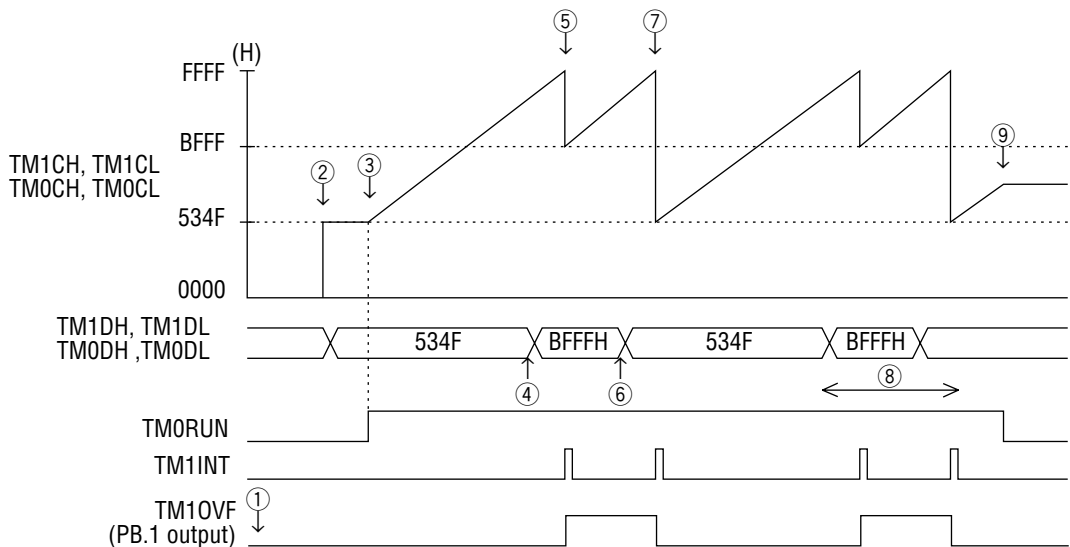
Figure 7-6 Auto-Reload Mode Timing

The operation procedures are as follows.

① Set PB.1 to the output mode (TM1OVF) secondary function.

② Write 534FH to the timer data and timer counter registers.
TM1DH = TM1CH = 5H   (bits 15–12)
TM1DL = TM1CL = 3H   (bits 11–8)
TM0DH = TM0CH = 4H   (bits 7–4)
TM0DL = TM0CL = FH   (bits 3–0)

③ If TM0CON and TM1CON are set to auto-reload mode and TM0RUN is set to "1", the timer counter register will start to count from 534FH.

④ Before the timer counter register overflows, write the next reload value BFFFH to the timer data register.

⑤ When the timer counter register overflows, BFFFH is set to the timer counter register, timer interrupt TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register continues to count up from BFFFH.

⑥ Before the timer counter register overflows, write the next reload value 534FH to the timer data register.

⑦ When the timer counter register overflows, 534FH is set to the timer counter register, timer interrupt TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register resumes counting from address 534FH.

⑧ Repeat steps 4 through 7. This allows a user-defined pulse to be output from PB.1/TM1OVF.

⑨ Halt the count by resetting TM0RUN to "0".

Figure 7-7 shows TM0RUN count start/halt timing.
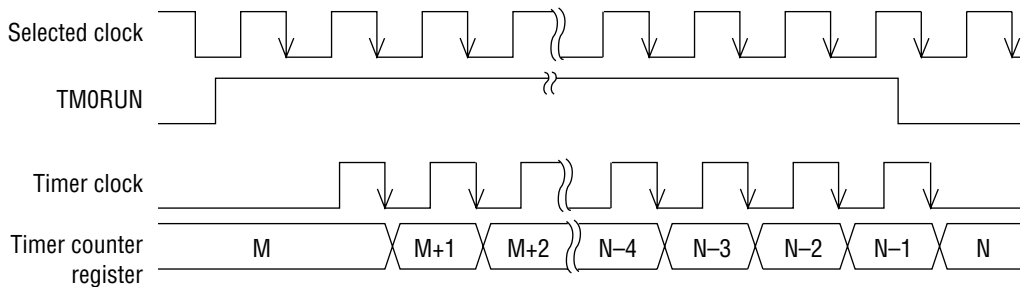
Figure 7-7 TM0RUN Count Start/Halt Timing

When TM0RUN is set to "1", the timer counter starts to count from the second falling edge of the selected clock. When TM0RUN is reset to "0", the counter stops counting at the falling edge of the selected clock which appears immediately after the TM0RUN falling edge.

7.4.6 Capture Mode Operation

Timer 0 and timer 1 can be used as capture mode timers.

In a capture operation, a change in the capture input (PB.0/TM0CAP, PB.1/TM1CAP) level during operation of the timer counter register triggers loading of the value of the timer counter register into the timer data register.

Methods to set the capture mode for each timer are listed below.

  - Timer 0: Set TM0ECAP (bit 1 of TM0CON0) to "1", and set FMEAS0 (bit 2 of TM0CON0) to "0".

  - Timer 1: Set TM1ECAP (bit 1 of TM1CON0) to "1".

In the capture mode, reloading the timer data register data into the timer counter register is inhibited, and when the timer counter register overflows, counting is restarted from 00H.

When a capture occurs, the capture flags (TM0CAP, TM1CAP) of the timer status registers (TM0STAT, TM1STAT) are set to "1". Additional captures are disabled while the capture flags are "1". The capture flags are assigned to bit 0 of the timer status registers, and are automatically cleared to "0" when the timer status registers are read.

If both the TM1CL1 and TM1CL0 bits of the timer 1 control register 1 (TM1CON1) are set to "1" and timer 0 overflow is selected as the clock, the 16-bit capture mode will be set. In this case, the PB.0/TM0CAP pin is the capture trigger input.

Figure 7-8 shows the timer 0 capture mode timing for pulse width measurement.
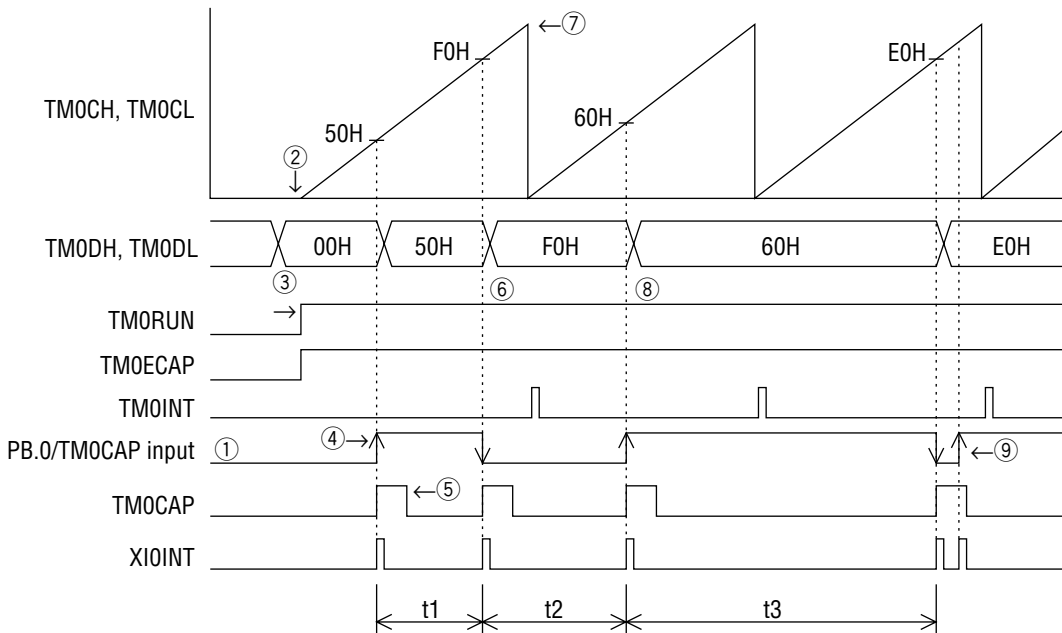
Figure 7-8 Capture Mode Timing

The operation procedure is listed below.

① Set PB.0/TM0CAP to input mode, and enable XI0INT and TM0INT.

② Clear all bits of the timer counter registers and timer data registers to zero.

③ Set TM0CON0 to the capture mode, and set TM0RUN to "1" to begin upward counting.

④ If the PB.0/TM0CAP input changes, the TM0CH/TM0CL value is captured by TM0DH/TM0DL and TM0CAP is set to "1" (first capture). The CPU detects this through XI0INT and reads the values of TM0DH/TM0DL.

⑤ After the TM0DH/TM0DL read is complete, TM0CAP is cleared to "0" to wait for the next capture.

⑥ If the PB.0/TM0CAP input changes, repeat operations ④ and ⑤ (second capture).

The high-level pulse width t1 of the PB.0 input can be determined as follows.

$$t1 = (F0H - 50H) \times t_{CLK} \qquad t_{CLK}: \text{TMCLK cycle}$$

⑦ TM0INT is generated when the timer counter register overflows. When overflow occurs, the timer counter register changes from FFH to 00H and continues upward counting.

⑧ If the PB.0/TM0CAP input changes, repeat operations ④ and ⑤ (third capture). Because the counter overflows once during the interval between the second capture and the third capture, the low-level pulse width t2 of the PB.0 input can be determined as follows.

$$t2 = (60H - F0H + 100H) \times t_{CLK}$$

⑨ While TM0CAP = "1", there is no capture even when PB.0/TM0CAP changes.

Figure 7-9 shows the capture timing and Figure 7-10 shows the capture signal (CAPT) generator circuit.
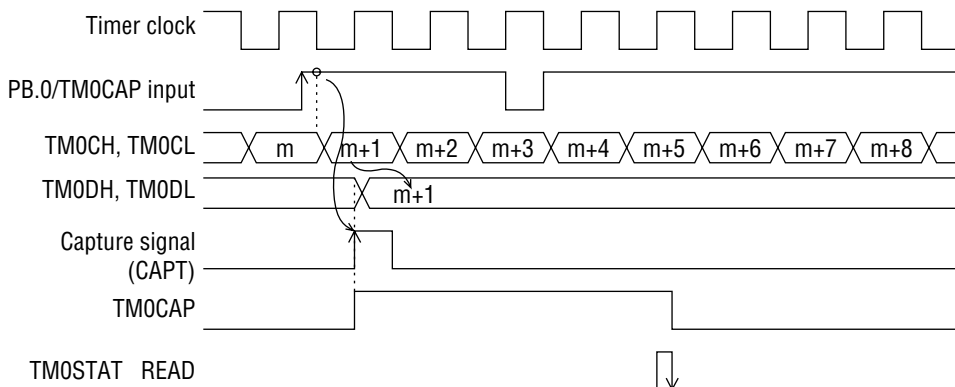
Figure 7-9 Capture Timing
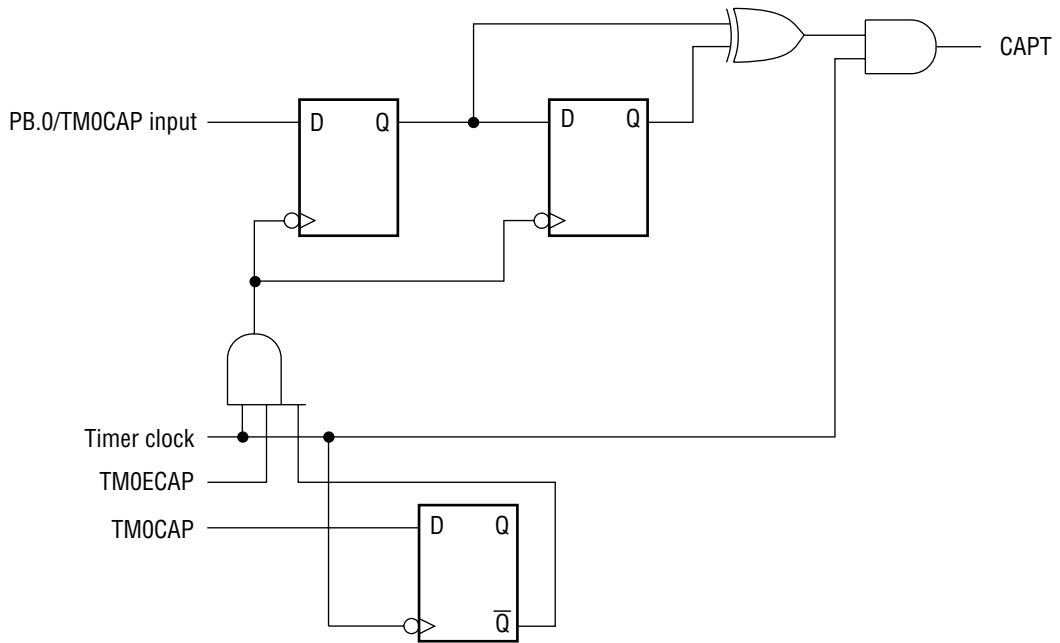
Figure 7-10 Capture Signal (CAPT) Generator Circuit

⚠ Note:

The maximum delay from a PB.0/TM0CAP input level change until capture is one cycle of the timer clock.

7.4.7 Frequency Measurement Mode Operation

The frequency measurement mode is used to measure the frequency of the RC oscillator clock, which has wide product variation.

Timers 0 and 1, and timers 2 and 3 can be used in the frequency measurement mode. These timers are set as follows for the frequency measurement mode:

- Timer 0: Set FMEAS0 (bit 2 of TM0CON0) to "1", and set TM0ECAP (bit 1 of TM0CON0) and TM0RUN (bit 0 of TM0CON0) to "0".
- Timer 1: Set TM1ECAP (bit 1 of TM1CON0) and TM1RUN (bit 0 of TM1CON0) to "0".
- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "1", and set TM2RUN (bit 0 of TM2CON0) to "0".
- Timer 3: Set TM3RUN (bit 0 of TM3CON0) to "0".

Figure 7-11 indicates frequency measurement mode timing when timers 2 and 3 are used as a 16-bit timer.
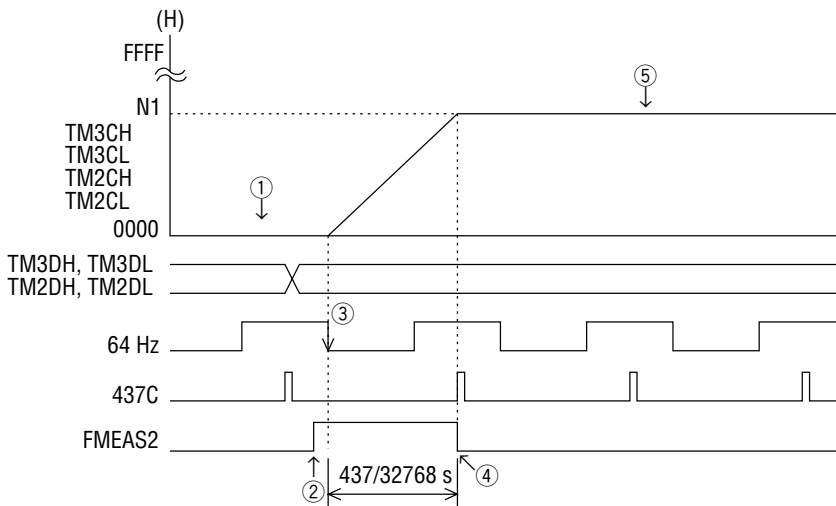
Figure 7-11 Frequency Measurement Mode Timing

The operation sequence for Figure 7-11 is as follows.

① Timer 3 control registers 0 and 1 (TM3CON0, TM3CON1) are set for 16-bit timer mode, and the timer counter and timer data register are cleared to "0". Enable the high-speed clock by the frequency control register (FCON) and the timer clock is set to HSCLK.

② Wait 10 ms or more in the crystal oscillation mode or 5 ms or more in the RC oscillation mode after starting the high-speed clock and set FMEAS2 to "1" to enter the frequency measurement mode.

③ When FMEAS2 is "1", the counter starts at the 64 Hz falling edge.

④ When the 437C signal is "1", FMEAS2 is reset to "0", and the counter stops at the falling edge of the next clock. The 437C signal is a pulse signal which rises in 437/32768 seconds after the 64 Hz falling edge.

⑤ Timer counter register value N1 is read.

Assuming that the ceramic oscillation clock is exactly 2 MHz, value N1 read from the timer counter register is:

$$N1 = 2000000 \times 437/32768$$
$$= 26672 \text{ (decimal)}$$
$$= 6380 \text{ (hexadecimal)}$$
$$= 0110\ 1000\ \underline{0011\ 0000}\ \text{(binary)}$$
$$\text{(truncated)}$$

Because 437/32768 seconds are equivalent to 128 clocks at 9600 Hz (more precisely, 9598 Hz), a division of the count by 128 provides the frequency ratio (N2) between 2 MHz and 9600 Hz. Because $128 = 2^7$, that can be determined by merely truncating the righthand seven digits of N1 (binary), yielding.

$$N2 = 26672/128 = 011010000 \text{ (binary)}$$
$$= D0 \text{ (hexadecimal)}$$
$$= 208 \text{ (decimal)}$$

This indicates that 9600 Hz is about 208 times the cycle of 2 MHz, which means that the timer data register should be set to FF30H so that the counter overflows every 208 counts of the 2 MHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/2000000 \times 208 = 0.104 \text{ ms (9615 Hz)}$$

In the same way, assuming that RC oscillation clock is 600 kHz due to manufacturing variation, we get

$$N1 = 600000 \times 437/32768 = 8001 \text{ (decimal)}$$
$$= 1F41 \text{ (hexadecimal)}$$
$$= 0001\ 1111\ \underline{0100\ 0001}\ \text{(binary)}$$
$$\text{(truncated)}$$

Truncating the righthand seven digits of N1 (binary), we get

$$N2 = 8001/128 = 000111110 \text{ (binary)}$$
$$= 3E \text{ (hexadecimal)}$$
$$= 62 \text{ (decimal)}$$

Set the timer data register to FFC2H so that the counter overflows every 62 counts of the 600 kHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/600000 \times 62 = 0.10333 \text{ ms (9677 Hz)}$$

In this way the frequency measurement mode can be applied to generate TM3INT signals with precision cycles.

Figure 7-12 illustrates the operation of timer 3 interrupt for an RC oscillator clock frequency of 600 kHz.
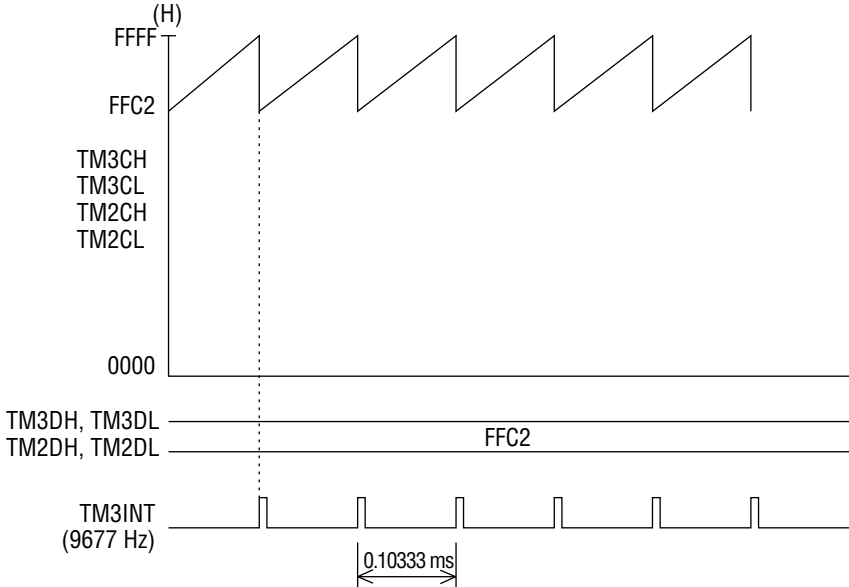
Figure 7-12 Timer 3 Interrupt (TM3INT) Generation

100 Hz Timer Counter (100HzTC)

Chapter 8 100 Hz Timer Counter (100HzTC)

8.1 Overview

The 100 Hz timer counter has a circuit that divides the TBC6 output (512 Hz) of the time base counter to generate a 10 Hz interrupt. The 100 Hz timer consists of a 5/6-base counter and two decimal counters.

8.2 100 Hz Timer Counter Configuration

Figure 8-1 indicates the configuration of the 100 Hz timer counter.
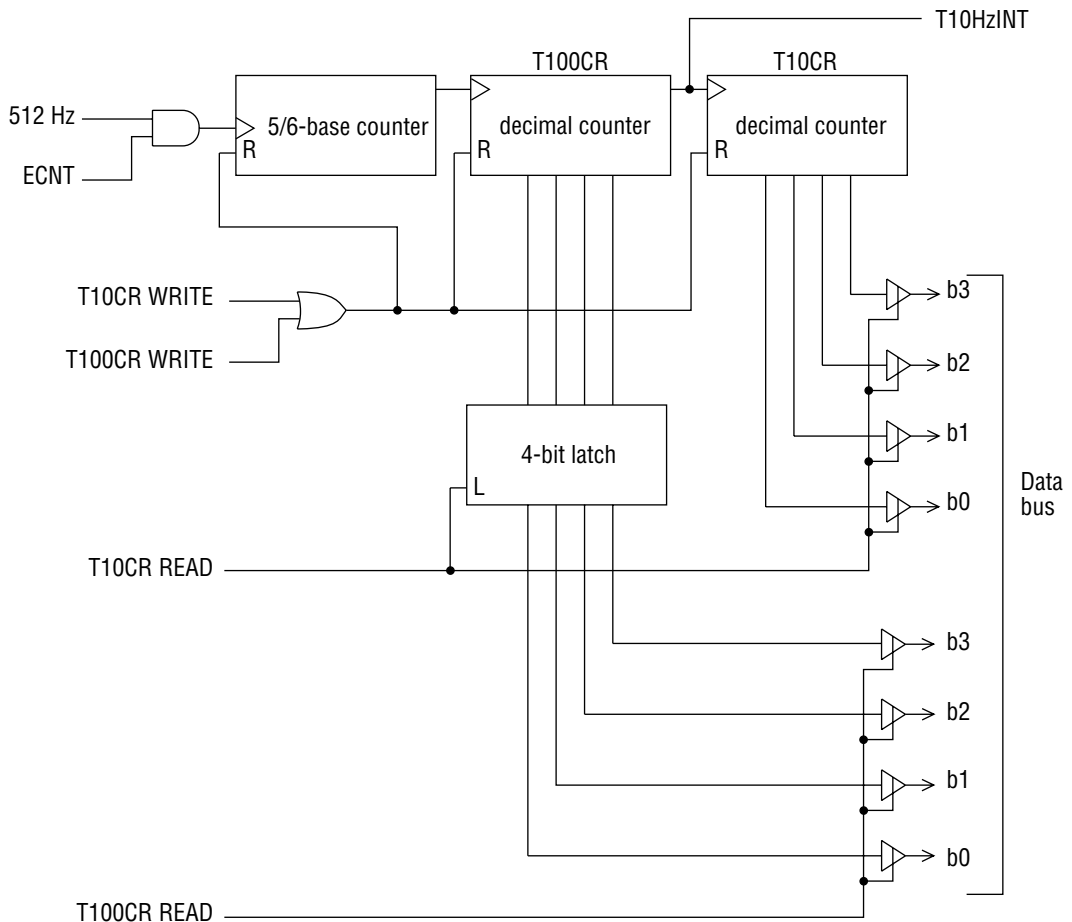
Figure 8-1 100 Hz Timer Counter Configuration

8.3 100 Hz Timer Counter Registers

(1) 100 Hz timer counter control register (T100CON)

This is a 4-bit special function register (SFR) controlling the 100 Hz timer counter.

	bit 3	bit 2	bit 1	bit 0
T100CON (066H) (R/W)	—	—	—	ECNT

Count start/stop select
 0 : Count stop (initial value)
 1 : Count start
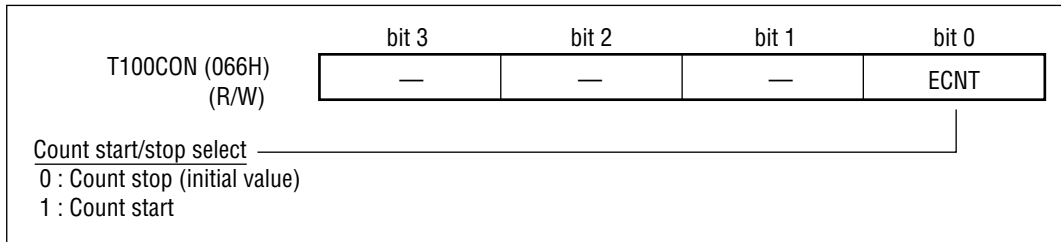
> bit 0: ECNT
>
>> This bit controls count start/stop for the 100 Hz timer counter internal counter. Count starts when set to "1". At system reset the value is reset to "0" and counting is stopped.

(2) 100 Hz counter register (T100CR)

This is a 4-bit special function register (SFR) to read the 100 Hz counter of the 100 Hz timer counter. The content of the T100CR is latched by a 4-bit latch in T10CR read operation, so the value of the T100CR must always be read after reading T10CR.

When data is written in T100CR, both T100CR and T10CR are reset to "0".

	bit 3	bit 2	bit 1	bit 0
T100CR (064H) (R/W)	100C3	100C2	100C1	100C0
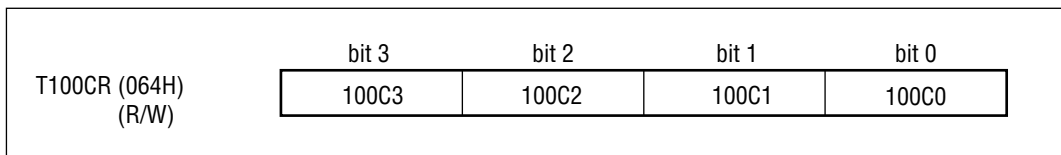
(3) 10 Hz counter register (T10CR)

A 4-bit special function register (SFR) to read the 10 Hz counter in the 100 Hz timer counter.

When data is written in T10CR, both T100CR and T10CR are reset to "0".

	bit 3	bit 2	bit 1	bit 0
T10CR (065H) (R/W)	10C3	10C2	10C1	10C0
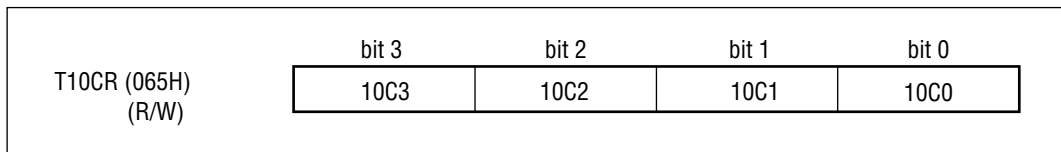
8.4 100 Hz Timer Counter Operation

The 100 Hz timer counter begins counting when bit 0 (ECNT) of the 100 Hz timer counter control register (T100CON) is set to "1". The 512 Hz output of the time base counter is divided into 100 Hz by the 5/6-base counter.

The 100 Hz signal is input to the 100 Hz counter (T100CR) and the carry output of that counter is input to the 10 Hz counter (T10CR). The 10HzINT signal, which is the carry output (10 Hz) of the T100CR 100 Hz counter also generates an interrupt request, setting bit 3 (Q10Hz) of interrupt request registers 3 (IRQ3) to "1".

If either T100CR or T10CR is written to, both are reset to "0". The write data used has no significance. For example, the "MOV T100CR, A" instruction is not dependent on the contents of the accumulator.

If T10CR is read, the contents of T100CR at that time are latched to the 4-bit latch. Therefore, the contents of T100CR at the time T10CR is read can be read correctly.

8

Watchdog Timer (WDT)

9

Chapter 9 Watchdog Timer (WDT)

9.1 Overview

The watchdog timer is a circuit to detect CPU malfunction. The WDT consists of a 9-bit watchdog timer counter (WTDC) counting the 256 Hz output of the TBC7 of the time base counter (TBC), and a watchdog timer control register (WDTCON) to start and clear WDTC.

9.2 Watchdog Timer Configuration

Figure 9-1 shows the configuration of the watchdog timer.
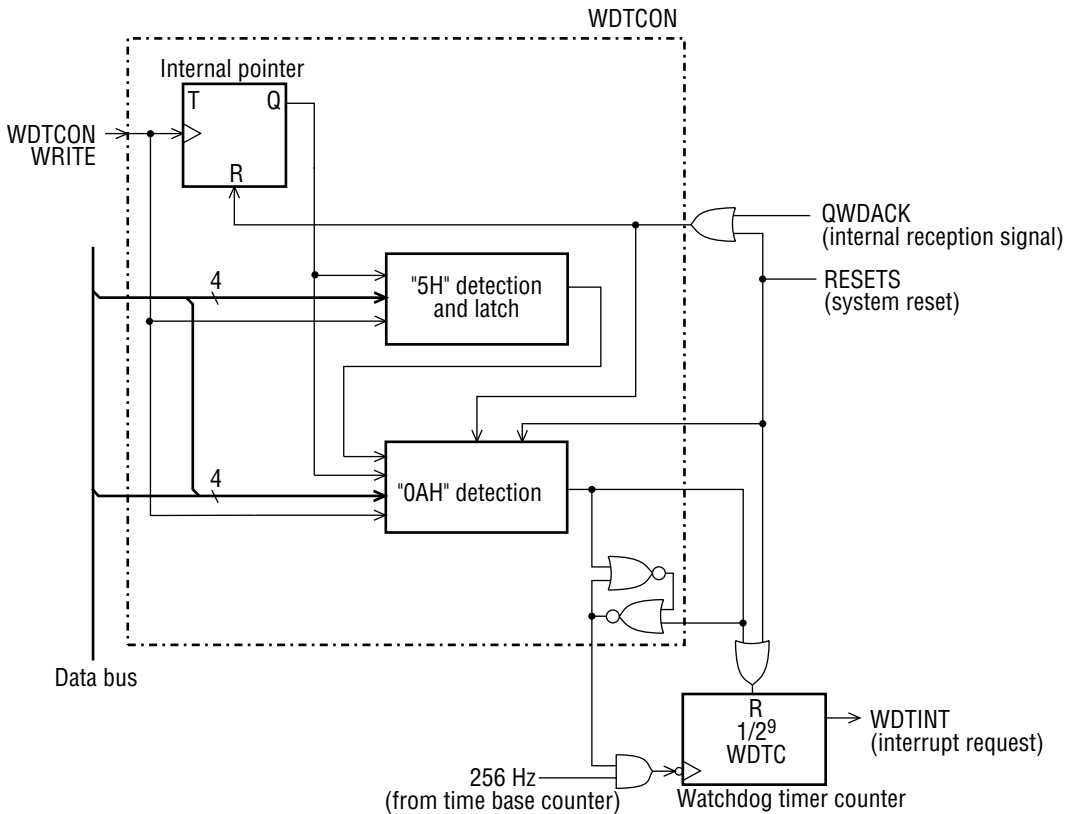
Figure 9-1 Watchdog Timer Configuration

9.3 Watchdog Timer Control Register (WDTCON)

The watchdog timer control register (WDTCON) is a 4-bit write only special function register (SFR) used to start/clear the watchdog timer counter (WDTC).

	bit 3	bit 2	bit 1	bit 0
WDTCON (09FH) (W)	d3	d2	d1	d0
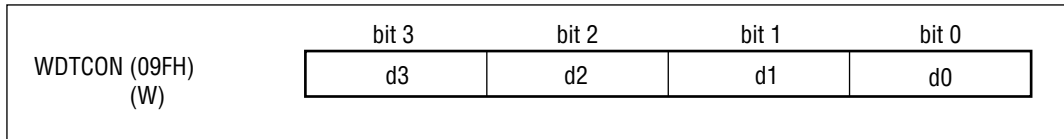
9.4 Watchdog Timer Operation

At system reset, WDTC (watchdog timer counter) stops counting.

WDTC begins counting by writing "5H" to WDTCON (watchdog timer control register) while the internal pointer is "0", and then writing "0AH" (while the internal pointer is "1").

The internal pointer is cleared to "0" at system reset or when WDTC overflows, and toggles every time a write operation to WDTCON is performed.

After WDTC is activated, WDTC is cleared by writing "5H" to WDTCON while the internal pointer is "0", and then writing "0AH" while the internal pointer is "1". When WDTC overflows (1FFH→000H), a watchdog timer interrupt request (WDTINT) is generated. WDTINT cannot be disabled by the software (non-maskable interrupt) and has the highest level of interrupt priority.

The WDTC overflow cycle (T) is given by:

$$T = \frac{128 \times 512}{32768 \text{ (Hz)}} = 2 \text{ s}$$

The minus deviation (t) of the WDTC overflow cycle is given by:

$$t = \frac{128}{32768 \text{ (Hz)}} = \text{approximately 3.9 ms}$$

Therefore, the WDTC clear cycle (Ct) can be computed as follows.

$$Ct = T - t = 2 \text{ s} - 3.9 \text{ ms} = 1.9961 \text{ s}$$

If 32.768 kHz is to be used as the low-speed clock, the software must be programmed to clear WDTC within 1.9961 s.

If the CPU malfunctions due to a power failure or other factor and the WDTC cannot be cleared normally, WDTC will overflow and WDTINT will be generated. Program the watchdog timer interrupt routine to handle recovery operations by returning to the normal routine.

⚠ Note:

The watchdog timer cannot detect all operating faults. If the CPU malfunctions but WDTC can still be cleared, a fault will not be detected.

Figure 9-2 shows a flowchart of watchdog timer processing.
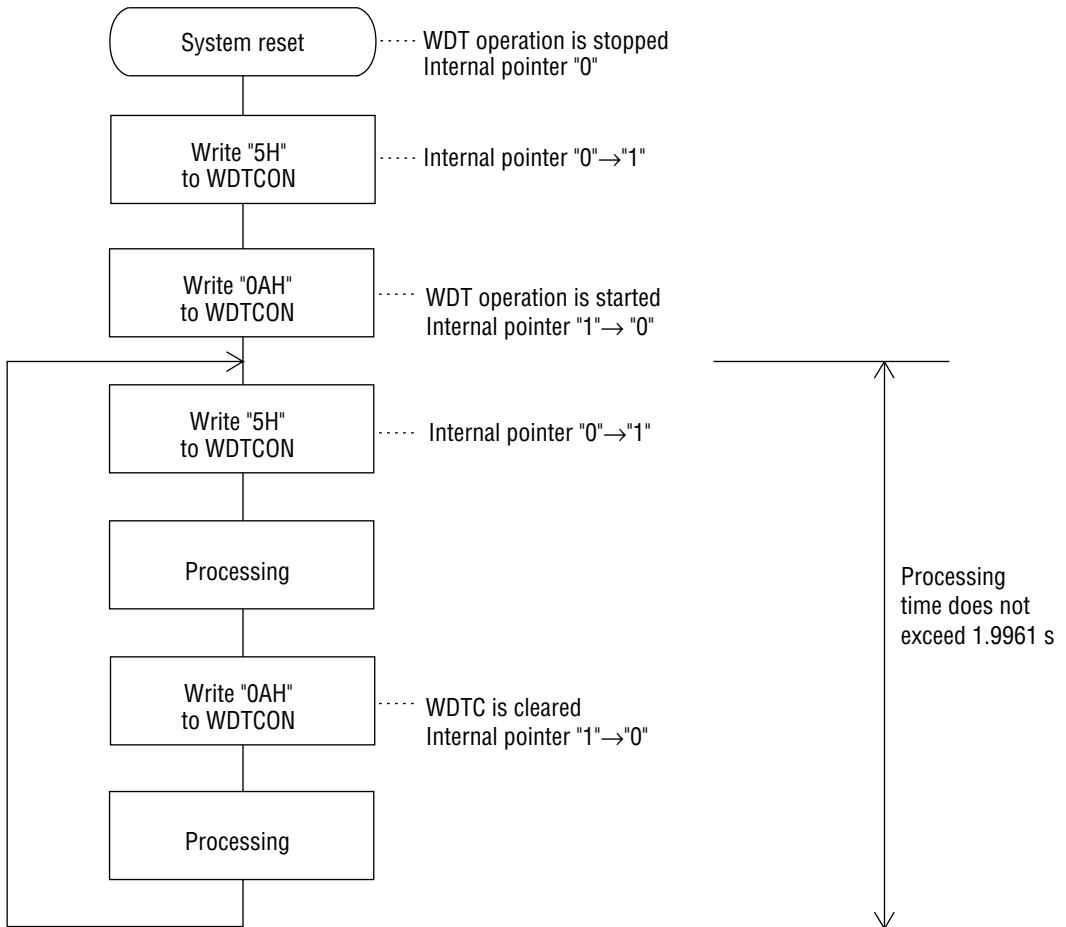
Figure 9-2 Watchdog Timer Processing Flowchart

Figure 9-3 shows the timing chart for watchdog timer operation.
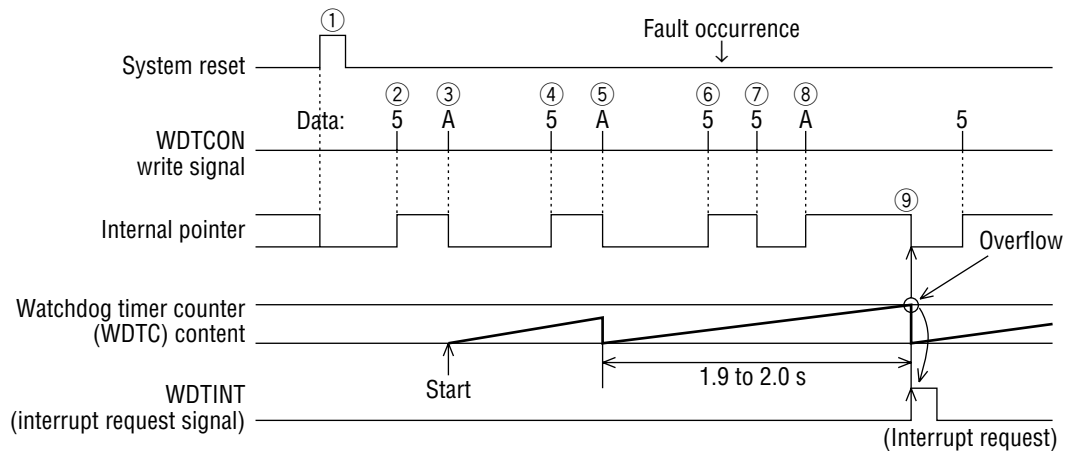
Figure 9-3 Watchdog Timer Operation Timing Chart

The watchdog timer operating sequence is listed below.

① System reset clears the internal pointer and WDTC.

② Write "5H" to WDTCON. (Internal pointer 0→1)

③ Write "0AH" to WDTCON to start WDTC. (Internal pointer 1→0)

④ Write "5H" to WDTCON. (Internal pointer 0→1)

⑤ Write "0AH" to WDTCON to clear WDTC. (Internal pointer 1→0)

⑥ Write "5H" to WDTCON. (Internal pointer 0→1)

⑦ After a fault occurs, "5H" is written to WDTCON but is not accepted since the internal pointer is "1". (Internal pointer 1→0)

⑧ "0AH" is written to WDTCON, but since the internal pointer is "0" and the write of "5H" in step ⑦ was not accepted, WDTC will not be cleared. (Internal pointer 0→1)

⑨ Because WDTC was not cleared, overflow of WDTC will generate the watchdog timer interrupt WDTINT. At this time, the internal pointer is cleared to "0".

Ports (INPUT, OUTPUT, I/O PORT)

Chapter 10 Ports (INPUT, OUTPUT, I/O PORT)

10.1 Overview

The ML63326 has one internal 4-bit input port, four internal 4-bit output ports, five internal 4-bit I/O ports, and one internal 2-bit I/O port.

The V_{DDI} (interface power supply) pin supplies power to the ports.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.

⚠ Note:

Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.

10.2 Ports List

The ports of the ML63326 are shown in Table 10-1.

10

Table 10-1 Ports List

Port	I/O	Interrupt	Sedondary function	Page
Port 0	I	●	●	10-2
Port 4		—	●	10-7
Port 5	0	—	●	10-7
Port 6		—	●	10-7
Port 7		—	●	10-7
Port 8		—	●	10-15
Port 9		—	●	10-15
Port A	I/0	—	●	10-15
Port B		●	●	10-24
Port E		●	●	10-30
Port F		●	●	10-35

10.3 Port 0 (P0.0–P0.3)

10.3.1 Port 0 Configuration

The ML63326 has Port 0, a 4-bit input-only port.

Figure 10-1 shows the configuration of port 0.
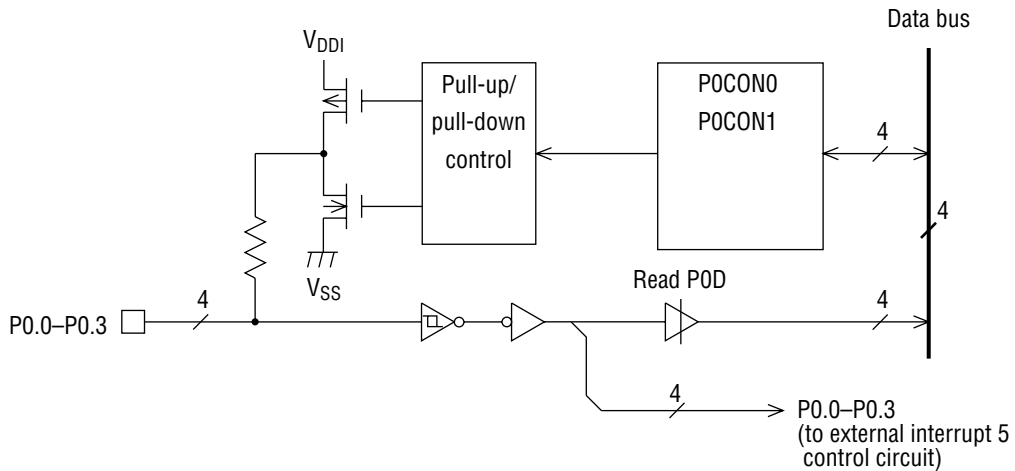
Figure 10-1 Input-Only Port (Port 0) Configuration

10.3.2 Port 0 Registers

(1) Port 0 Data Register (P0D)

The port 0 data register (P0D) is a 4-bit read-only special function register (SFR) used to read the pin levels of each bit of port 0.
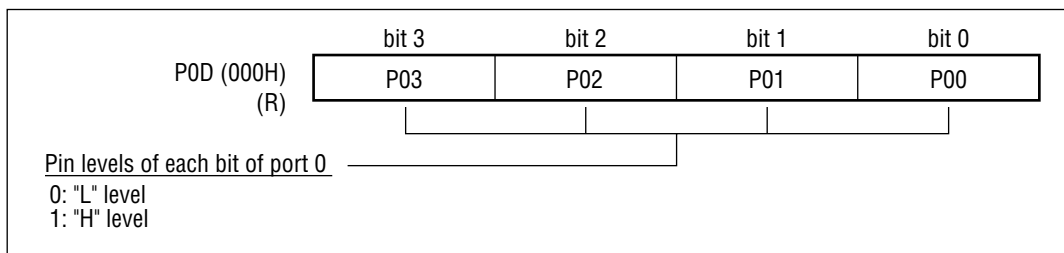
(2) Port Control Registers (P0CON0, P0CON1)

Port 0 control registers 0/1 (P0CON0, P0CON1) are 4-bit special function registers (SFRs) that select pull-up or pull-down resistors and select the external interrupt sampling frequency of Port 0 secondary function.

	bit 3	bit 2	bit 1	bit 0
P0CON0 (010H) (R/W)	P03MD	P02MD	P01MD	P00MD

Port 0.3 input mode select
 0: Input with pull-up/pull-down resistor (initial value)
 1: High impedance input

Port 0.2 input mode select
 0: Input with pull-up/pull-down resistor (initial value)
 1: High impedance input

Port 0.1 input mode select
 0: Input with pull-up/pull-down resistor (initial value)
 1: High impedance input

Port 0.0 input mode select
 0: Input with pull-up/pull-down resistor (initial value)
 1: High impedance input

	bit 3	bit 2	bit 1	bit 0
P0CON1 (011H) (R/W)	—	—	P0PUD	P0F

Port 0 pull-up/pull-down resistor mode select
 0: Inputs with pull-down resistors (initial value)
 1: Inputs with pull-up resistors

External interrupt sampling frequency select
 0: 128 Hz sampling (initial value)
 1: 4 kHz sampling

bit 1: P0PUD

This bit is used to select pull-up or pull-down resistors when any of the port 0 pins are selected by P0CON0 as an input with pull-up/pull-down resistor.

Setting P0PUD to "0" selects pull-down resistors, and setting to "1" selects pull-up resistors.

Individual specification of pull-down or pull-up resistors for the pins of port 0.0 to 0.3 is not possible.

(3) Port Interrupt Enable Register (P0IE)

The port 0 interrupt enable register (P0IE) is a 4-bit special function register (SFR) that enables/disables individual bits when port 0 is used as an external interrupt.

At system reset, the port interrupt enable register is cleared to "0" and all bits of port 0 are initialized to the interrupt disabled state.

	bit 3	bit 2	bit 1	bit 0
P0IE (012H) (R/W)	P03IE	P02IE	P01IE	P00IE

Port 0.3 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port 0.2 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port 0.1 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port 0.0 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

10.3.3 Port 0 External Interrupt Functions (External Interrupt 5)

An external interrupt (external interrupt 5) is assigned to port 0 as a secondary function. Individual bits can be enabled/disabled for external interrupt 5.

External interrupt generation for each input of port 0 is triggered by the falling edge of either the 128 Hz or 4 kHz sampling clock from the time base counter.

After the port level changes, interrupt request signal XI5INT is output and external interrupt 5 request flag (QXI5) is set. The maximum time delay from the change in port level until setting QXI5 is one cycle of the sampling clock (128 Hz or 4 kHZ).

Because the port 0 external interrupt 5 is set by a level change at any of the port 0 inputs, each bit of the port must be read to determine which bit of port 0 generated the interrupt.

External interrupt 5 is generated during the following states.

P0PUD = "0" (initial value: inputs with pull-down resistors) setting

With all P0.0 to P0.3 inputs at a "L" level, external interrupt 5 is generated when any port 0 input changes to a "H" level.

With any of P0.0 to P0.3 inputs at a "H" level, external interrupt 5 is generated when all the port 0 inputs change to a "L" level.

P0PUD = "1" (initial value: inputs with pull-up resistors) setting

With all P0.0 to P0.3 inputs at a "H" level, external interrupt 5 is generated when any port 0 input changes to a "L" level.

With any of P0.0 to P0.3 inputs at a "L" level, external interrupt 5 is generated when all the port 0 inputs change to a "H" level.

The interrupt vector address for external interrupt 5 is 001EH.

Figure 10-2 shows the timing for generation of external interrupt 5.

Figure 10-3 shows an equivalent circuit of external interrupt 5 control.

10

(a) When P0PUD = 0
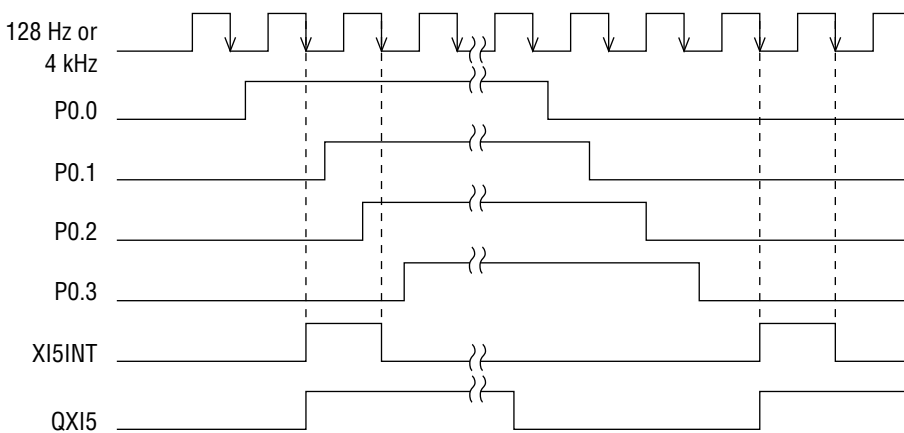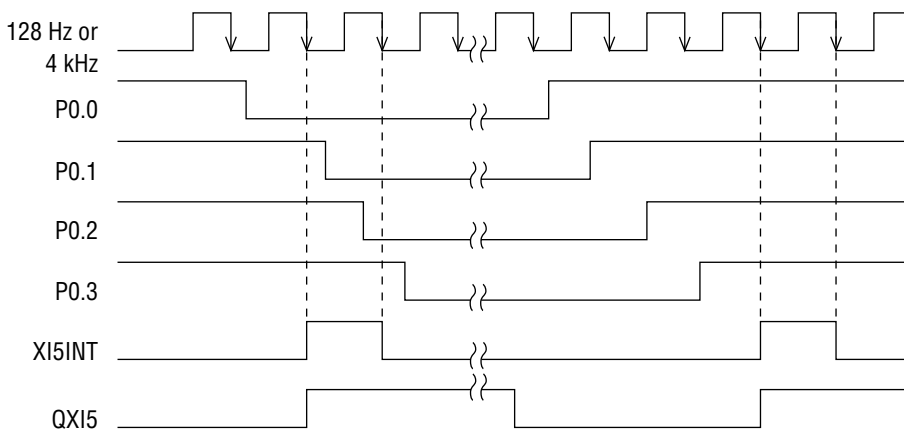
(b) When P0PUD = 1

Figure 10-2 Interrupt Generation Timing of External Interrupt 5
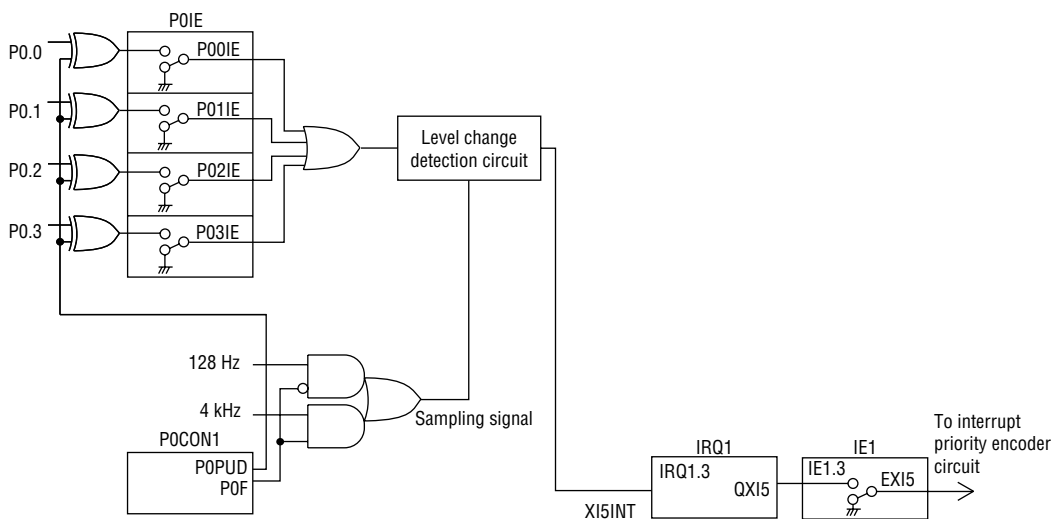
Figure 10-3 Equivalent Circuit of External Interrupt 5 Control

10.4 Ports 4–7 (P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)

The ML63326 has four 4-bit output ports: Port 4, Port 5, Port 6, and Port 7.

10.4.1 Port 4–7 Configuration

The circuit configuration for ports 4, 5, 6, and 7 is shown in Figure 10-4.
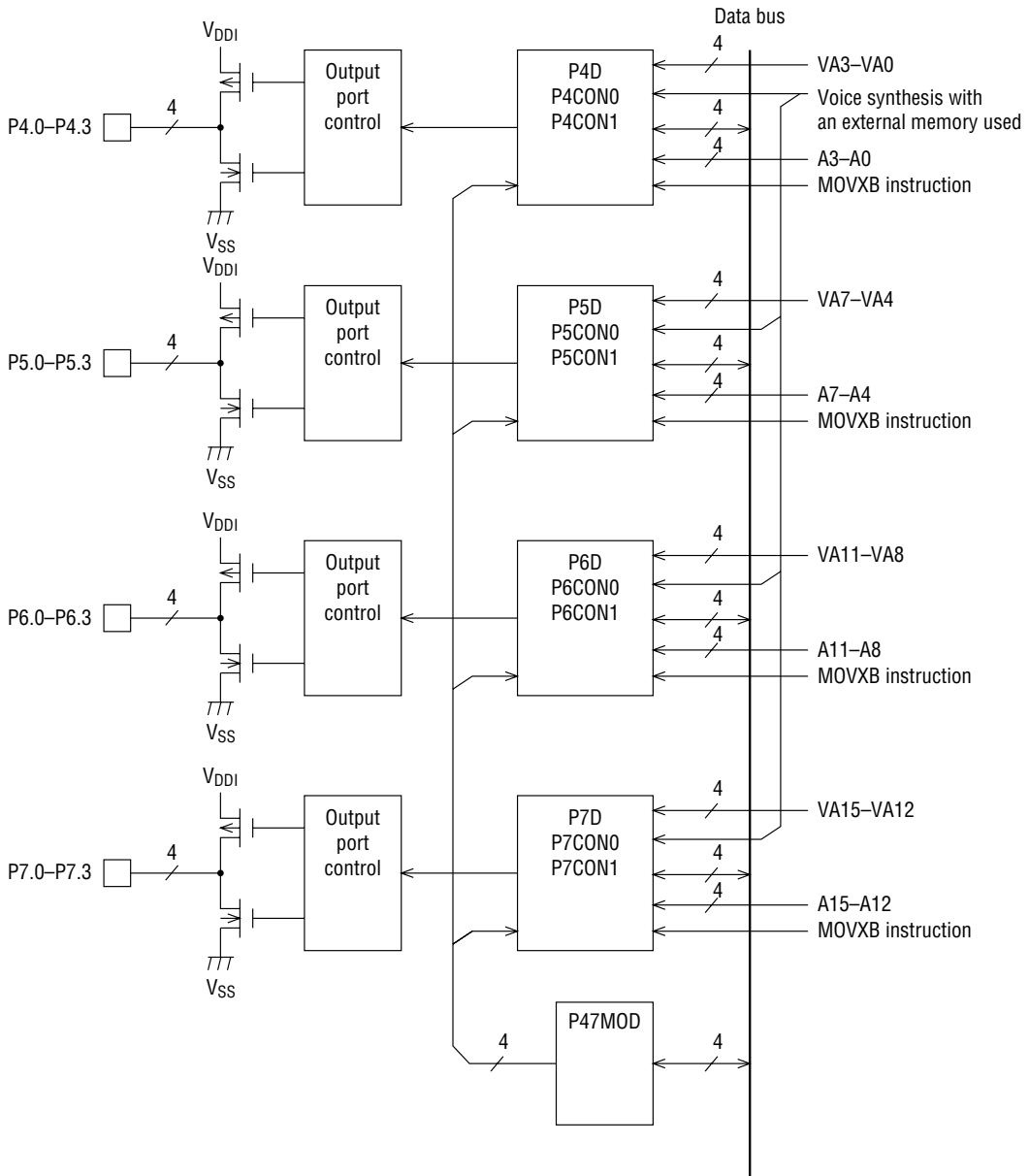
Figure 10-4 Input/Output Port (Ports 4–7) Configuration

10.4.2 Port 4–7 Registers

(1) Port data registers (P4D, P5D, P6D, P7D)

The port 4 data register (P4D), port 5 data register (P5D), port 6 data register (P6D) and port 7 data register (P7D) are 4-bit special function registers (SFRs) used to set the output values for the ports.

• Port 4
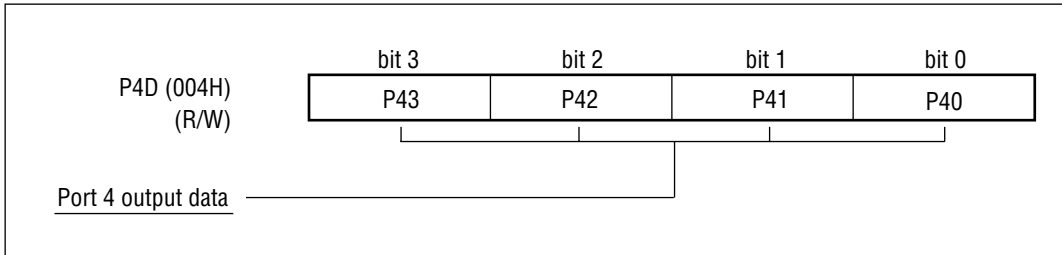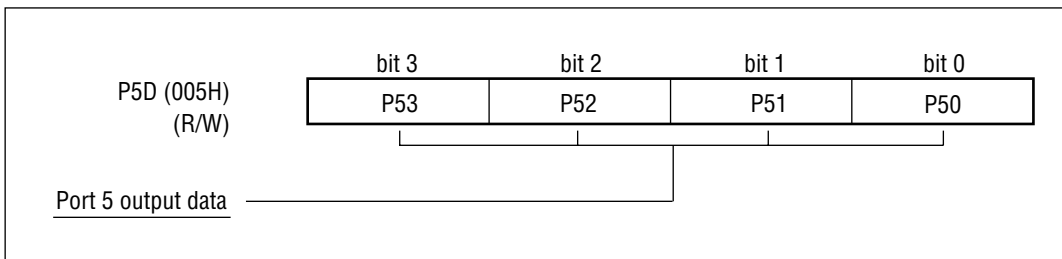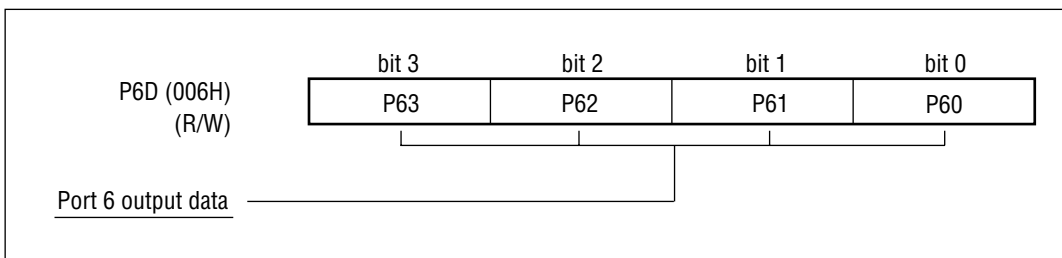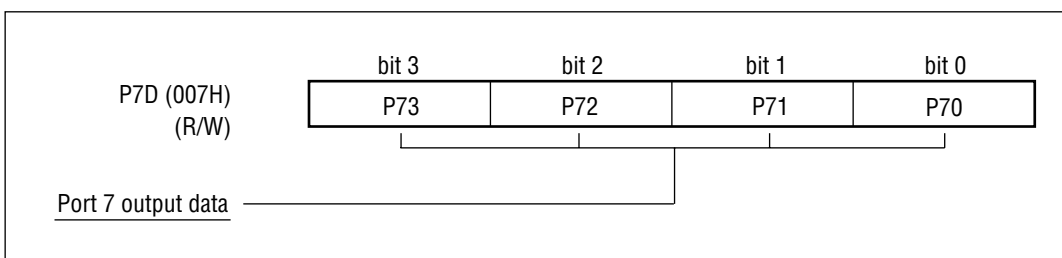
	bit 3	bit 2	bit 1	bit 0
P4D (004H) (R/W)	P43	P42	P41	P40

Port 4 output data

• Port 5

	bit 3	bit 2	bit 1	bit 0
P5D (005H) (R/W)	P53	P52	P51	P50

Port 5 output data

• Port 6

	bit 3	bit 2	bit 1	bit 0
P6D (006H) (R/W)	P63	P62	P61	P60

Port 6 output data

• Port 7

	bit 3	bit 2	bit 1	bit 0
P7D (007H) (R/W)	P73	P72	P71	P70

Port 7 output data

At system reset the port data registers are set to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-5 shows port change timing.
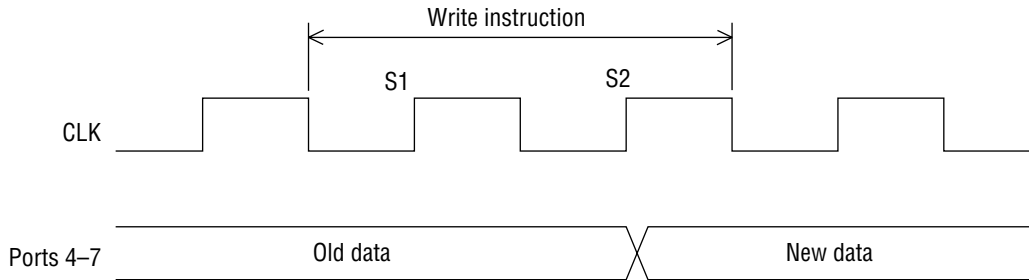
Figure 10-5 Port Change Timing

(2) Port control registers (P4CON0, P4CON1, P5CON0, P5CON1, P6CON0, P6CON1, P7CON0, P7CON1)

The port 4 control registers 0/1 (P4CON0, P4CON1), port 5 control registers 0/1 (P5CON0, P5CON1), port 6 control registers 0/1 (P6CON0, P6CON1) and port 7 control registers (P7CON0, P7CON1) are 4-bit special function registers (SFRs) used to select port output mode.

The output mode may be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset the port control registers are set to "0", and all ports are initialized to the CMOS output mode.

• Port 4

	bit 3	bit 2	bit 1	bit 0
P4CON0 (01AH) (R/W)	P41MD1	P41MD0	P40MD1	P40MD0

Port 4.1 output mode select
bit 3 bit 2
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

Port 4.0 output mode select
bit 1 bit 0
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

	bit 3	bit 2	bit 1	bit 0
P4CON1 (01BH) (R/W)	P43MD1	P43MD0	P42MD1	P42MD0

Port 4.3 output mode select
bit 3 bit 2
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

Port 4.2 output mode select
bit 1 bit 0
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

• Port 5

	bit 3	bit 2	bit 1	bit 0
P5CON0 (01CH) (R/W)	P51MD1	P51MD0	P50MD1	P50MD0

Port 5.1 output mode select

bit 3 bit 2
- 0   0 : CMOS output (initial value)
- 0   1 : N-channel open drain output
- 1   0 : P-channel open drain output
- 1   1 : High-impedance output

Port 5.0 output mode select

bit 1 bit 0
- 0   0 : CMOS output (initial value)
- 0   1 : N-channel open drain output
- 1   0 : P-channel open drain output
- 1   1 : High-impedance output

	bit 3	bit 2	bit 1	bit 0
P5CON1 (01DH) (R/W)	P53MD1	P53MD0	P52MD1	P52MD0

Port 5.3 output mode select

bit 3 bit 2
- 0   0 : CMOS output (initial value)
- 0   1 : N-channel open drain output
- 1   0 : P-channel open drain output
- 1   1 : High-impedance output

Port 5.2 output mode select

bit 1 bit 0
- 0   0 : CMOS output (initial value)
- 0   1 : N-channel open drain output
- 1   0 : P-channel open drain output
- 1   1 : High-impedance output

10

• Port 6

	bit 3	bit 2	bit 1	bit 0
P6CON0 (01EH) (R/W)	P61MD1	P61MD0	P60MD1	P60MD0

Port 6.1 output mode select

bit 3 bit 2
    0   0 : CMOS output (initial value)
    0   1 : N-channel open drain output
    1   0 : P-channel open drain output
    1   1 : High-impedance output

Port 6.0 output mode select

bit 1 bit 0
    0   0 : CMOS output (initial value)
    0   1 : N-channel open drain output
    1   0 : P-channel open drain output
    1   1 : High-impedance output

	bit 3	bit 2	bit 1	bit 0
P6CON1 (01FH) (R/W)	P63MD1	P63MD0	P62MD1	P62MD0

Port 6.3 output mode select

bit 3 bit 2
    0   0 : CMOS output (initial value)
    0   1 : N-channel open drain output
    1   0 : P-channel open drain output
    1   1 : High-impedance output

Port 6.2 output mode select

bit 1 bit 0
    0   0 : CMOS output (initial value)
    0   1 : N-channel open drain output
    1   0 : P-channel open drain output
    1   1 : High-impedance output

• Port 7

	bit 3	bit 2	bit 1	bit 0
P7CON0 (020H) (R/W)	P71MD1	P71MD0	P70MD1	P70MD0

Port 7.1 output mode select

bit 3 bit 2

0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

Port 7.0 output mode select

bit 1 bit 0

0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

	bit 3	bit 2	bit 1	bit 0
P7CON1 (021H) (R/W)	P73MD1	P73MD0	P72MD1	P72MD0

Port 7.3 output mode select

bit 3 bit 2

0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

Port 7.2 output mode select

bit 1 bit 0

0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

10

(3) Port mode register (P47MOD)

The port 4–7 mode register (P47MOD) is a 4-bit special function register (SFR) that enables the external memory address bus function, which is the secondary function of ports 4–7.

```
                        bit 3        bit 2        bit 1        bit 0
P47MOD (022H)      ┌──────────┬──────────┬──────────┬──────────┐
       (R/W)       │  P7MOD   │  P6MOD   │  P5MOD   │  P4MOD   │
                   └──────────┴──────────┴──────────┴──────────┘

    Port 7 pin function select
        0: Output port function (initial value)
        1: A15–A12 output function

    Port 6 pin function select
        0: Output port function (initial value)
        1: A11–A8 output function

    Port 5 pin function select
        0: Output port function (initial value)
        1: A7–A4 output function

    Port 4 pin function select
        0: Output port function (initial value)
        1: A3–A0 output function
```

At system reset the P47MOD register is set to "0", and all ports are set as normal output ports. When P47MOD bits are set to "1" and the MOVXB instruction executed, external memory addresses are output to the ports. If the MOVXB instruction is not executed, data register contents are output to the ports.

(4) Voice synthesis when using an external memory

When carrying out voice synthesis using an external memory, ports 4–7 output the lower 16 bits of the address (VA15–0). When carrying out voice synthesis using the ROM inside the chip, these will be in the normal port state. For details, see Chapter 13, "Voice Synthesis."

10.5 Port 8, Port 9, Port A (P8.0, P8.1, P9.0–P9.3, PA.0–PA.3)

The ML63326 has Port 8, Port 9 and Port A input/output ports.

10.5.1 Port 8, Port 9, Port A Configuration

The circuit configuration for ports 8, 9 and A is shown in Figure 10-6.
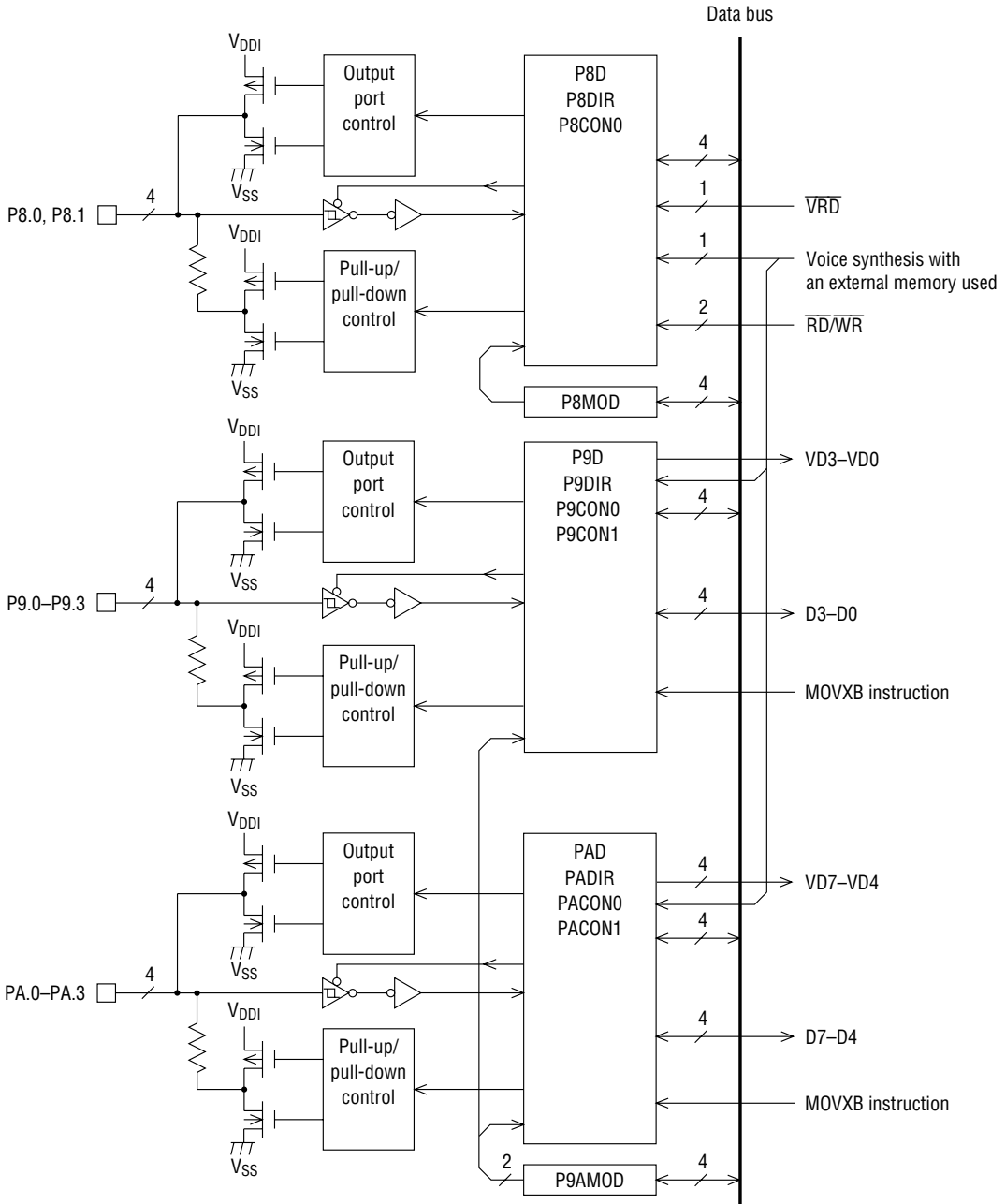
Figure 10-6 Input/Output Port (Ports 8, 9 and A) Configuration

10.5.2 Port 8, Port 9, Port A Registers

(1) Port direction registers (P8DIR, P9DIR, PADIR)

The port 8 direction register (P8DIR), the port 9 direction register (P9DIR), and port A direction register (PADIR) are 4-bit special function registers (SFRs) which specify the port input/output direction for each bit. Pins corresponding to port direction register bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset the direction registers are set to "0", and all ports are initialized in input mode.

• Port 8

	bit 3	bit 2	bit 1	bit 0
P8DIR (025H) (R/W)	P83DIR*	P82DIR*	P81DIR	P80DIR

Port 8 input/output setting
 0: Input (initial value)
 1: Output
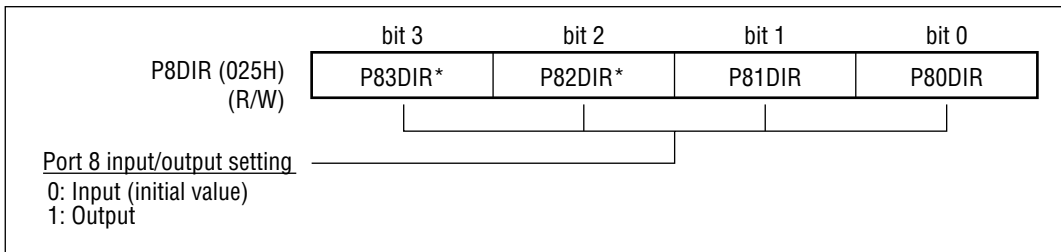
⚠ Note:

*: The bits P83DIR and P82DIR have to be set to "1" or "0" before executing an external memory transfer instruction (MOVXB) or carrying out voice synthesis.

The pins P8.3 and P8.2 are not present in the ML63326.

For details, see Chapter 11, "External Memory Transfer Function" and Chapter 13, "Voice Synthesis."

• Port 9

	bit 3	bit 2	bit 1	bit 0
P9DIR (029H) (R/W)	P93DIR	P92DIR	P91DIR	P90DIR

Port 9 input/output setting
 0: Input (initial value)
 1: Output

• Port A

	bit 3	bit 2	bit 1	bit 0
PADIR (02CH) (R/W)	PA3DIR	PA2DIR	PA1DIR	PA0DIR

Port A input/output setting
 0: Input (initial value)
 1: Output
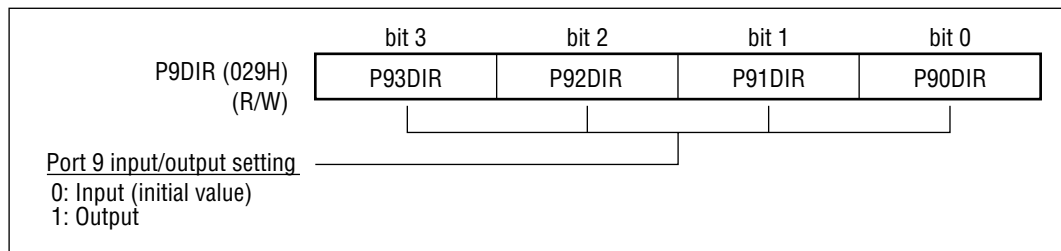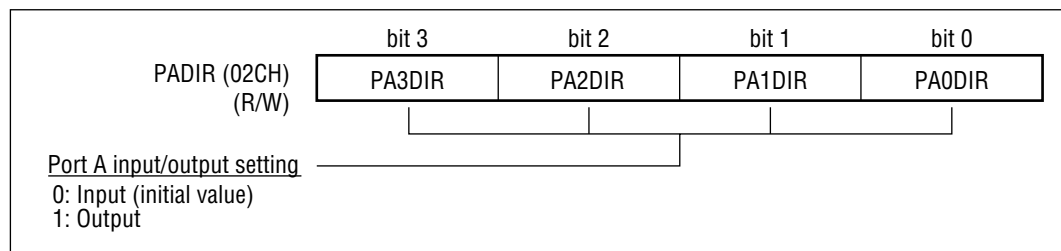
(2) Port data registers (P8D, P9D, PAD)

The port 8 data register (P8D), the port 9 data register (P9D), and port A data register (PAD) are 4-bit special function registers (SFRs) used to set the output values for the ports.

When port direction register (P8DIR, P9DIR, PADIR) bits are set to "1" and the output mode selected, the contents of the port data registers are output to the ports.

When the output mode is selected and the port data register read, the contents of the data register are read.

The port pin levels are read when the port data registers are read with the port direction register bits set to "0" and the input mode selected.

• Port 8

	bit 3	bit 2	bit 1	bit 0
P8D (008H) (R/W)	P83*	P82*	P81	P80

Port 8 input/output data
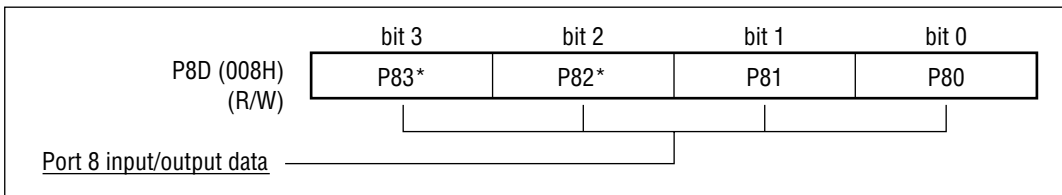
⚠ Note:

*: Bits P83 and P82 have to be set to "1" or "0" before executing an external memory transfer instruction (MOVXB) or carrying out voice synthesis.

The pins P8.3 and P8.2 are not present in the ML63326.

For details, see Chapter 11, "External Memory Transfer Function" and Chapter 13, "Voice Synthesis."

• Port 9

	bit 3	bit 2	bit 1	bit 0
P9D (009H) (R/W)	P93	P92	P91	P90

Port 9 input/output data

• Port A

	bit 3	bit 2	bit 1	bit 0
PAD (00AH) (R/W)	PA3	PA2	PA1	PA0

Port A input/output data
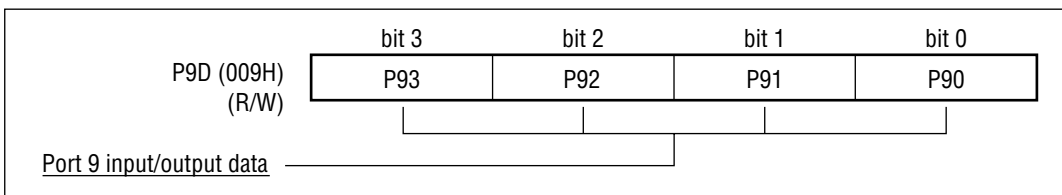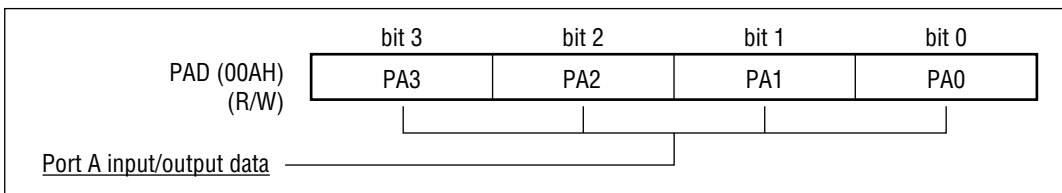
At system reset the port data registers are set to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-7 shows port change timing.
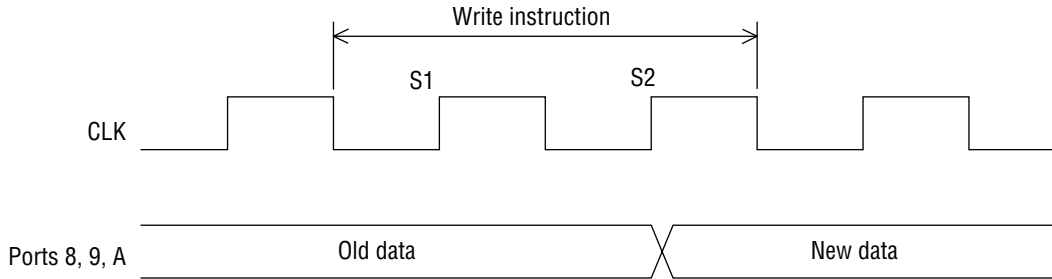
Figure 10-7 Port Change Timing

(3) Port control registers (P8CON0, P9CON0, P9CON1, PACON0, PACON1)

The port 8 control register 0 (P8CON0), the port 9 control registers 0/1 (P9CON0, P9CON1), and port A control registers 0/1 (PACON0, PACON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode may be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode may be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset the port control registers are set to "0", and all ports are initialized to pull-down resistor input mode and CMOS output mode.

• Port 8

	bit 3	bit 2	bit 1	bit 0
P8CON0 (023H) (R/W)	P81MD1	P81MD0	P80MD1	P80MD0

Port 8.1 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port 8.0 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

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• Port 9

	bit 3	bit 2	bit 1	bit 0
P9CON0 (027H) (R/W)	P91MD1	P91MD0	P90MD1	P90MD0

Port 9.1 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port 9.0 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

	bit 3	bit 2	bit 1	bit 0
P9CON1 (028H) (R/W)	P93MD1	P93MD0	P92MD1	P92MD0

Port 9.3 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port 9.2 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

• Port A

	bit 3	bit 2	bit 1	bit 0
PACON0 (02AH) (R/W)	PA1MD1	PA1MD0	PA0MD1	PA0MD0

Port A.1 input/output mode select

Input mode
bit 3 bit 2
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 3 bit 2
0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

Port A.0 input/output mode select

Input mode
bit 1 bit 0
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 1 bit 0
0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

	bit 3	bit 2	bit 1	bit 0
PACON1 (02BH) (R/W)	PA3MD1	PA3MD0	PA2MD1	PA2MD0

Port A.3 input/output mode select

Input mode
bit 3 bit 2
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 3 bit 2
0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

Port A.2 input/output mode select

Input mode
bit 1 bit 0
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 1 bit 0
0   0 : CMOS output (initial value)
0   1 : N-channel open drain output
1   0 : P-channel open drain output
1   1 : High-impedance output

10

(4) Port mode registers (P8MOD, P9AMOD)

P8MOD and P9AMOD are 4-bit special function registers (SFRs) that enable the function of access by external memory transfer instruction (MOVXB) which is a secondary function of the respective ports.

Table 10-2 lists the secondary functions of ports 8, 9, and A.

Table 10-2 Port 8, 9, A Secondary Functions

Port	Secondary function	Description
P8.0	$\overline{RD}$	External memory read signal
P8.1	$\overline{WR}$	External memory write signal
P9.0	D0	Data bus of the external memory
P9.1	D1	
P9.2	D2	
P9.3	D3	
PA.0	D4	
PA.1	D5	
PA.2	D6	
PA.3	D7	

The port mode registers are set to "0" at a system reset thereby making the ports have the normal port functions.

	bit 3	bit 2	bit 1	bit 0
P8MOD (026H) (R/W)	—	—	P81MOD	P80MOD

Port 8.1 pin function select
 0: Input/output port function (initial value)
 1: $\overline{WR}$ output function (the output mode is set irrespective of P81DIR)

Port 8.0 pin function select
 0: Input/output port function (initial value)
 1: $\overline{RD}$ output function (the output mode is set irrespective of P80DIR)

	bit 3	bit 2	bit 1	bit 0
P9AMOD (02DH) (R/W)	—	—	PAMOD	P9MOD

Port A pin function select
 0: Input/output port function (initial value)
 1: D7–D4 input/output function

Port 9 pin function select
 0: Input/output port function (initial value)
 1: D3–D0 input/output function

When each of the bits of P9AMOD is set to "1" and the MOVXB instruction is executed, P9–PA become the data signals for the external memory. Further, when the MOVXB instruction is not executed, P9–PA have the normal input/output port function.

(5) Voice synthesis when using an external memory

When carrying out voice synthesis using an external memory, the $\overline{\text{RD}}$ signal is output at P8.0 and the data from the external memory is input via P9 (P9.3–P9.0) and PA (PA.3–PA.0). These pins will be in the normal port state when carrying out voice synthesis using the ROM inside the chip.

For details, see Chapter 13, "Voice Synthesis."

10

10.6 Port B (PB.0–PB.3)

The ML63326 has Port B, a 4-bit input/output port.

10.6.1 Port B Configuration

The circuit configuration for port B is shown in Figure 10-8.
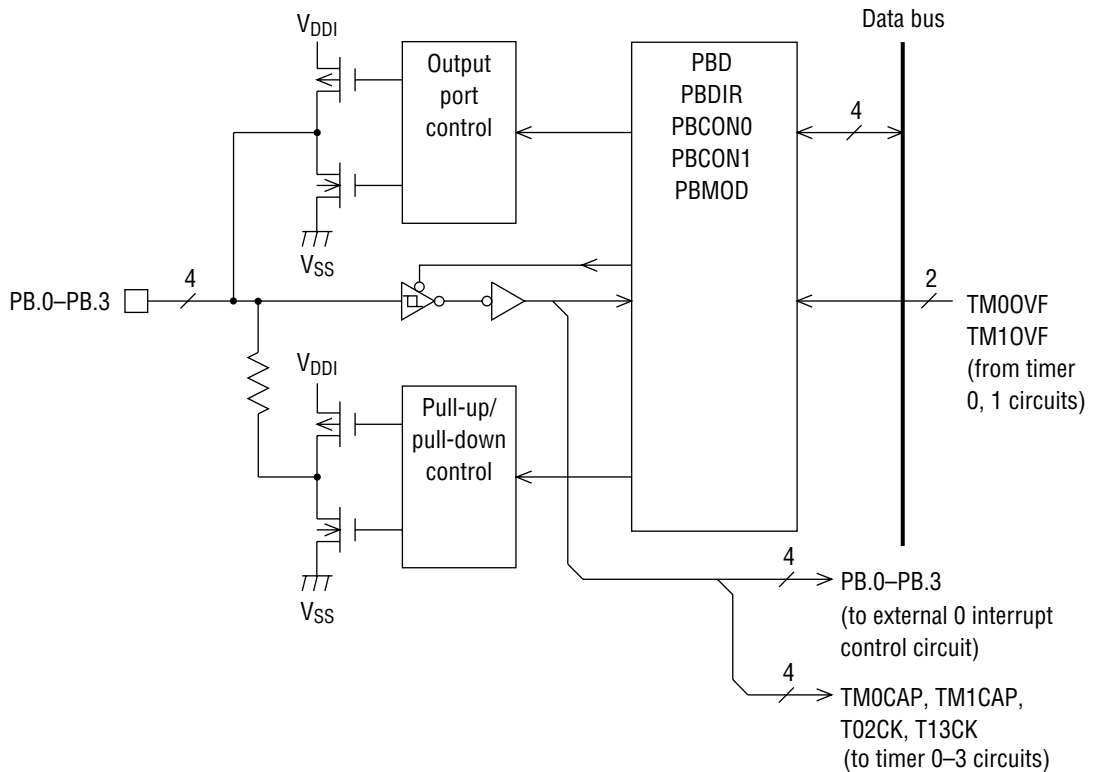
Figure 10-8 Input /Output Port (Port B) Configuration

10.6.2 Port B Registers

(1) Port B direction register (PBDIR)

PBDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PBDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset the port B direction register is set to "0", and port B is initialized to input mode.
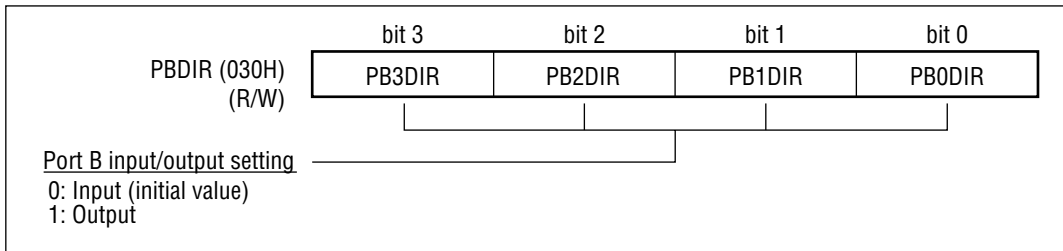
(2) Port B data register (PBD)

PBD is a 4-bit special function register used to set the output values for port B.

When the port B data register is read during the output mode, the content of the PBD is read.

The port B pin levels are read when the port B data register is read with the port B direction register bits set to "0" and the input mode selected.

10
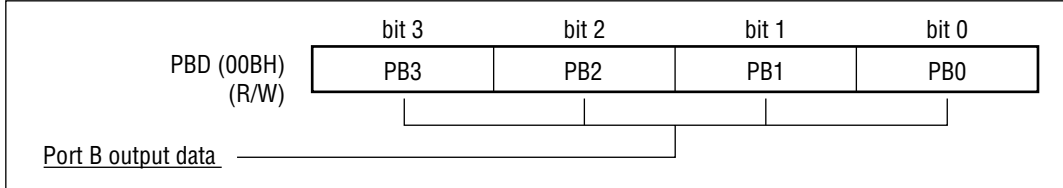
At system reset the port B data register (PBD) is set to "0". When data is written to the port B data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-9 indicates port change timing.
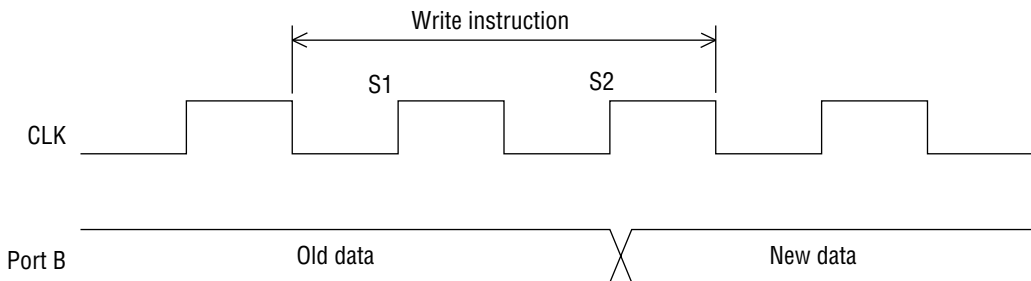
Figure 10-9 Port B Change Timing

(3) Port B control registers (PBCON0, PBCON1)

The port B control registers 0/1 (PBCON0, PBCON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset the PBCON0 and PBCON1 are set to "0", and port B is initialized to pull-down resistor input mode and CMOS output mode.

	bit 3	bit 2	bit 1	bit 0
PBCON0 (02EH) (R/W)	PB1MD1	PB1MD0	PB0MD1	PB0MD0

Port B.1 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port B.0 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

	bit 3	bit 2	bit 1	bit 0
PBCON1 (02FH) (R/W)	PB3MD1	PB3MD0	PB2MD1	PB2MD0

Port B.3 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port B.2 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

(4) Port B mode register (PBMOD)

PBMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port B is used as an external interrupt. It is also used to select port B secondary functions other than external interrupt.

The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

Port B secondary functions are indicated in Table 10-3.

Table 10-3 Port B Secondary Functions

Port	Secondary function	Description
PB.0	TM0CAP	Timer 0 capture input
PB.1	TM1CAP	Timer 1 capture input
PB.2	T02CK	Timer 0, timer 2 external clock input
PB.3	T13CK	Timer 1, timer 3 external clock input
PB.0	TM0OVF	Timer 0 overflow flag output
PB.1	TM1OVF	Timer 1 overflow flag output
PB.0		
PB.1	INT0	External interrupt 0
PB.2		
PB.3		
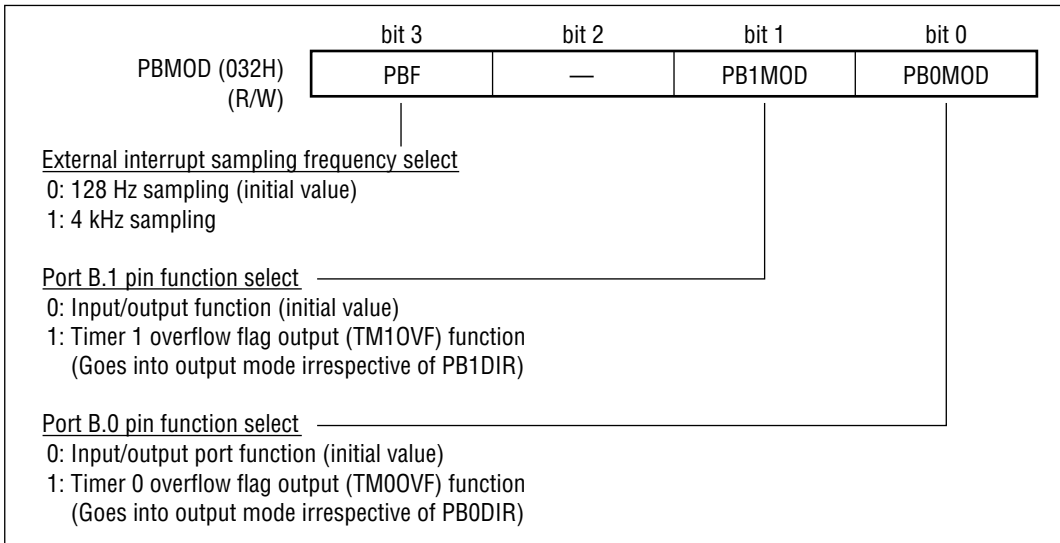
At system reset the PBMOD is initialized to "0".

(5) Port B interrupt enable register (PBIE)

PBIE is a 4-bit special function register (SFR) that enables/disables individual bits when port B is used as an external interrupt input.

At system reset, PBIE is cleared to "0" and all bits of port B are initialized to the interrupt disabled state.

	bit 3	bit 2	bit 1	bit 0
PBIE (031H) (R/W)	PB3IE	PB2IE	PB1IE	PB0IE

Port B.3 interrupt enable/disable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port B.2 interrupt enable/disable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port B.1 interrupt enable/disable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port B.0 interrupt enable/disable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

10.6.3 Port B External Interrupt Function (External Interrupt 0)

Port B has external interrupt 0 allocated as secondary function. Individual bits of port B can be enabled/disabled.

External interrupt generation for port B is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI0INT) is output, and the interrupt request flag (QXI0) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port B external interrupt is set by a level change at any of the port B inputs, each bit of the port must be read to determine which bit of port B generated the interrupt.

The interrupt start address for external interrupt 0 is 0014H.

Figure 10-10 shows the external interrupt 0 generation timing.

Figure 10-11 shows the equivalent circuit for external interrupt 0 control.
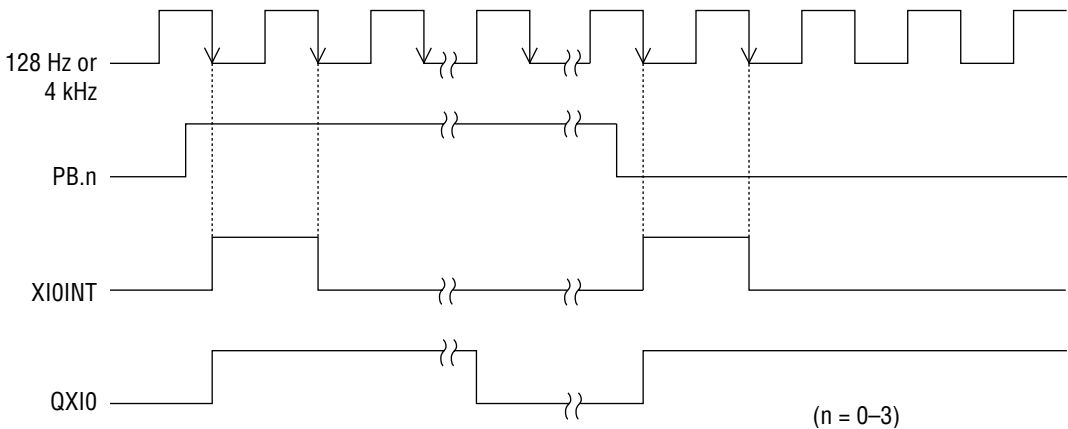
Figure 10-10 External Interrupt 0 Generation Timing
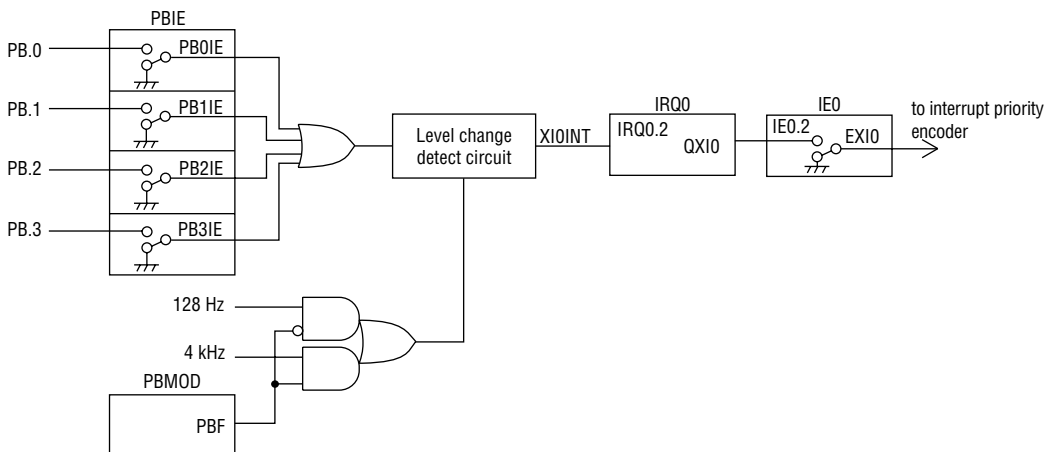
Figure 10-11 External Interrupt 0 Control Equivalent Circuit

10.7 Port E (PE.0–PE.3)

The ML63326 has Port E, a 4-bit input/output port.

10.7.1 Port E Configuration

The circuit configuration for port E is shown in Figure 10-12.
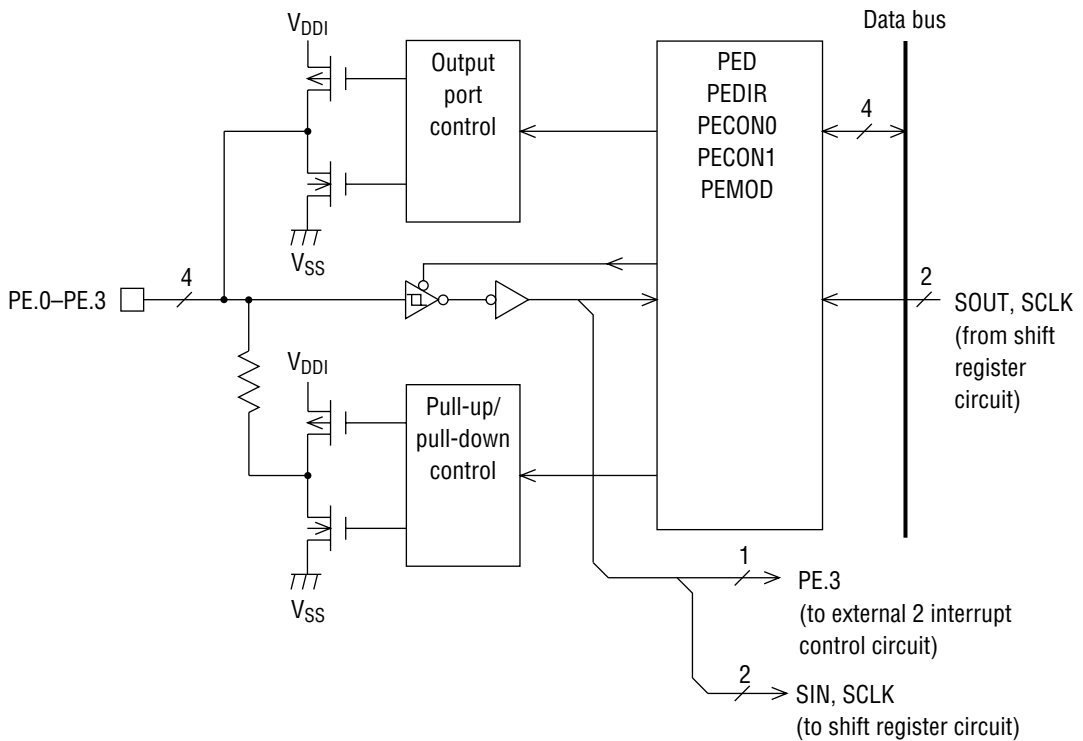
Figure 10-12 Input/Output Port (Port E) Configuration

10.7.2 Port E Registers

(1) Port E direction register (PEDIR)

PEDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PEDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset the port E direction register is set to "0", and port E is initialized to input mode.

	bit 3	bit 2	bit 1	bit 0
PEDIR (03FH) (R/W)	PE3DIR	PE2DIR	PE1DIR	PE0DIR

Port E input/output setting
 0: Input (initial value)
 1: Output
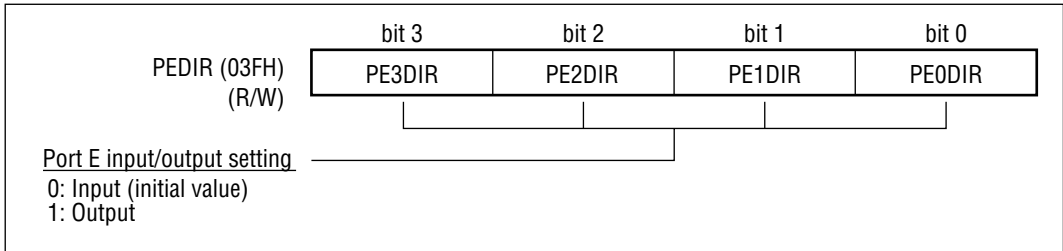
(2) Port E data register (PED)

PED is a 4-bit special function register used to set the output values for port E.

When the port E direction register (PEDIR) is set to "1" and the output mode is selected, the content of the PED is output to port E.

The port E pin levels are read when PED is read with the port E direction register bits set to "0" and the input mode selected.

	bit 3	bit 2	bit 1	bit 0
PED (00EH) (R/W)	PE3	PE2	PE1	PE0

Port E output data
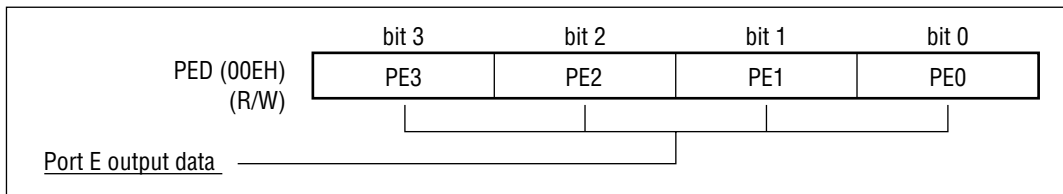
At system reset the port E data register is reset to "0". When data is written to the port E data register, the pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-13 indicates port change timing.
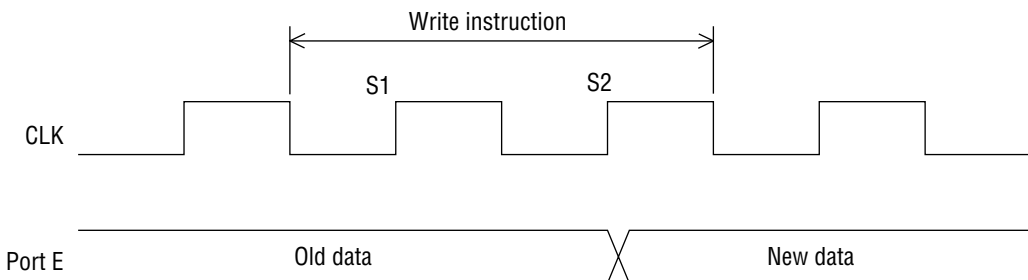
Figure 10-13 Port E Change Timing

(3) Port E control registers (PECON0, PECON1)

The port E control registers 0/1 (PECON0, PECON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset the PECON0 and PECON1 are set to "0", and port E is initialized to pull-down resistor input mode and CMOS output mode.

	bit 3	bit 2	bit 1	bit 0
PECON0 (03DH) (R/W)	PE1MD1	PE1MD0	PE0MD1	PE0MD0

Port E.1 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port E.0 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

	bit 3	bit 2	bit 1	bit 0
PECON1 (03EH) (R/W)	PE3MD1	PE3MD0	PE2MD1	PE2MD0

Port E.3 input/output mode select

Input mode			Output mode		
bit 3	bit 2		bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

Port E.2 input/output mode select

Input mode			Output mode		
bit 1	bit 0		bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)	0	0	: CMOS output (initial value)
1	0	: Input with pull-up resistor	0	1	: N-channel open drain output
×	1	: High-impedance input	1	0	: P-channel open drain output
			1	1	: High-impedance output

(4) Port E mode register (PEMOD)

PEMOD is a 4-bit special function register (SFR) used to select the sampling frequency when PE.3 is used as an external interrupt. It is also used to select port E secondary functions other than external interrupt.

The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

Port E secondary functions are indicated in Table 10-4.

Table 10-4 Port E Secondary Functions

Port	Secondary function	Description
PE.0	SIN	Shift register data input
PE.1	SOUT	Shift register data output
PE.2	SCLK	Shift register clock I/O
PE.3	INT2	External interrupt 2

	bit 3	bit 2	bit 1	bit 0
PEMOD (040H) (R/W)	PEF	PE2MOD	PE1MOD	PE0MOD

External interrupt sampling frequency select
 0: 128 Hz sampling (initial value)
 1: 4 kHz sampling

Port E.2 pin function select
 0: Input/output port function (initial value)
 1: Shift register clock input/output (SCLK) function
    (Switching of input/output mode depends on the input/output selection of
    the shift clock of the shift register control register SFTCON0, irrespective
    of the PE2DIR value.)

Port E.1 pin function select
 0: Input/output port function (initial value)
 1: Shift register data output (SOUT) function (goes into output mode irrespective of PE1DIR)

Port E.0 pin function select
 0: Input/output port function (initial value)
 1: Shift register data input (SIN) function (goes into input mode irrespective of PE0DIR)

10

At system reset the PEMOD is initialized to "0".

10.7.3 Port E.3 External Interrupt Function (External Interrupt 2)

Port E.3 has external interrupt 2 allocated as secondary function.

External interrupt generation for PE.3 is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI2INT) is output, and the interrupt request flag (QXI2) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt start address for external interrupt 2 is 0018H.

Figure 10-14 shows the external interrupt 2 generation timing.

Figure 10-15 shows the equivalent circuit for external interrupt 2 control.
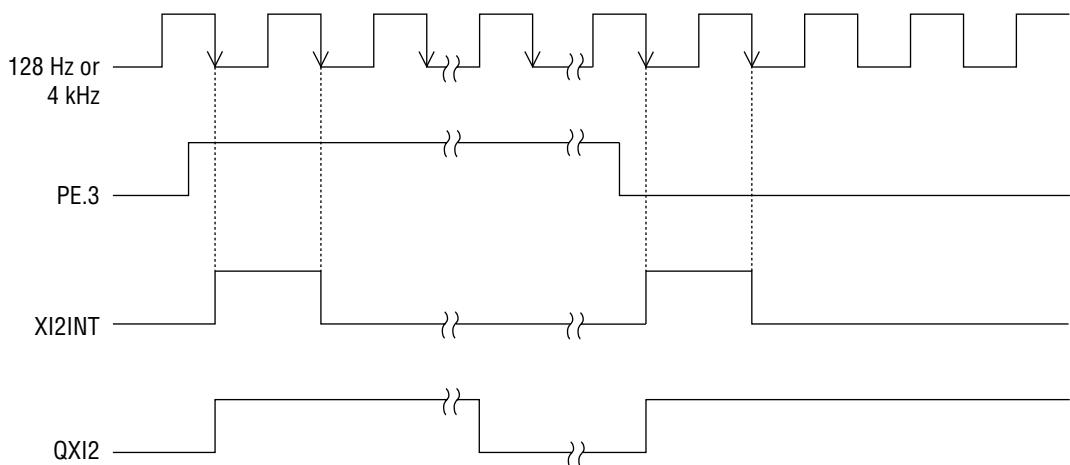
Figure 10-14 External Interrupt 2 Generation Timing
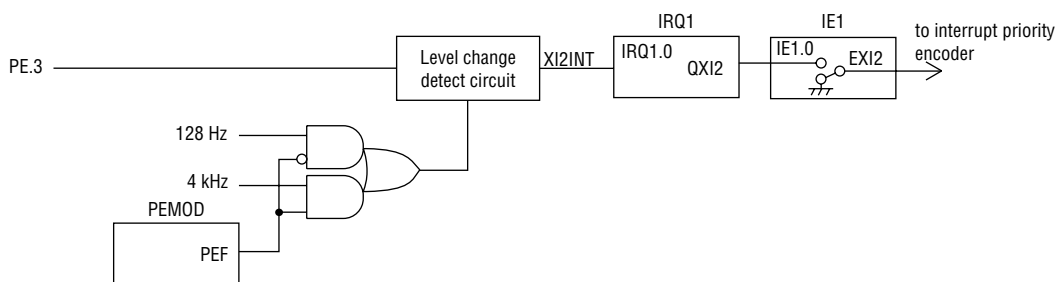
Figure 10-15 External Interrupt 2 Control Equivalent Circuit

10.8 Port F (PF.0–PF.3)

The ML63326 has Port F, a 4-bit input/output port.

10.8.1 Port F Configuration

The circuit configuration for port F is shown in Figure 10-16.
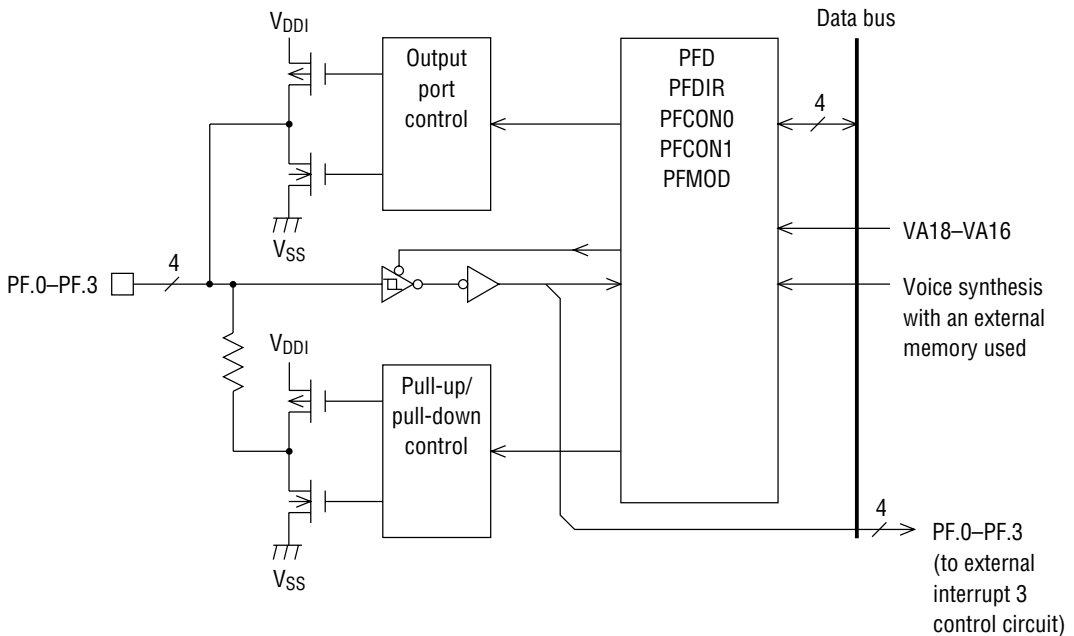
Figure 10-16 Input/Output Port (Port F) Configuration

10.8.2 Port F Registers

(1) Port F direction register (PFDIR)

PFDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PFDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset the port F direction register is set to "0", and port F is initialized to input mode.
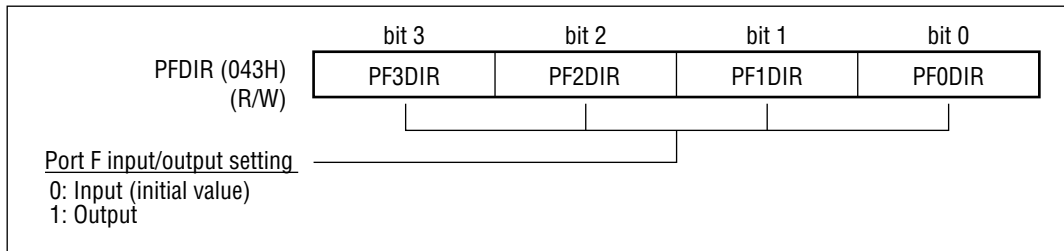
(2) Port F data register (PFD)

PFD is a 4-bit special function register used to set the output values for port F.

When the port F direction register (PFDIR) is set to "1" and the output mode is selected, the content of the PFD is output to port F.

The port F pin levels are read when PFD is read with the port F direction register bits set to "0" and the input mode selected.
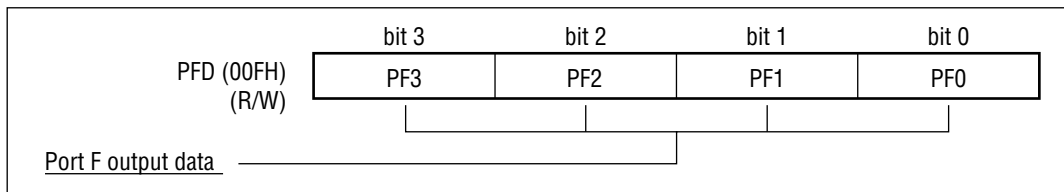
At system reset the port F data register is reset to "0". When data is written to the port F data register, the pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 10-17 indicates port change timing.
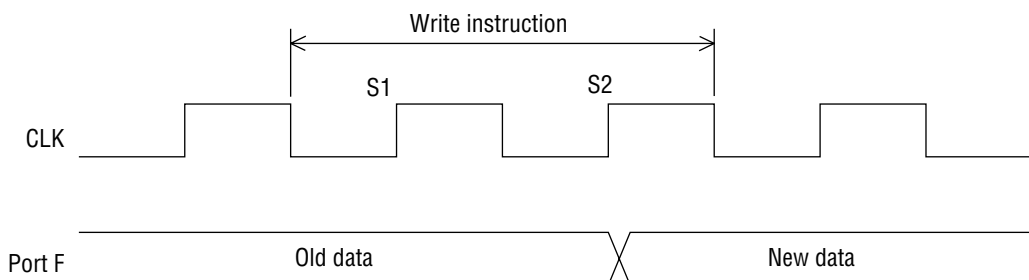
Figure 10-17 Port F Change Timing

(3) Port F control registers (PFCON0, PFCON1)

The port F control registers 0/1 (PFCON0, PFCON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset the PFCON0 and PFCON1 are set to "0", and port F is initialized to pull-down resistor input mode and CMOS output mode.

	bit 3	bit 2	bit 1	bit 0
PFCON0 (041H) (R/W)	PF1MD1	PF1MD0	PF0MD1	PF0MD0

Port F.1 input/output mode select

Input mode
bit 3 bit 2
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 3 bit 2
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

Port F.0 input/output mode select

Input mode
bit 1 bit 0
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 1 bit 0
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

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	bit 3	bit 2	bit 1	bit 0
PFCON1 (042H) (R/W)	PF3MD1	PF3MD0	PF2MD1	PF2MD0

Port F.3 input/output mode select

Input mode
bit 3 bit 2
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 3 bit 2
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

Port F.2 input/output mode select

Input mode
bit 1 bit 0
  0   0 : Input with pull-down resistor (initial value)
  1   0 : Input with pull-up resistor
  ×   1 : High-impedance input

Output mode
bit 1 bit 0
  0   0 : CMOS output (initial value)
  0   1 : N-channel open drain output
  1   0 : P-channel open drain output
  1   1 : High-impedance output

(4) Port F mode register (PFMOD)

PFMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port F is used as an external interrupt.

The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

Port F secondary functions are indicated in Table 10-5.

Table 10-5 Port F Secondary Functions

Port	Secondary function	Description
PF.0		
PF.1	INT3	External interrupt 3
PF.2		
PF.3		

	bit 3	bit 2	bit 1	bit 0
PFMOD (045H) (R/W)	—	—	—	PFF

External interrupt sampling frequency select
 0: 128 Hz sampling (initial value)
 1: 4 kHz sampling
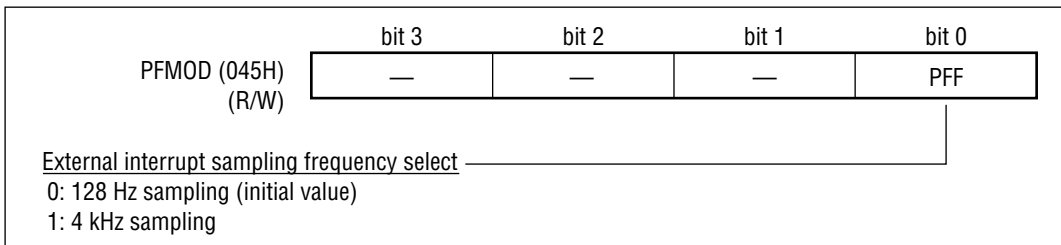
At system reset the PFMOD is initialized to "0".

(5) Voice synthesis when using an external memory

The pins PF.2, PF.1, and PF.0 output the high order 3-bit address (VA18–VA16) when carrying out voice synthesis using an external memory. These pins will be in the normal port state when carrying out voice synthesis using the ROM inside the chip.

For details, see Chapter 13, "Voice Synthesis."

(6) Port F interrupt enable register (PFIE)

PFIE is a 4-bit special function register (SFR) that is used for selecting the interrupt enable/disable state for each bit when port F is used as an external interrupt input.

All bits of PFIE are reset to "0" at a system reset and all port F interrupts will be initialized to the interrupt disabled state.

	bit 3	bit 2	bit 1	bit 0
PFIE (044H) (R/W)	PF3IE	PF2IE	PF1IE	PF0IE

Port F.3 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port F.2 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port F.1 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

Port F.0 interrupt disable/enable select
 0: Interrupt disabled (initial value)
 1: Interrupt enabled

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10.8.3 Port F External Interrupt Function (External Interrupt 3)

Port F has external interrupt 3 allocated as secondary function.

External interrupt generation for PF is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI3INT) is output, and the interrupt request flag (QXI3) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port F external interrupt is set by a level change at any of the port F inputs, each bit of the port must be read to determine which bit of port F generated the interrupt.

The interrupt start address for external interrupt 3 is 001AH.

Figure 10-18 shows the external interrupt 3 generation timing.

Figure 10-19 shows the equivalent circuit for external interrupt 3 control.
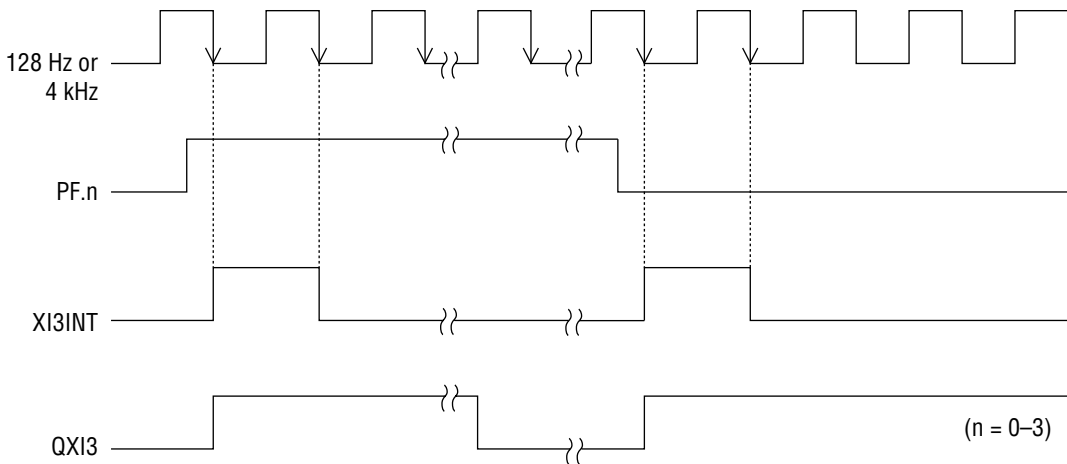
Figure 10-18 External Interrupt 3 Generation Timing
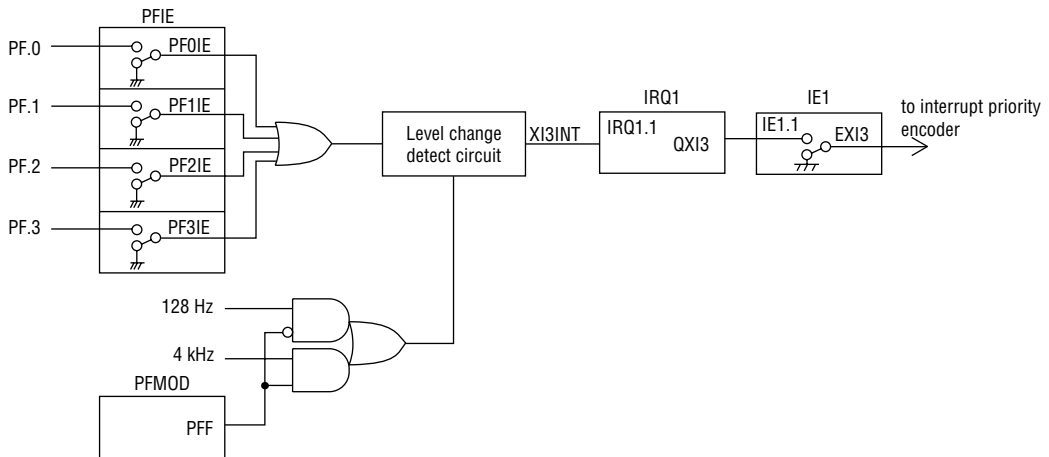
Figure 10-19 External Interrupt 3 Control Equivalent Circuit

External Memory Transfer Function (EXTMEM)

Chapter 11 External Memory Transfer Function (EXTMEM)

11.1 Overview

In the ML63326, the character data in the voice ROM area inside the chip or the character data in the memory area external to the chip can be accessed using the external memory transfer instruction (MOVXB).

The distinction of whether to access the area of the ROM inside the chip or to access the memory area external to the chip is done by setting P83 (bit 3 of P8D) and P82 (bit 2 of P8D).

⚠ Note :

It is not possible to access the voice synthesis section while the external memory transfer instruction is being executed. Further, it is also not possible to execute the external memory transfer instruction while the voice synthesis section is being accessed.

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11.2 Connection with the External Memory

The secondary port functions required when using the external memory transfer instruction are shown in Table 11-1, and Figure 11-1 shows the diagram of connections with the external memory.

Table 11-1 Port Secondary Functions

Pin name	I/O	Function
P4.0/A0	0	P4, P5, P6, P7 secondary functions: Address bus signals for external memory access
P4.1/A1		
P4.2/A2		
P4.3/A3		
P5.0/A4		
P5.1/A5		
P5.2/A6		
P5.3/A7		
P6.0/A8		
P6.1/A9		
P6.2/A10		
P6.3/A11		
P7.0/A12		
P7.1/A13		
P7.2/A14		
P7.3/A15		
P9.0/D0	I/O	P9, PA secondary functions: Data bus signals for external memory access
P9.1/D1		
P9.2/D2		
P9.3/D3		
PA.0/D4		
PA.1/D5		
PA.2/D6		
PA.3/D7		
P8.0/$\overline{\text{RD}}$	0	P8.0 secondary functions: Read signal (negative logic) for external memory access
P8.1/$\overline{\text{WR}}$	0	P8.1 secondary functions: Write signal (negative logic) for external memory access
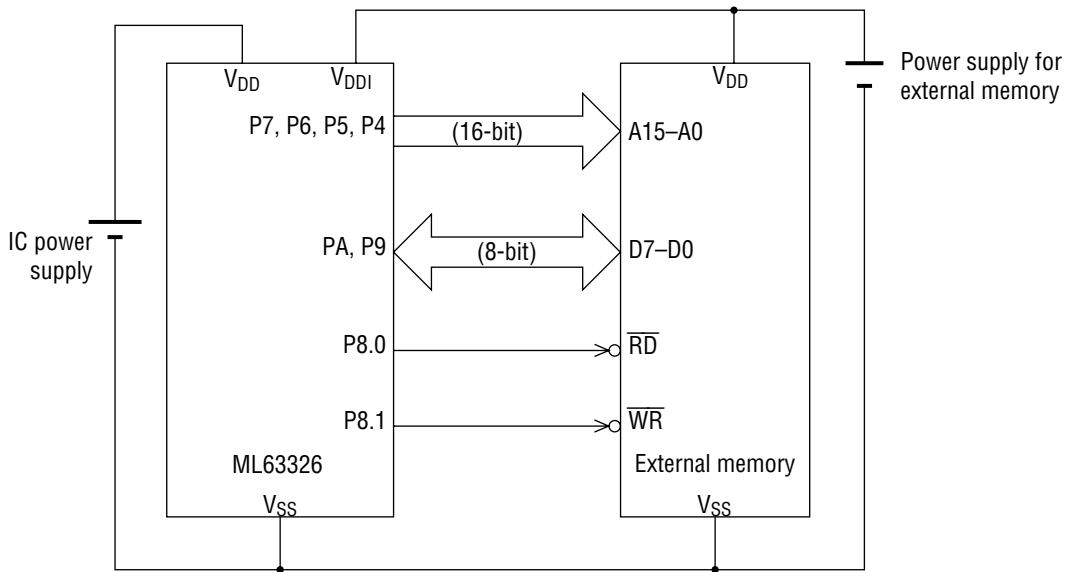
Figure 11-1 Connection to External Memory

11.3 External Memory Address Space

A maximum of 16 address lines can be selected as port secondary functions, allowing access to 64 Kbytes of external memory.

Also, the external memory space can be extended beyond 64 Kbytes by using ports other than those being used in the secondary function as the additional address lines. For example (Figure 11-2), if port F (PF.2–PF.0) is used for chip select, the external memory space will be

64 Kbytes $\times$ 8 = 512 Kbytes
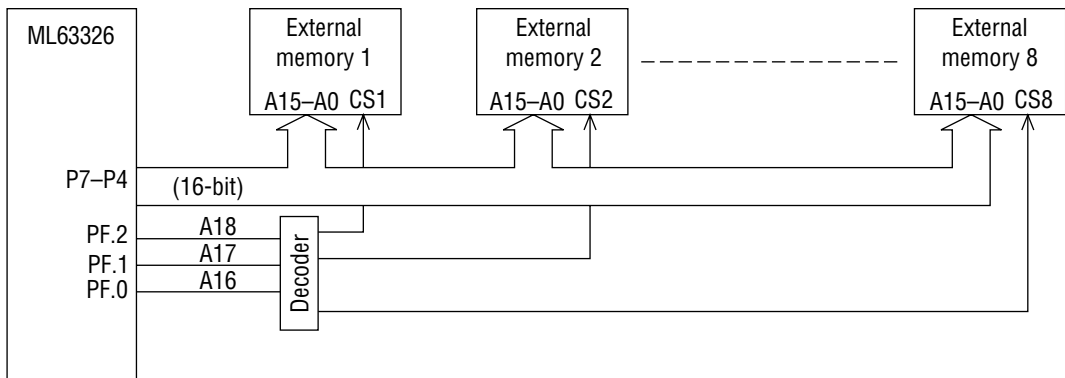
Figure 11-2 Example of Memory Space Extension Using Additional Address Lines

11.4 Setting of Secondary Port Functions

The secondary functions of the port need to be set in order to execute the external memory transfer instruction. This setting is necessary for accessing both the voice ROM inside the chip and the memory area external to the chip. See Chapter 10, "Ports" for details of the registers, etc., for the settings.

Further, even if secondary functions are set for the ports P7–P4, PA, and P9, the state set by the port control registers will be effective when the external memory transfer instruction is not executed. Therefore, these ports will become the normal output ports or I/O ports.

In addition, the pins P8.0 and P8.1 are assigned to the read signal ($\overline{RD}$) and the write signal ($\overline{WR}$) respectively from the moment when the secondary functions are set for them.

11.5 Distinction between ROM Area inside the Chip and Memory Area External to the Chip

The distinction of whether to access the area of the ROM inside the chip or to access the memory area external to the chip is done by setting P83 (bit 3 of P8D) and P82 (bit 2 of P8D). Table 11-2 shows the relationship between the set values of P83 and P82 and the memory accessed.

Table 11-2 Relationship between P83 and P82 Settings and the Memory Area Accessed

P83	P82	Memory area accessed by the MOVXB instruction
0	1	Voice ROM area inside the chip
1	1	Memory area external to the chip

11.6 Reading from External Memory

Use the following procedure for reading data from the external memory.

(1) Set the secondary functions of the ports required for executing the external memory transfer instruction. (P47MOD, P8MOD, P9AMOD)

(2) Set both P83DIR (bit 3 of P8DIR) and P82DIR (bit 2 of P8DIR) to "1".

(3) Set both P83 (bit 3 of P8D) and P82 (bit 2 of P8D) to "1".

(4) Execute the instruction -

MOVXB obj, [RA]

or

MOVXB obj, xadr16

Figure 11-3 shows the timing of reading data from the external memory.
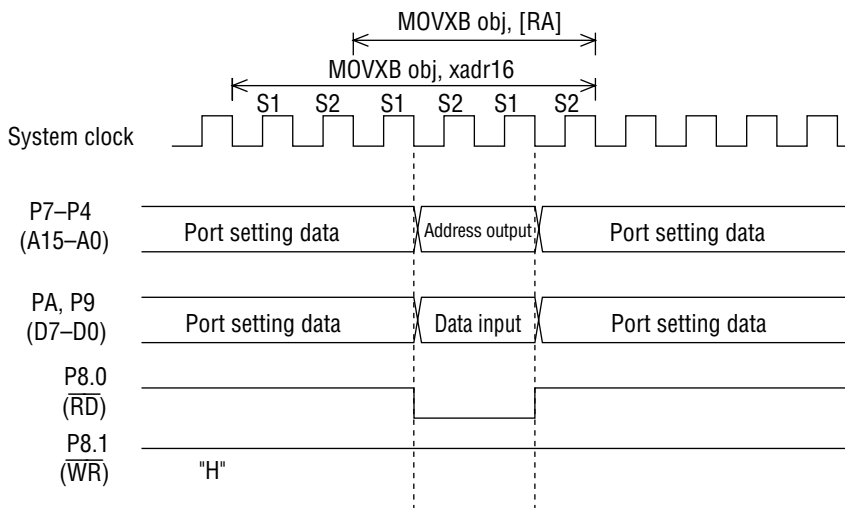
Figure 11-3 Timing of Reading from the External Memory

11.7 Reading from the Voice ROM inside the Chip

The ML63326 has a voice ROM area inside the chip, and it is possible to set character data in this area. Since a ROM area of 128 Kbytes is present (0H–1FFFFH), PF.0 is assigned as the MSB of the address.

Use the following procedure for reading data from the internal voice ROM area.

(1) Set the secondary functions of the ports required for executing the external memory transfer instruction. (P47MOD, P8MOD, P9AMOD)

(2) Set both P83DIR (bit 3 of P8DIR) and P82DIR (bit 2 of P8DIR) to "1".

(3) Set P83 (bit 3 of P8D) to "0" and P82 (bit 2 of P8D) to "1".

(4) Set PF0DIR (bit 0 of PFDIR) to "1".

(5) Set PF0 (bit 0 of PFD) to an address that can be read by positive logic.

(6) Execute the instruction -

   MOVXB obj, [RA]

   or

   MOVXB obj, xadr16

   The timing of reading is the same as that of reading from the external memory (Figure 11-3).

⚠ Note :

In the condition of P83 = "0" and P82 = "1", the external memory access ports cannot be used as normal ports.

When using the external memory access ports as normal ports, use in the condition of P83 = "0" and P82 = "0".

11.8 Writing to External Memory

Use the following procedure for writing data to the external memory.

(1) Set the secondary functions of the ports required for executing the external memory transfer instruction. (P47MOD, P8MOD, P9AMOD)

(2) Set both P83DIR (bit 3 of P8DIR) and P82DIR (bit 2 of P8DIR) to "1".

(3) Set both P83 (bit 3 of P8D) and P82 (bit 2 of P8D) to "1".

(4) Set PD3DIR (bit 3 of PDDIR) to "1".

(5) Set PD3 (bit 3 of PDD) to "1".

(6) Execute the instruction -

MOVXB [RA], obj

or

MOVXB xadr16, obj

(7) When writing is finished, set PD3 (bit 3 of PDD) to "0".

The timing of writing data to the external memory is shown in Figure 11-4.
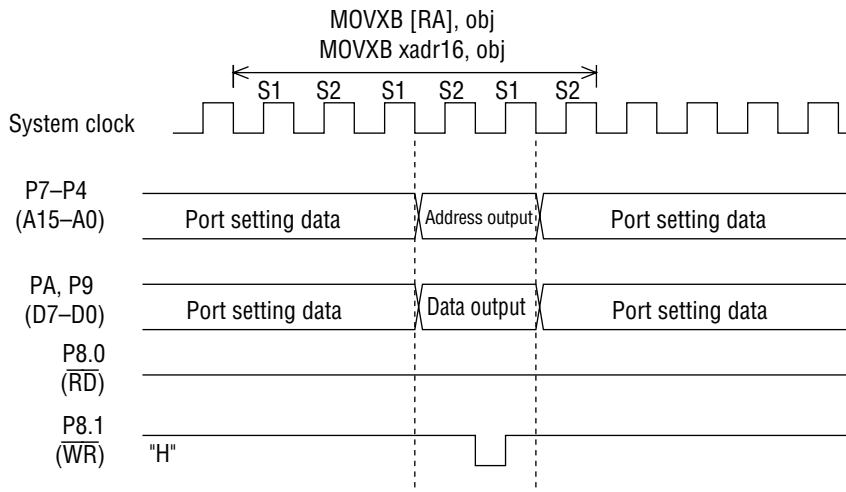
Figure 11-4 Timing of Writing Data to the External Memory

Melody Driver (MELODY63K)

Chapter 12 Melody Driver (MELODY63K)

12.1 Overview

The ML63326 has a melody circuit and buzzer circuit in the microcontroller section.

While automatically reading melody data in ROM (program memory) as specified by an MSA instruction, the melody circuit outputs a melody signal via the MD and MDB pins or DACOUT and AOUT pins.

The melody circuit can select 29 different tones, 63 different tone lengths, and 15 different tempos.

The buzzer circuit has four different buzzer output modes at a frequency of 4 kHz. The buzzer driver signal is output via the MD and MDB pins or DACOUT and AOUT pins.

Melody output is a higher priority operation than buzzer output.

12.2 Melody Driver Configuration

The melody driver configuration is shown in Figure 12-1.
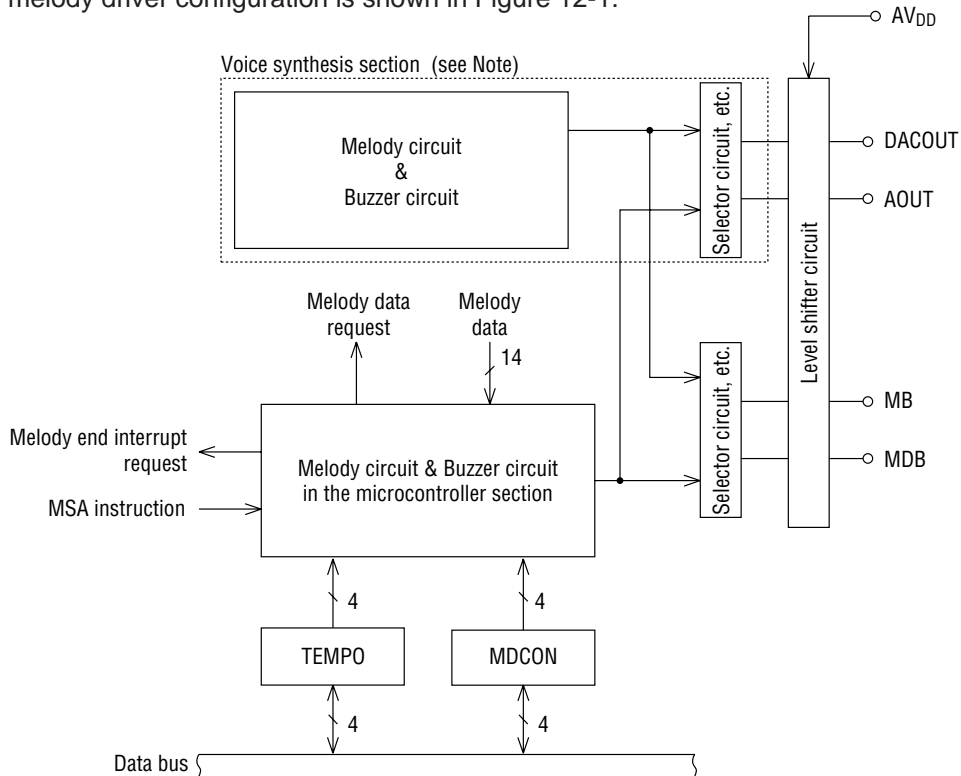
Figure 12-1 Melody Driver Configuration

⚠ Note:

See Chapter 13, "Voice Synthesis" for details of the voice synthesis section.

12.3 Melody Driver Registers

(1) Tempo Register (TEMPO)

TEMPO is a 4-bit special function register (SFR) that sets the tempo of the melody driver.

	bit 3	bit 2	bit 1	bit 0
TEMPO (096H) (R/W)	TMP3	TMP2	TMP1	TMP0

Melody tempo select

bit 3 bit 2 bit 1 bit 0
  0   0   0   0 : ♩ = 480 (initial value)
  0   0   0   1 : ♩ = 480
  0   0   1   0 : ♩ = 320
  0   0   1   1 : ♩ = 240
  0   1   0   0 : ♩ = 192
  0   1   0   1 : ♩ = 160
  0   1   1   0 : ♩ ≒ 137
  0   1   1   1 : ♩ = 120
  1   0   0   0 : ♩ ≒ 107
  1   0   0   1 : ♩ = 96
  1   0   1   0 : ♩ ≒ 87
  1   0   1   1 : ♩ = 80
  1   1   0   0 : ♩ ≒ 74
  1   1   0   1 : ♩ ≒ 69
  1   1   1   0 : ♩ = 64
  1   1   1   1 : ♩ = 60
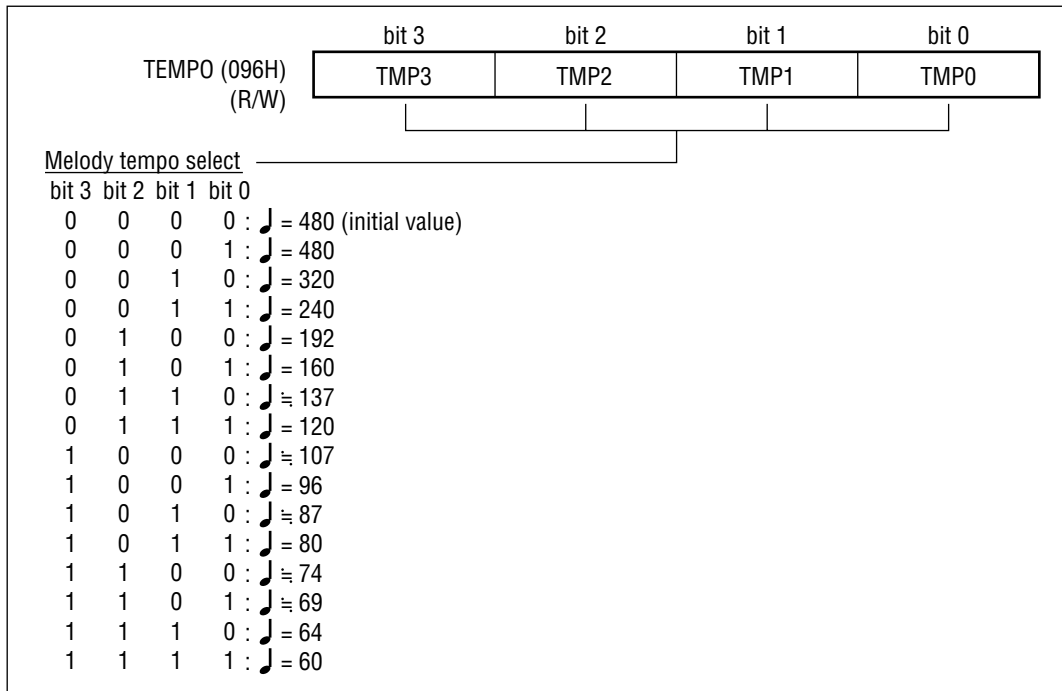
(2) Melody Driver Control Register (MDCON)

MDCON is a 4-bit special function register (SFR) that controls output of the melody driver.

	bit 3	bit 2	bit 1	bit 0
MDCON (097H) (R/W)	MSF	EMBD	MBM1	MBM0

Melody status flag
 0 : Melody stopped (initial value)
 1 : Melody output

Buzzer output ON/OFF control
 0 : Buzzer output OFF (initial value)
 1 : Buzzer output ON

Buzzer mode select
bit 1 bit 0
  0   0 : Intermittent tone 1 (initial value)
  0   1 : Intermittent tone 2
  1   0 : Single tone
  1   1 : Continuous tone
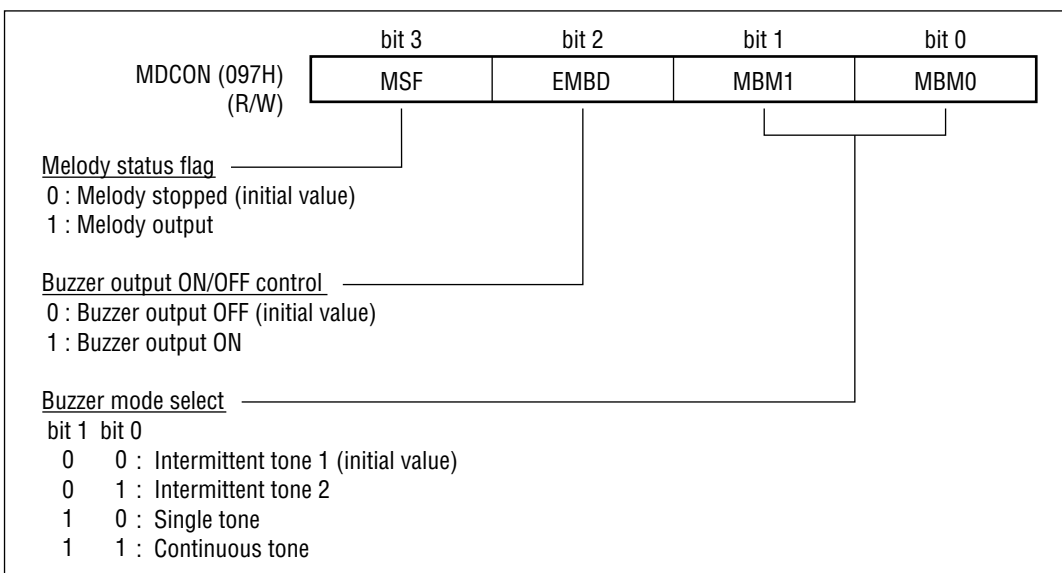
bit 3: MSF

This flag indicates the melody output status.

When an MSA instruction starts the melody, MSF is set to "1". After output of the last melody data (END bit is "1"), MSF is cleared to "0".

Setting MSF to "0" during melody output stops the melody output forcibly. If forcibly stopped, the melody output cannot be restarted from the address at which it was stopped.

At system reset, MSF is cleared to "0".

⚠ Note:

If it is required to set MSF (bit 3 of MDCON) to "0" during melody output to forcibly stop the melody output, describe the program as follows:

```
;*Program part***********
   DI                           ; 0. Disable master interrupt.
   MSA   MDSTOP_DATA            ; 1. Write melody end data to the melody circuit.
   MOV  A,#0                    ; 2. Set the MSF flag to "0".
   MOV  MDCON,A                 ;
   MOV  A,#1101b                ; 3. Clear melody interrupt request (QMD).
   AND  IRQ0,A                  ;
   EI                           ; 4. Enable master interrupt (MIE).
;*ROM table data part****
;*Provide two items of melody data so that a melody will always be terminated even if a melody
;*request is issued twice.
MDSTOP_DATA:
   DW   8000H                   ; Silence data 1
   DW   8000H                   ; Silence data 2
;***********************
;
```

bit 2: EMBD

This bit turns the buzzer output ON or OFF.

At system reset, EMBD is cleared to "0" and buzzer output is turned OFF.

In the single tone output mode, setting EMBD to "1" turns ON the buzzer output. After the second falling edge of the 32 Hz output, EMBD is cleared to "0" and buzzer output is turned OFF.

If melody output is started during buzzer output, EMBD is cleared to "0" and the buzzer output is turned OFF.

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bit 1, 0: MBM1, MBM0

> These bits select the buzzer output mode.
> Output of two types of intermittent tones, a single tone or a continuous tone can be selected.
> At system reset, MBM1 and MBM0 are cleared to "0", selecting output of intermittent tone 1.

Buzzer output mode	Waveform
Intermittent tone 1	Intermittent tone waveform synchronized to 8 Hz output of time base counter
Intermittent tone 2	Intermittent tone waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal output of the time base counter
Single tone	Single tone waveform beginning when EMBD is set to "1" until second falling edge of 32 Hz output of time base counter
Continuous tone	Continuous tone waveform that is constant while EMBD is "1"

Figure 12-2 shows the output waveforms of the melody driver output pins.
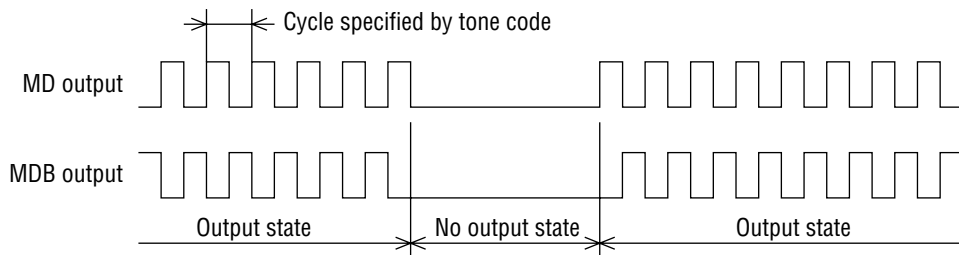
Figure 12-2 Output Waveforms of Melody Driver Output Pins

12.4 Melody Circuit Operation

After the melody tempo is set in the tempo register (TEMP), execution of an MSA instruction will start operation of the melody circuit.

The melody circuit outputs melody data while automatically reading melody data in ROM (program memory) as specified by an MSA instruction. When the last melody data is read (END bit is "1"), the melody circuit generates a melody end interrupt request. At this time, if an MSA instruction is executed, after the last melody data is output, melody output will continue from the melody data specified by the MSA instruction. If an MSA instruction is not executed, the melody output will stop after the last melody data is output.

MSF (bit 3 of MDCON) is a flag indicating the melody output status. When MSF is "1", the melody is being output, and when "0", the melody is stopped. Setting MSF to "0" during melody output stops the melody output forcibly. To stop melody output forcibly, describe the program in accordance with the description provided in the Note on page 12-3. If forcibly stopped, the melody output cannot be restarted from the address at which it was stopped.

12.4.1 Tempo Data

Tempo data defines the basic tone length. Tempo data is set in the tempo register (TEMPO).
The tempos (number of counts per minute) set by TEMPO are shown in Table 12-1.

Table 12-1 Melody Tempo

TEMPO					Tempo
TP3–0	TP3	TP2	TP1	TP0	
0H	0	0	0	0	♩ = 480
1H	0	0	0	1	♩ = 480
2H	0	0	1	0	♩ = 320
3H	0	0	1	1	♩ = 240
4H	0	1	0	0	♩ = 192
5H	0	1	0	1	♩ = 160
6H	0	1	1	0	♩ ≒ 137
7H	0	1	1	1	♩ = 120
8H	1	0	0	0	♩ ≒ 107
9H	1	0	0	1	♩ = 96
AH	1	0	1	0	♩ ≒ 87
BH	1	0	1	1	♩ = 80
CH	1	1	0	0	♩ ≒ 74
DH	1	1	0	1	♩ ≒ 69
EH	1	1	1	0	♩ = 64
FH	1	1	1	1	♩ = 60

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12.4.2 Melody Data

Melody data is 14-bit format data in the program ROM defining tone, tone length and end tone. The melody data format is indicated in Figure 12-3.

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
END	—*	L5	L4	L3	L2	L1	L0	—*	N6	N5	N4	N3	N2	N1	N0

End bit

Tone length code   Tone code

* Bits 14 and 7 may be either "0" or "1".
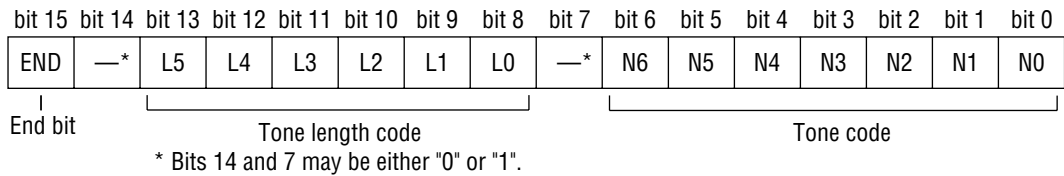
Figure 12-3 Melody Data Format

(1) Tone code

The tone code is set in bits 6 through 0 of the melody data. The frequencies that can be output by the melody circuit are defined as:

$$\frac{65536}{(N + 2)} \text{ Hz} \text{ (where N is an integer from 4 to 127)}$$

The relation between N and tone code bits is:

$$N = 2^6 N6 + 2^5 N5 + 2^4 N4 + 2^3 N3 + 2^2 N2 + 2^1 N1 + 2^0 N0$$

If N6 through N2 are all set to "0", there is no melody output for the time specified by the tone length code. Values for N1 and N0 are irrelevant.

Table 12-2 indicates the relations between tones and tone codes.

Table 12-2 Tone and Tone Code Correspondence

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	0	1	1	73H
D^1	590	1	1	0	1	1	0	1	6DH
Dis^1	624	1	1	0	0	1	1	1	67H
E^1	662	1	1	0	0	0	0	1	61H
F^1	705	1	0	1	1	0	1	1	5BH
Fis^1	745	1	0	1	0	1	1	0	56H
G^1	790	1	0	1	0	0	0	1	51H
Gis^1	840	1	0	0	1	1	0	0	4CH
A^1	886	1	0	0	1	0	0	0	48H
Ais^1	936	1	0	0	0	1	0	0	44H
B^1	993	1	0	0	0	0	0	0	40H
C^2	1057	0	1	1	1	1	0	0	3CH
Cis^2	1111	0	1	1	1	0	0	1	39H
D^2	1192	0	1	1	0	1	0	1	35H

Table 12-2 Tone and Tone Code Correspondence (continued)

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
Dis^2	1260	0	1	1	0	0	1	0	32H
E^2	1338	0	1	0	1	1	1	1	2FH
F^2	1394	0	1	0	1	1	0	1	2DH
Fis^2	1490	0	1	0	1	0	1	0	2AH
G^2	1560	0	1	0	1	0	0	0	28H
Gis^2	1680	0	1	0	0	1	0	1	25H
A^2	1771	0	1	0	0	0	1	1	23H
Ais^2	1872	0	1	0	0	0	0	1	21H
B^2	1986	0	0	1	1	1	1	1	1FH
C^3	2114	0	0	1	1	1	0	1	1DH
D^3	2341	0	0	1	1	0	1	0	1AH
Dis^3	2521	0	0	1	1	0	0	0	18H
E^3	2621	0	0	1	0	1	1	1	17H
Fis^3	2979	0	0	1	0	1	0	0	14H

(2) Tone length code

The tone length code is set in melody data bits 13 through 8.

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Table 12-3 indicates the relation between tone length and tone length code (L5 to L0).

The tone length that is set during execution of the MSA instruction is shorter by approximately 1 to 3 ms.

When all bits are set to "0", the tone length will be the same as the minimum tone length (the tone length with only L0 set to "1").

Table 12-3 Tone Length and Tone Length Code Correspondence

Tone length	Tone length code						
	L5	L4	L3	L2	L1	L0	L5–L0
(half note)	1	1	1	1	1	1	3FH
(dotted quarter note)	1	0	1	1	1	1	2FH
(quarter note)	0	1	1	1	1	1	1FH
(dotted eighth note)	0	1	0	1	1	1	17H
(eighth note)	0	0	1	1	1	1	0FH
(dotted sixteenth note)	0	0	1	0	1	1	0BH
(sixteenth note)	0	0	0	1	1	1	07H
(dotted thirty-second note)	0	0	0	1	0	1	05H
(thirty-second note)	0	0	0	0	1	1	03H
(dotted sixty-fourth note)	0	0	0	0	1	0	02H
(sixty-fourth note)	0	0	0	0	0	1	01H

Tone lengths specified by the tone length code and the tempo data are expressed by the following:

$1.953125 \times (TP + 1) \times (L + 1)$ ms   (where TP is an integer from 1 to 15, and L is an integer from 1 to 63)

TP is a value set in the tempo register (TEMPO), and has the following bit correspondence:

$TP = 2^3 TP3 + 2^2 TP2 + 2^1 TP1 + 2^0 TP0$

L is set by the tone length code and has a bit correspondence with the tone length code as:

$L = 2^5 L5 + 2^4 L4 + 2^3 L3 + 2^2 L2 + 2^1 L1 + 2^0 L0$

(3) END bit

The END bit is set in bit 15 of the melody data. When the output of the last melody data is started (END bit is "1"), the melody circuit generates a melody end interrupt request, and stops the melody after the last melody data is output.

12.4.3 Melody Circuit Application Example

An example melody is shown in Figure 12-4.

Table 12-4 lists the note codes for the melody shown in Figure 12-4.

Figure 12-4 Example Melody

Table 12-4 Note Code Table

Note		Note code															Hex
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		END	—*	L5	L4	L3	L2	L1	L0	—*	N6	N5	N4	N3	N2	N1	N0	
	G^2	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	2F28H
	D^2	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0F35H
	G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
	—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0700H
	D^2	0	0	0	0	0	1	1	1	0	0	1	1	0	1	0	1	0735H
	G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
	—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0700H
	A^2	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0723H
	B^2	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1	3F1FH
	G^2	1	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0	BF28H

* Bits 14 and 7 may be "0" or "1", but in this example they are shown as "0".

12.5 Buzzer Circuit Operation

When EMBD (bit 2 of MDCON) is set to "1", a buzzer driver signal is sent to the melody driver output pins (MD, MDB) or DACOUT and AOUT pins.

Four buzzer output modes can be selected by MBM1 (bit 1 of MDCON) and MBM0 (bit 0 of MDCON): two types of intermittent tones, a single tone, or a continuous tone output. The buzzer output frequency is 4 kHz and has a 50% duty ratio.

In the intermittent tone 1 mode, a waveform synchronized to the 8 Hz output of the time base counter is output.

In the intermittent tone 2 mode, a waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal of the time base counter is output.

In the single tone mode, output starts in synchronization with the rising edge of EMBD. At the second falling edge of the 32 Hz output of the time base counter, EMBD is cleared to "0" and output is stopped.

In the continuous tone mode, output is continued while EMBD is "1".

While the melody is being output (MSF (bit 3 of MDCON) = "1"), the buzzer output is turned OFF. If melody output is started during buzzer output, EMBD is cleared to "0", the buzzer output is stopped, and melody output is given priority.

Figure 12-5 shows the output waveforms of each mode. Shaded sections indicate the 4 kHz output frequency.

(a) MBM1 = 0, MBM0 = 0   (intermittent tone 1)

(b) MBM1 = 0, MBM0 = 1   (intermittent tone 2)

(c) MBM1 = 1, MBM0 = 0   (single tone)

(d) MBM1 = 1, MBM0 = 1   (continuous tone)
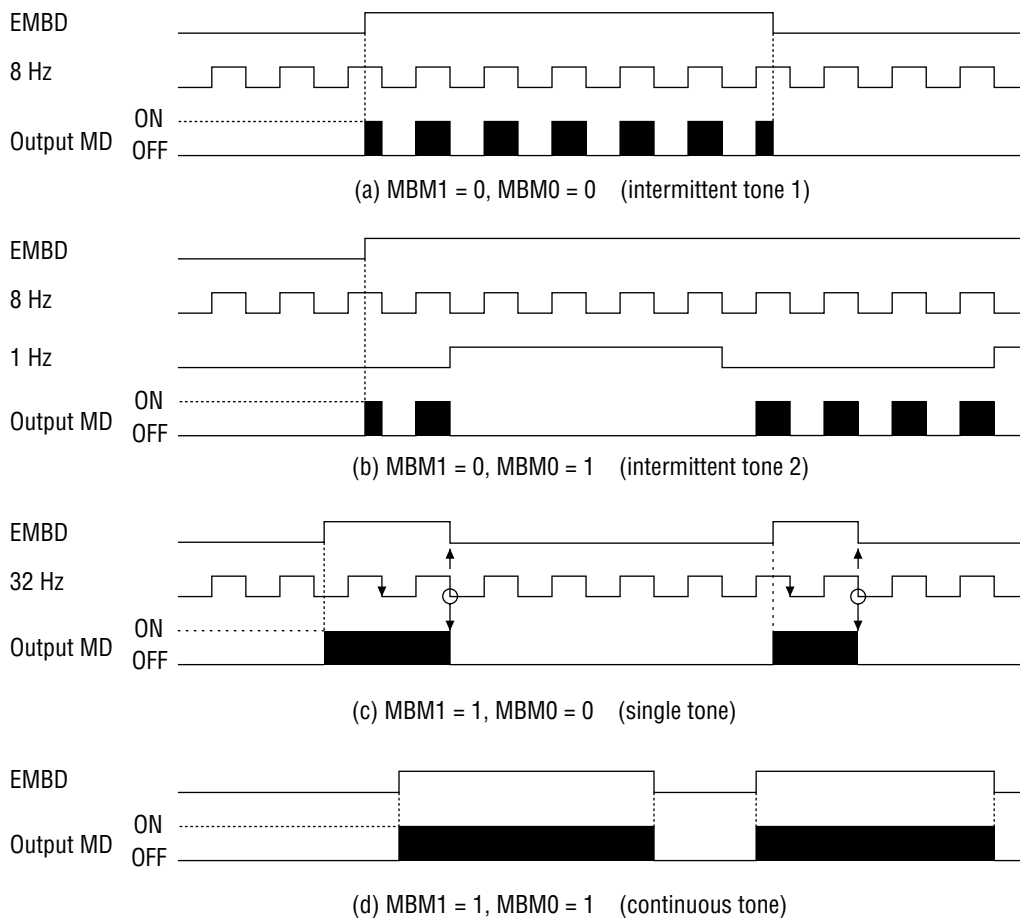
Figure 12-5 Buzzer Driver Output Waveforms in Each Output Mode

12.6 Melody/Buzzer Output Selector Circuit

The melody output and the buzzer output can be made respectively at pins MD and MDB or pins DACOUT and AOUT. It is possible to select which pins to output each of these waveforms using PD1 (bit 1 of PDD) and PD0 (bit 0 of PDD).

Table 12-5 shows the relationship between the statuses of PD1 and PD0 and the output waveforms at each of these pins.

Table 12-5 Relationship between the PD1 and PD0 Statuses and Pin Outputs

PD1	PD0	Pins MD and MDB	Pins DACOUT and AOUT
0	0	Microcontroller section melody/buzzer output	Voice output*
1	0	Microcontroller section melody/buzzer output	Voice synthesis section melody/buzzer output*
1	1	Voice synthesis section melody/buzzer output*	Microcontroller section melody/buzzer output

*See Chapter 13, "Voice Synthesis" for details of the voice synthesis section.

⚠ Note:

Before starting the melody/buzzer output, always make sure that the settings of PD1 and PD0 have been made.

When making melody/buzzer output of the microcontroller section at pins DACOUT and AOUT with PD0 and PD1 both set to "1", release the reset state of the voice synthesis section by setting PC1 (bit 1 of PCD) to "1".

12.7 Differences with Voice Synthesis Section Melody/Buzzer Output

While the ML63326 has melody drivers built into the microcontroller section and the voice synthesis section, the driving methods are different in these two sections.

The differences in the melody outputs of the microcontroller section and the voice synthesis section are shown in Table 12-6 and the differences in the buzzer outputs are shown in Table 12-7. Further, see Chapter 13, "Voice Synthesis" for details of the melody/buzzer outputs of the voice synthesis section.

Table 12-6 Differences in the Melody Outputs of the Microcontroller Section and the Voice Synthesis Section

Item	Microcontroller section	Voice synthesis section
Start of melody	Execute the MSA instruction.	Set the phrase address in P2D and P3D, and transfer it to the voice synthesis section.
Preparation of the next sound and termination of melody	Not necessary. Automatic sound production is made until the last melody data is played completely.	Same as at left.
Forced termination of melody	Set MSF (bit 3 of MDCON) to "0".	Set the stop code in P2D and P3D, and transfer it to the voice synthesis section.
Forced starting of melody	Set MSF (bit 3 of MDCON) to "1". (Starts with the sound next to the one that was forcibly terminated earlier.)	Not possible.
Interrupt	The melody interrupt (MDINT) is generated after reading the last melody data into the melody section.	The voice output interrupt (VOINT) is generated when the transfer of one phrase address is completed and the transfer of the next phrase address is enabled.
Control method as seen from the CPU	The melody output state can be monitored using MSF (bit 3 of MDCON). It is possible to recognize the reading in of the final data by the generation of the interrupt (MDINT).	The melody output state can be monitored using P10 (bit 0 of P1D). Judgment of whether or not the next sound can be set is made using P11 (bit 1 of P1D). The generation of the interrupt (VOINT) is used for judging whether the next sound can be set.

Table 12-7 Differences in the Buzzer Outputs of the Microcontroller Section and the Voice Synthesis Section

Item	Microcontroller section	Voice synthesis section
Buzzer start	Set EMBD (bit 1 of MDCON) to "1".	Set the phrase address in P2D and P3D, and transfer it to the voice synthesis section.
Buzzer stop	Set EMBD (bit 1 of MDCON) to "0" (excepting during the single tone mode).	Set the stop code in P2D and P3D, and transfer it to the voice synthesis section.

Voice Synthesis

Chapter 13 Voice Synthesis

13.1 Overview

The ML63326 has a built-in voice synthesis section. This voice synthesis section has the functions of melody output and buzzer output in addition to voice output. Each of these types of output data is stored in the internal 1-Mbit (128 Kbytes) mask ROM or in the externally connected memory of up to a maximum of 4 Mbits (512 Kbytes).

13.2 Voice Synthesis Section Configuration

Figure 13-1 shows the configuration of the voice synthesis section.

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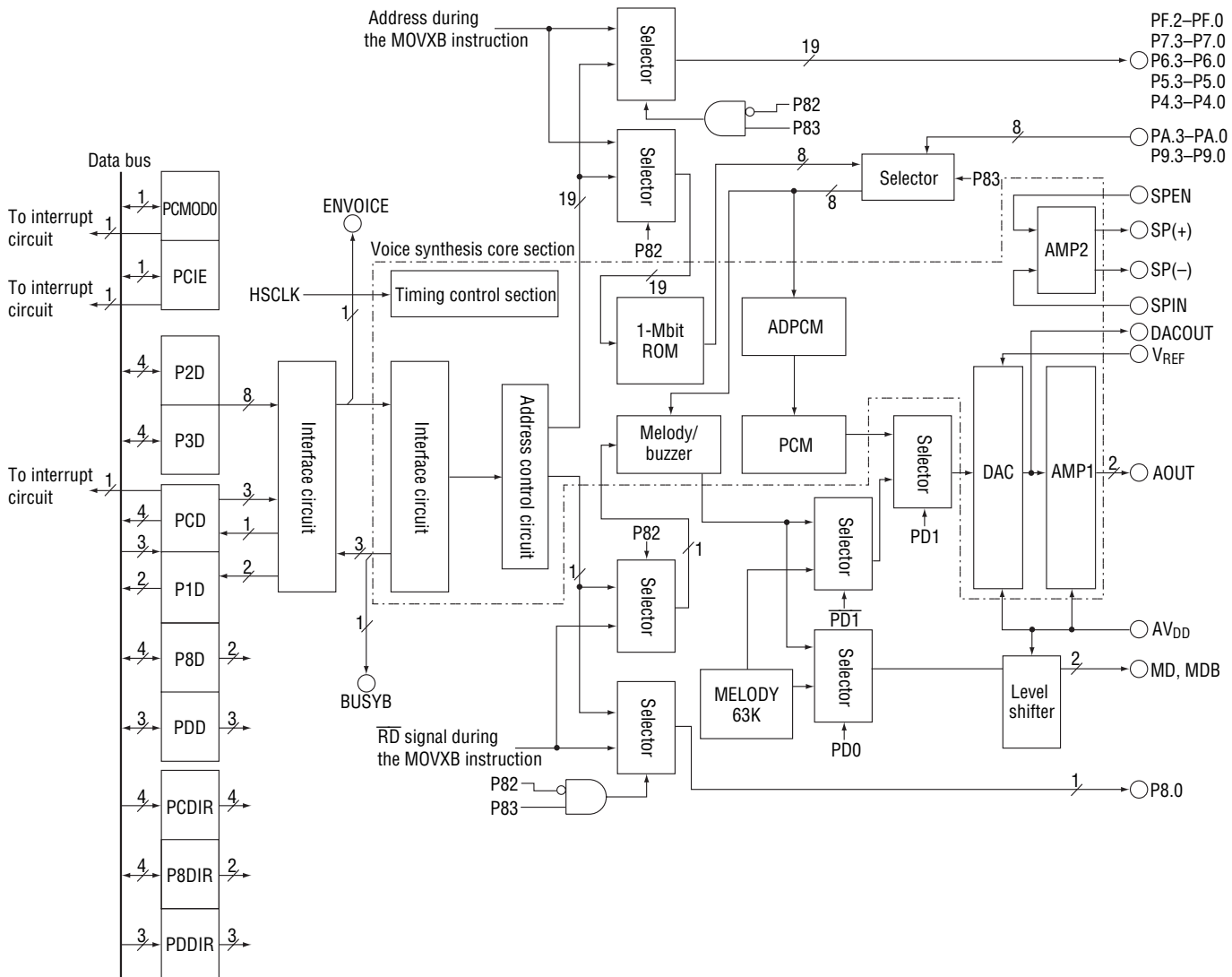
Figure13-1 Voice Synthesis Section Configuration

13.3 Registers Related to the Voice Synthesis Section

(1) Phrase setting register 0 (P2D), phrase setting register 1 (P3D)

P2D and P3D are 4-bit special function registers (SFRs) for setting the 8-bit phrase address.

P33 (bit 3 of P3D) is the MSB and P20 (bit 0 of P2D) is the LSB of the address.

All these bits are reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
P2D (002H) (R/W)	P23	P22	P21	P20

	bit 3	bit 2	bit 1	bit 0
P3D (003H) (R/W)	P33	P32	P31	P30

(2) Voice synthesis control register 0 (PCD)

PCD is a 4-bit special function register (SFR) for controlling the voice synthesis section. All bits are reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
PCD (00CH) (R/W)	PC3	PC2	PC1	PC0

bit 3: PC3

This bit is for monitoring the signal that gets inverted every time there is a rising edge in the signal enabling the transfer of phrase data of the next sound from the voice synthesis section. This is a read-only bit and all write operations to this bit are ignored.

This bit is reset to "0" at a system reset.

bit 2: PC2

This is the signal corresponding to the chip select ($\overline{CS}$) signal of the voice synthesis section.

This bit is reset to "0" at a system reset.

bit 1: PC1

This is the signal corresponding to the resetting of the voice synthesis section, and is also simultaneously output at the ENVOICE pin.

This bit is reset to "0" at a system reset, and the voice synthesis section goes into the reset state.

bit 0: PC0

This is the signal for starting the serial transfer of the phrase address to the voice synthesis section, and the transfer is started when this bit is changed from "1" to "0".

This bit is reset to "0" at a system reset.

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(3) Voice synthesis control register 1 (PCDIR)

PCDIR is a 4-bit special function register (SFR) for controlling the voice synthesis section. PCDIR is a write-only register and all read operations to this register are ignored.

When operating voice synthesis, set bits 2, 1 and 0 to "1" and bit 3 to "0".

All bits are reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
PCDIR (035H) (W)	PC3DIR	PC2DIR	PC1DIR	PC0DIR
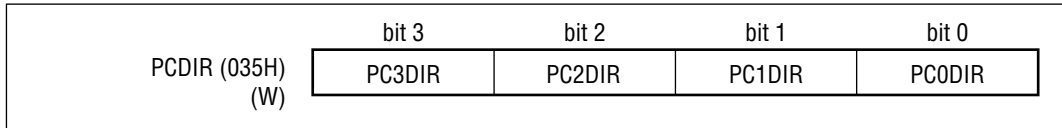
Refer to step ④ in Section 13.7.3, "Voice Output Procedure."

(4) Voice synthesis section monitor register (P1D)

P1D is a 4-bit special function register (SFR) for monitoring the signal output from the voice synthesis section. This is a read-only register and all write operations to this register are ignored.

The valid bits of this register are set to "1" at a system reset.

	bit 3	bit 2	bit 1	bit 0
P1D (001H) (R)	—	—	P11	P10
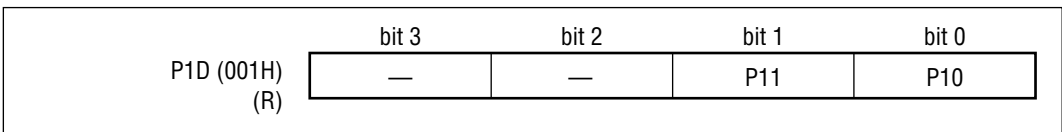
bit 1: P11

This is the bit that directly monitors the signal from the voice synthesis section that enables the transfer of the next sound phrase data.

This bit is set to "1" at a system reset.

bit 0: P10

This is the bit that monitors the BUSYB signal of the voice synthesis section.

This bit is set to "1" at a system reset.

(5) Port 8 data register (P8D)

P8D is a 4-bit special function register (SFR) whose low-order 2 bits P80 and P81 set the output value (see Chapter 10, "Ports" for details).

The high-order 2 bits P82 and P83 of this register are used for selecting voice synthesis or the external memory transfer instruction, and for selecting the internal voice ROM area or the external memory area.

All these bits are reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
P8D (008H) (R/W)	P83	P82	P81	P80

Internal voice ROM area/external memory area select
 0: The internal voice ROM area is selected (initial value).
 1: The memory area external to the IC is selected.

Voice synthesis/external memory transfer instruction select
 0: Voice synthesis is selected (initial value).
 1: External memory transfer instruction is selected.
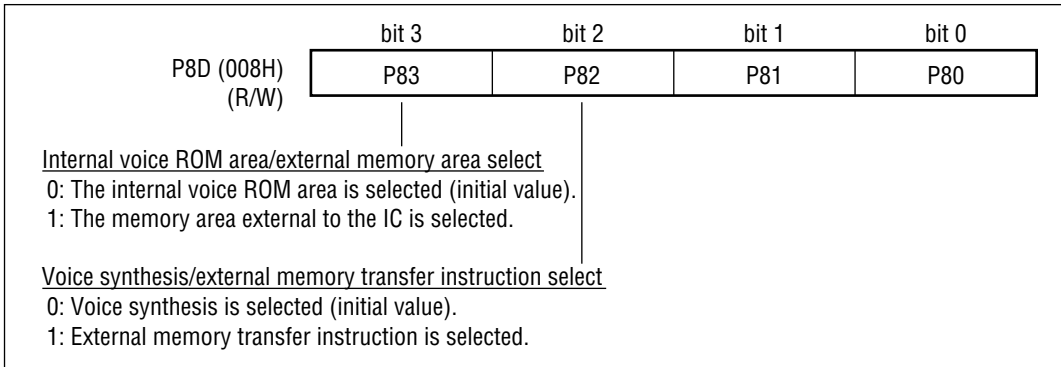
(6) Port 8 direction register (P8DIR)

P8DIR is a 4-bit special function register (SFR) whose low-order 2 bits specify the input/output direction of P80 and P81 (see Chapter 10, "Ports" for details).

The high-order 2 bits P83DIR and P82DIR of this register are used for selecting voice synthesis or the external memory transfer instruction, and for selecting the internal voice ROM area or the external memory area.

All these bits are reset to "0" at a system reset.

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	bit 3	bit 2	bit 1	bit 0
P8DIR (025H) (R/W)	P83DIR	P82DIR	P81DIR	P80DIR
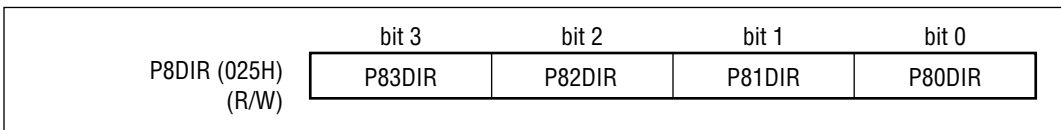
(7) Voice/melody-buzzer output control register 0 (PDD)

PDD is a 4-bit special function register (SFR) that is used for the control of the waveforms output at the DACOUT/AOUT pins and the MD/MDB pins, and is also used when a write operation is made to the external memory using the external memory transfer instruction.

The valid bits of this register are all reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
PDD (00DH) (R/W)	PD3	—	PD1	PD0

Register for setting the external memory transfer write instruction
0: Initial value
1: Set when a write operation is made to the external
   memory using the external memory transfer instruction.

DACOUT/AOUT pin output selection
0: Voice output (initial value)
1: Melody/buzzer output

MD/MDB pin output selection
0: Melody/buzzer output of the microcontroller section (initial value)
1: Melody/buzzer output of the voice synthesis section

bit 3: PD3

This bit should be set to "1" when a write operation is made to the external memory using the external memory transfer instructions. Reset this bit to "0" after the write operation has been completed.

This is a write-only bit and all read operations to this bit are ignored.

bit 1: PD1

This is the bit for selecting whether to output the voice output or the melody/buzzer output at the DACOUT/AOUT pins.

When this bit is set to "1", the melody/buzzer output is selected. The status of PD0 determines whether the melody/buzzer output of the microcontroller section or of the voice synthesis section is output. The relationship of the selection to the status of PD0 is given below.

Table 13-1 Relationship between the DACOUT/AOUT Outputs and the Bits PD1 and PD0

PD1	PD0	DACOUT/AOUT Output Status
1	0	The voice synthesis section melody/buzzer output is selected.
1	1	The microcontroller section melody/buzzer output is selected.

bit 0: PD0

This is the bit for selecting whether to output the melody/buzzer output of the microcontroller section or of the voice synthesis section at the MD/MDB pins.

When this bit is set to "0", the melody/buzzer output of the microcontroller section is output, and when set to "1", the melody/buzzer output of the voice synthesis section is output.

(8) Voice/melody-buzzer output control register 1 (PDDIR)

PDDIR is a 4-bit special function register (SFR) for controlling voice/melody-buzzer output. PDDIR is a write-only register and all read operations to this register are ignored.

The valid bits of this register are all reset to "0" at a system reset.

	bit 3	bit 2	bit 1	bit 0
PDDIR (03BH) (W)	PD3DIR	—	PD1DIR	PD0DIR
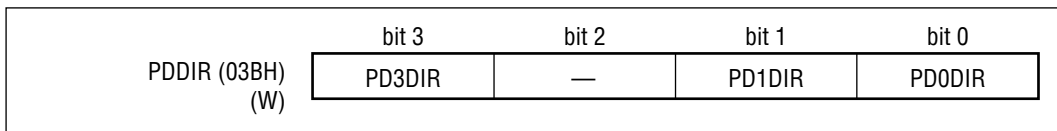
Refer to: step ① in Section 13.9.4, "Melody Output Procedure."

step ④ in Section 11.8, "Writing to External Memory."

(9) Voice synthesis interrupt mode register (PCMOD0)

PCMOD0 is a 4-bit special function register (SFR) for selecting the sampling frequency of the voice synthesis interrupt signal.

	bit 3	bit 2	bit 1	bit 0
PCMOD0 (037H) (R/W)	—	—	—	PCF

Selection of the voice synthesis interrupt sampling frequency
 0: Sampling at 128 Hz (initial value)
 1: Sampling at 4 kHz
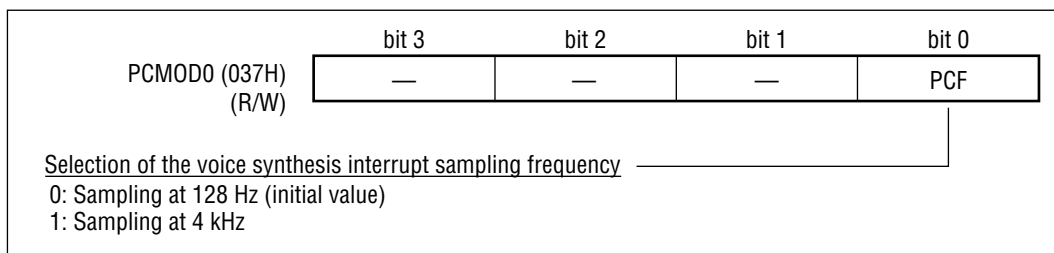
(10) Voice synthesis interrupt enable register (PCIE)

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PCIE is a 4-bit special function register (SFR) that enables and disables the voice synthesis interrupt.

	bit 3	bit 2	bit 1	bit 0
PCIE (036H) (R/W)	PC3IE	—	—	—

Voice synthesis interrupt disable/enable select
 0: Disabled (initial value)
 1: Enabled
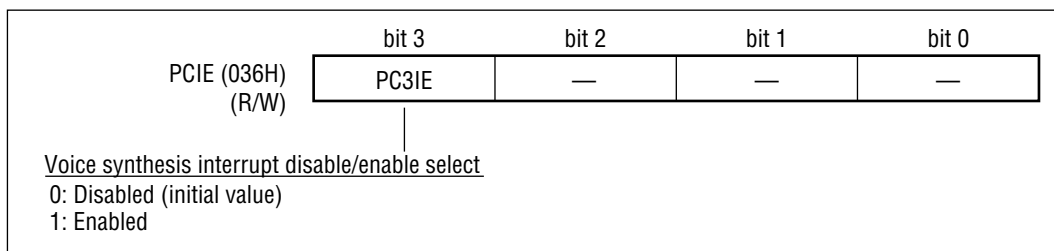
13.4 Voice ROM

13.4.1 Voice ROM Configuration

Figure 13-2 shows the configuration of the voice ROM.

The voice ROM is composed of the phrase address management area, the test data area, and the user data area.

In addition to the identification of voice/melody/buzzer, the method of reproduction in the case of voice synthesis, the setting of the sampling frequency, the voice data, the melody data, and the buzzer data are stored in the phrase address management area and the user data area.

The test data area is the area for carrying out tests of the voice synthesis functions and cannot be used by the end user.

The memory configuration is the same even when carrying out voice synthesis using an externally connected ROM. The maximum address of the externally connected ROM is 7FFFFH (512 Kbytes).
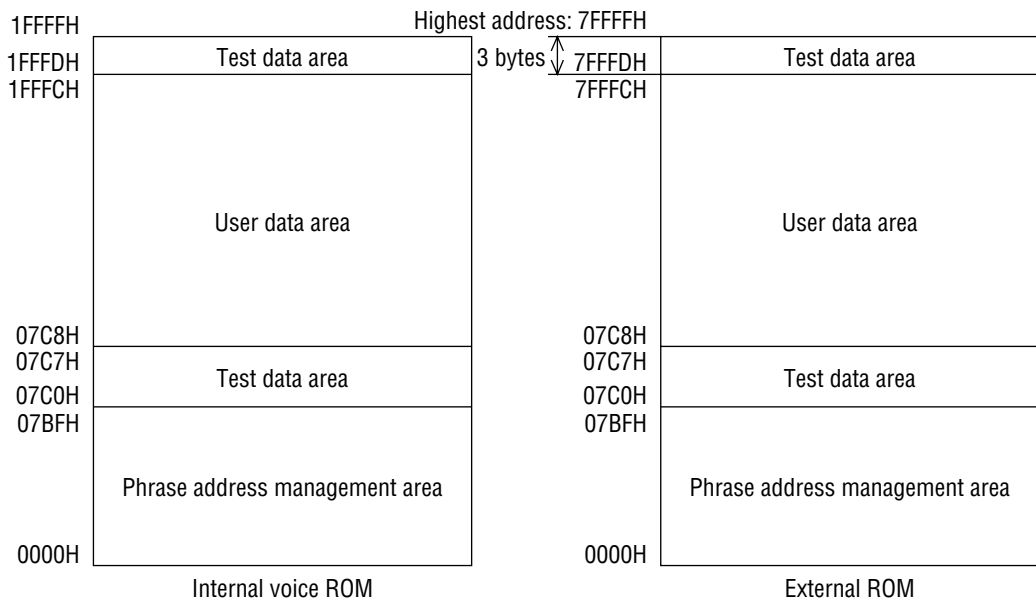
Figure 13-2 Voice ROM Configuration

13.4.2 Creation of Voice ROM Store Data

The voice ROM store data consists of the data stored in the phrase address management area and the user data area.

A dedicated voice analysis tool is used for creating the voice ROM store data. Follow the procedure given below for creating the voice ROM store data.

① Record the voice and determine the melody/buzzer sound.

② Determine the synthesized voice reproduction method and the sampling frequency.

   Determine the melody tempo.

   Determine the buzzer frequency and the output mode.

③ Determine the correspondence between the phrase address and the voice/melody/ buzzer sounds.

④ Convert the data to voice data using the voice analysis tool.

⑤ Voice data creation is completed.

⚠ Note:

The conversion to voice data using the voice analysis tool of step ④ is undertaken by Oki.

The determination of the different parameters in steps ① and ② are to be made by the customers.

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13.5 Voice Synthesis Section Clock Input Frequency

The clock used in the voice synthesis section is a high-speed clock supplied from the high-speed clock generator circuit and is basically intended to have frequency of 2.048 MHz.

When selecting the crystal oscillation mode, since the signal frequency is internally halved (1/2 frequency division), use a 4.096 MHz crystal.

When selecting the RC oscillation mode, since the oscillation waveform is used as it is, select the value of R_{OS} so that the frequency is in the range of 2 MHz to 1.8 MHz. However, in the case of RC oscillation, care should be taken because the frequency of oscillations varies due to changes in the voltage V_{DDH} (2 times the value of V_{DD2}) which is the power supply voltage of the high-speed clock generator circuit.

Table 13-2 shows the relationship between the voice synthesis section input frequency and the internal sampling frequencies.

Table 13-2 Relationship between the Voice Synthesis Section Input Clock Frequency and the Internal Sampling Frequencies

Input frequency	Internal sampling frequencies
2.048 MHz	4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, 16.0 kHz

When a different frequency signal is input, the sampling frequency changes in proportion to that signal frequency. For example, when the input clock signal frequency is 1.024 MHz, the sampling frequency will be half the sampling frequency given in Table 13-2.

13.6 Operation of the Voice Synthesis Section

The voice synthesis section has the functions of voice, melody, and buzzer outputs.

13.6.1 Description of Pins Related to Voice Synthesis

The DACOUT pin is the output pin of the 12-bit D/A converter, and the AOUT pin is the output pin of the amplifier whose input is the output of the 12-bit D/A converter. Both these pins are used for the output of voice as well as melody/buzzer sounds.

At a system reset, the DACOUT pin will be at the AV_{DD} level and the AOUT pin will be at the V_{SS} level.

The SPEN pin is the enable input pin for the amplifier which is intended for driving a piezoelectric speaker. When not using this amplifier, leave this SPEN pin open or tie it to GND. When using this amplifier, setting this pin to a "H" level only when the output is being made will reduce the supply current.

The SPIN pin is the input pin for the amplifier which is intended for driving a piezoelectric speaker. Connect this pin to GND when this amplifier is not used.

The SP($-$) pin is the negative side output pin for driving a piezoelectric speaker, and the SP($+$) pin is the positive side output pin. Both pins will be at the V_{SS} level at a system reset.

The MD/MDB pins are used for outputting the melody/buzzer output of the voice synthesis section or of the microcontroller section. At a system reset, both these outputs will be at a "L" level, and when the melody/buzzer output state is entered, the MDB pin outputs the opposite level of the MD pin.

The BUSYB pin normally outputs a "H" level (V_{DD}). It outputs a "L" level (0 V) when the voice synthesis section is in the output state.

The ENVOICE pin is the pin that outputs the level of PC1 (bit 1 of PCD), and is used for the RESET signal of the voice synthesis section. This pin will be at a "L" level at a system reset thereby putting the voice synthesis section in the reset state, and the voice synthesis section goes into the enabled state when this pin is set to a "H" level (V_{DD}).

The V_{REF} pin is the volume control function input pin that changes the amplitude of the output at DACOUT. When this pin is in the open condition, the 1/5 AV_{DD} voltage appears at this pin. Leave this pin open when not using the volume control function.

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13.6.2 Phrase Address and Stop Code

The phrase address specifies which data is to be selected from among the data set in the phrase address management area of the memory area to be accessed.

A maximum of 247 phrases can be set as the phrase address.

The stop code is the code that is transferred instead of the phrase address when forcibly terminating the voice, melody, or buzzer output. The data of all-zeroes is transferred as the stop code.

When the transfer of the stop code is completed, all the outputs are terminated and the DACOUT pin goes to the 1/2 AV_{DD} level.

Table 13-3 shows the stop code and examples of phrase addresses.

Table 13-3 Stop Code and Sample Phrase Addresses

MSB - - - LSB		Code description
0000	0000	Stop code
0000	0001	
0000	0010	
⋮		User specified phrase addresses
⋮		(247 phrases)
1111	0110	
1111	0111	
1111	1000	Test code*

*: The test code is used for testing the voice synthesis section and cannot be used by the customers.

13.7 Voice

During voice synthesis, the voice output at the DACOUT/AOUT pins is started by initiating the phrase with the voice setting from the interface circuit after storing the voice reproduction method, the sampling frequency, the starting and ending addresses, etc., in the phrase address management area.

The voice synthesis section automatically retrieves the voice data successively beginning from the starting address of the voice data stored in the memory, continuously outputs the voice, and stops the voice output after outputting the data of the ending address. The creation of voice data is made using the dedicated voice analysis tool.

13.7.1 Voice Reproduction Method

The ML63326 allows the user to select from the three methods of 4-bit ADPCM, 8-bit straight PCM, and 8-bit non-linear PCM so as to meet various types of sounds and voice.

13.7.1.1 4-Bit ADPCM Method

The ADPCM (Adaptive Differential Pulse Code Modulation) method varies the quantization width Δ, which is the fundamental unit, in an adaptive manner at every sample, and encodes 4-bit data, thereby greatly increasing the voice waveform tracking characteristics.

The conversion to ADPCM data is carried out by the analysis tool.

The size of the voice data becomes smaller if the ADPCM method is used for human voice, animals' sounds, and natural sounds.

13.7.1.2 8-Bit Straight PCM Method

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This is the best method among those offered in this LSI device for voice waveform tracking characteristics over the entire voice region. This method is suitable when there are abrupt changes in the waveform (such as in sound effects) or for pulse type waveforms.

13.7.1.3 8-Bit Nonlinear PCM

This is the method of reproduction in which the area near the center of the waveform is reproduced with a sound quality equivalent to 10 bits. This method is suitable for improving the sound quality of sounds with low volumes.

The conversion to 8-bit nonlinear PCM is made using the analysis tool.

13.7.2 Forcible Stopping of Voice Output

To forcibly stop the voice output halfway, transfer the stop code instead of transferring the phrase address. When the transfer of the stop code is completed, the voice output is stopped (BUSYB = "H"), and the DACOUT/AOUT pins go to the 1/2 AV_{DD} level.

13.7.3 Voice Output Procedure

Follow the procedure given below when outputting voice. (Example using voice synthesis interrupt)

① Select the output from DACOUT/AMPOUT.

- Set PD1DIR and PD0DIR (bit 1 and bit 0 of PDDIR) to "1".

- Set PD1 (bit 1 of PDD) to "0", and PD0 (bit 0 of PDD) to "0".

② Make the selection of voice synthesis/external memory transfer instruction.

- Set P82DIR (bit 2 of P8DIR) to "1".

- Set P82 (bit 2 of P8D) to "0".

③ Select the internal voice ROM or the external memory.

- Set P83DIR (bit 3 of P8DIR) to "1".

- When using the internal voice ROM: Set P83 (bit 3 of P8D) to "0".

- When using the external memory: Set P83 to "1".

Note: Since the port F is used when the external memory exceeds 64 Kbytes, make the setting of the corresponding PFDIR register to the output mode.

④ Make the setting of PCDIR.

- Set PC2DIR, PC1DIR, and PC0DIR all to "1".

⑤ Set PC2 (bit 2 of PCD) to "1" ($\overline{CS}$ of the voice synthesis section is disabled).

⑥ Enable high-speed oscillation.

- For the crystal oscillation mode: Set bit 2 and bit 1 of FCON (062H) to "1".

- For the RC oscillation mode: Set bit 1 of FCON (062H) to "1".

Note: Wait for 10 ms for crystal oscillation and 5 ms for RC oscillation so that the high-speed oscillation waveform becomes stable.

⑦ Enable the acceptance of voice synthesis interrupts.

- Set bit 0 of PCMOD0 to "1" (4 kHz sampling).

- Set bit 3 of PCIE to "1".

- Set bit 3 of IE0 to "1".

- Set MIEF to "1".

⑧ Set PC1 (bit 1 of PCD) to "1" (releasing the reset state of the voice synthesis section).

⑨ Set the phrase address in P3D and P2D. (P33 is the MSB and P20 is the LSB.)

⑩ Set PC2 (bit 2 of PCD) to "0" ($\overline{CS}$ of the voice synthesis section is enabled).

⑪ First set PC0 (bit 0 of PCD) to "1" and then reset it to "0" (start of transfer).

The serial transfer of the phrase address is started.

⑫ The voice is output and a voice synthesis interrupt is generated.

⑬ Process the interrupt.

   • Set EVI (bit 3 of IE0) to "0".

   • Set PC2 (bit 2 of PCD) to "1".

⑭ For reproducing the second and subsequent phrases, first set EVI (bit 3 of IE0) to "1", and repeat steps ⑨ to ⑬ after enabling the voice synthesis interrupt.

⑮ Carry out the following settings for terminating the voice output.

   • Set PC1 (bit 1 of PCD) to "0" (the voice synthesis section is put in the reset state).

   • Stop the high-speed oscillation so as to reduce the supply current.

   (Reset ENOSC (bit 1 of FCON) to "0".)

Figure 13-3 shows the timing during voice synthesis output.

13
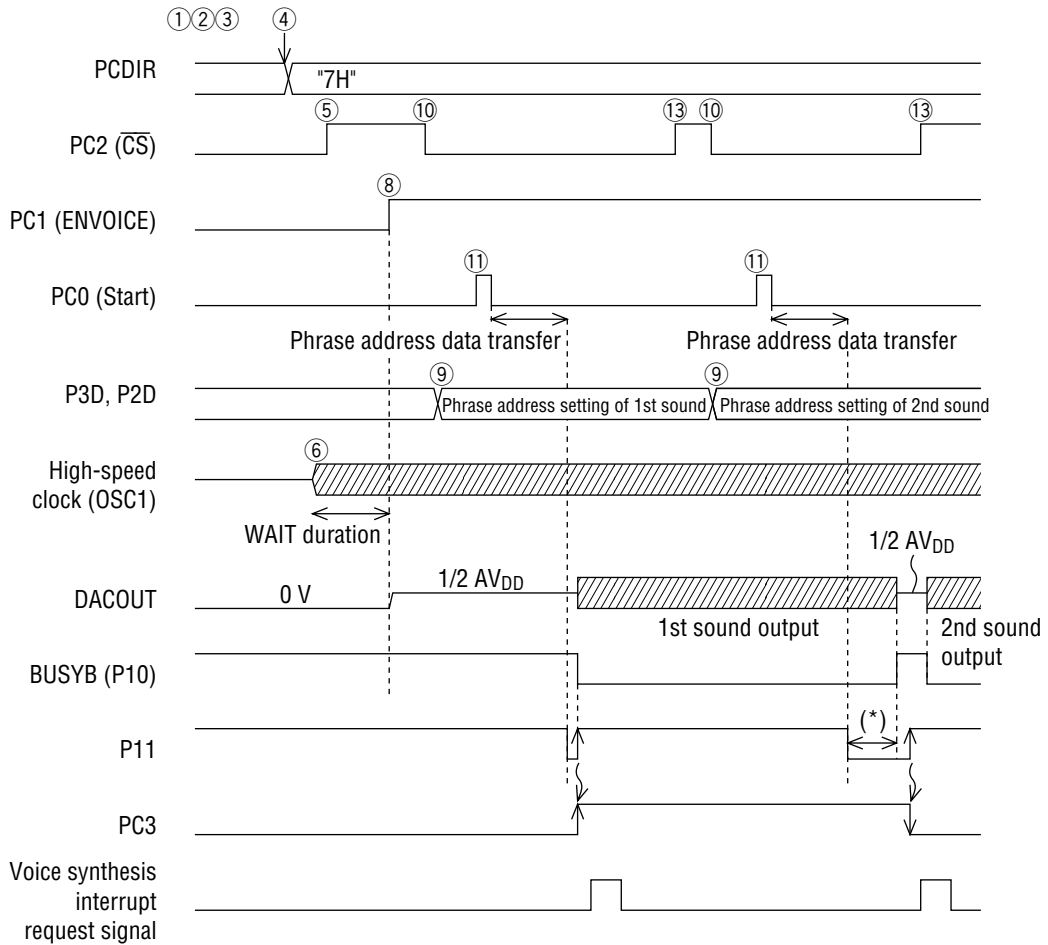
*: P11 maintains the "L" level if the sound output is being made at the time when transfer of the phrase data of the 2nd sound is completed (BUSYB = "L"), and goes to the "H" level after the sound output has been completed.

Figure 13-3 Voice Synthesis Output Timing

13.8 Voice Output Duration

Voice output duration can be obtained by the following expression:

voice output duration　= voice ROM capacity/bit rate

= voice ROM capacity/(sampling frequency $\times$ bit length)

Table 13-4 shows the maximum voice output duration for each sampling frequency and voice ROM capacity.

Table 13-4 Maximum Voice Output Duration

4-bit ADPCM method used [sec.]

Sampling frequency [kHz]	Voice ROM capacity [bits]		
	512K	1M	1.5M
4.0	32.8	65.5	98.3
5.3	24.7	49.5	74.2
6.4	20.5	41.0	61.4
8.0	16.4	32.8	49.2
10.7	12.2	24.5	36.7
12.8	10.2	20.5	30.7
16.0	8.2	16.4	24.6

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13.9 Melody

The melody circuit starts the melody output from the MD/MDB pins or the DACOUT/AOUT pins when the tempo and start address are stored in the phrase address management area and then the phrase in which the melody has been set is started from the interface circuit.

The melody circuit outputs the melody while automatically reading the melody data in the ROM. Melody output stops when the last melody data with the END bit set to "1" is read in.

The generation of the melody is done using the voice analysis tool.

13.9.1 Tempo Data

The tempo data is set in the phrase management area at the time the ROM is manufactured. It is not possible to externally change the tempo. Tempo data defines the reference tone length.

Table 13-5 lists the set tempos (the number of counts per minute).

Table 13-5 Melody Tempos

	TEMPO					Tempo
	TP4	TP3	TP2	TP1	TP0	
0H	0	0	0	0	0	♩ = 625
1H	0	0	0	0	1	♩ = 625
2H	0	0	0	1	0	♩ = 416.7
3H	0	0	0	1	1	♩ = 312.5
4H	0	0	1	0	0	♩ = 250
5H	0	0	1	0	1	♩ = 208.3
6H	0	0	1	1	0	♩ = 178.6
7H	0	0	1	1	1	♩ = 156.7
8H	0	1	0	0	0	♩ = 138.9
9H	0	1	0	0	1	♩ = 125
AH	0	1	0	1	0	♩ = 113.6
BH	0	1	0	1	1	♩ = 104.2
CH	0	1	1	0	0	♩ = 96.2
DH	0	1	1	0	1	♩ = 89.3

Table 13-5 Melody Tempos (continued)

	TEMPO					Tempo
	TP4	TP3	TP2	TP1	TP0	
EH	0	1	1	1	0	♩ = 83.3
FH	0	1	1	1	1	♩ = 78.1
10H	1	0	0	0	0	♩ = 73.5
11H	1	0	0	0	1	♩ = 69.4
12H	1	0	0	1	0	♩ = 65.8
13H	1	0	0	1	1	♩ = 62.5
14H	1	0	1	0	0	♩ = 59.5
15H	1	0	1	0	1	♩ = 56.8
16H	1	0	1	1	0	♩ = 54.3
17H	1	0	1	1	1	♩ = 52.1
18H	1	1	0	0	0	♩ = 50
19H	1	1	0	0	1	♩ = 48.1
1AH	1	1	0	1	0	♩ = 46.3
1BH	1	1	0	1	1	♩ = 44.6
1CH	1	1	1	0	0	♩ = 43.1
1DH	1	1	1	0	1	♩ = 41.7
1EH	1	1	1	1	0	♩ = 40.3
1FH	1	1	1	1	1	♩ = 39.1

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13.9.2 Melody Data

The melody data is the data in the memory that defines the tone, tone length, and the end tone, and consists of two bytes. The melody data format is shown in Figure 13-4.

First byte	END bit	0	L5	L4	L3	L2	L1	L0	Tone length code
Second byte	N7	N6	N5	N4	N3	N2	N1	N0	Tone code

Figure 13-4 Melody Data Format

(1) Tone code

The tone code is set in bits 6 through 0 of the melody data. The frequencies that can be output by the melody circuit are defined as:

$$\frac{65}{(N + 2)} \text{ kHz}\ \ \text{(where N is an integer from 4 to 127)}$$

The relation between N and tone code bits is:

$$N = 2^7N7 + 2^6N6 + 2^5N5 + 2^4N4 + 2^3N3 + 2^2N2 + 2^1N1 + 2^0N0$$

If N7 through N2 are all set to "0", there is no melody output for the time specified by the tone length code. Values for N1 and N0 are irrelevant.

Table 13-6 indicates the relations between tones and tone codes.

Table 13-6 Tone and Tone Code Correspondence

Tone	Frequency (Hz)	Tone code								
		N7	N6	N5	N4	N3	N2	N1	N0	N7–N0
C^1	261.22	1	1	1	1	0	0	1	1	F3H
Cis^1	277.06	1	1	1	0	0	1	0	1	E5H
D^1	293.58	1	1	0	1	1	0	0	0	D8H
Dis^1	310.68	1	1	0	0	1	1	0	0	CCH
E^1	329.90	1	1	0	0	0	0	0	0	C0H
F^1	349.73	1	0	1	1	0	1	0	1	B5H
Fis^1	369.94	1	0	1	0	1	0	1	1	ABH
G^1	392.64	1	0	1	0	0	0	0	1	A1H
Gis^1	415.58	1	0	0	1	1	0	0	0	98H
A^1	441.38	1	0	0	0	1	1	1	1	8FH
Ais^1	467.15	1	0	0	0	0	1	1	1	87H
B^1	492.31	1	0	0	0	0	0	0	0	80H
C^2	524.59	0	1	1	1	1	0	0	0	78H
Cis^2	556.52	0	1	1	1	0	0	0	1	71H
D^2	587.16	0	1	1	0	1	0	1	1	6BH
Dis^2	621.36	0	1	1	0	0	1	0	1	65H
E^2	659.79	0	1	0	1	1	1	1	1	5FH
F^2	695.65	0	1	0	1	1	0	1	0	5AH
Fis^2	744.19	0	1	0	1	0	1	0	0	54H
G^2	780.49	0	1	0	1	0	0	0	0	50H
Gis^2	831.17	0	1	0	0	1	0	1	1	4BH
A^2	876.71	0	1	0	0	0	1	1	1	47H
Ais^2	927.54	0	1	0	0	0	0	1	1	43H
B^2	984.62	0	0	1	1	1	1	1	1	3FH
C^3	1049.18	0	0	1	1	1	0	1	1	3BH
Cis^3	1103.45	0	0	1	1	1	0	0	0	38H
D^3	1185.19	0	0	1	1	0	1	0	0	34H
Dis^3	1254.90	0	0	1	1	0	0	0	1	31H
E^3	1306.12	0	0	1	0	1	1	1	1	2FH
F^3	1391.30	0	0	1	0	1	1	0	0	2CH
Fis^3	1488.37	0	0	1	0	1	0	0	1	29H

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(2) Tone length code

The tone length code is set in the first byte of the melody data.

Table 13-7 indicates the relation between tone length and tone length code (L5 to L0).

When all bits are set to "0", the tone length will be the same as the minimum tone length (the tone length with only L0 set to "1").

Table 13-7 Tone Length and Tone Length Code Correspondence

Tone length	Tone length code						
	L5	L4	L3	L2	L1	L0	L5–L0
♩	1	1	1	1	1	1	3FH
♩.	1	0	1	1	1	1	2FH
♩	0	1	1	1	1	1	1FH
♪.	0	1	0	1	1	1	17H
♪	0	0	1	1	1	1	0FH
♬.	0	0	1	0	1	1	0BH
♬	0	0	0	1	1	1	07H
♬.	0	0	0	1	0	1	05H
♬	0	0	0	0	1	1	03H
♬.	0	0	0	0	1	0	02H
♬	0	0	0	0	0	1	01H

The tone will be a rest when N6 to N0 are all set to "0" in the setting of the tone code. Table 13-8 indicates the relation between the rest and the rest code (L5 to L0).

Table 13-8 Rest and Rest Code Correspondence

Rest	Rest code						
	L5	L4	L3	L2	L1	L0	L5–L0
	1	1	1	1	1	1	3FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	0	1	1	1	07H
	0	0	0	0	1	1	03H

Tone lengths specified by the tone length code and the tempo data are expressed by the following:

$$1.5 \times (TP + 1) \times (L + 1) \text{ ms}$$

(where TP is an integer from 1 to 31, and L is an integer from 1 to 63)

TP is a value set by the tempo data in the phrase management area and has the following bit correspondence:

$$TP = 2^4 TP4 + 2^3 TP3 + 2^2 TP2 + 2^1 TP1 + 2^0 TP0$$

L is set by the tone length code and has a bit correspondence with the tone length code as:

$$L = 2^5 L5 + 2^4 L4 + 2^3 L3 + 2^2 L2 + 2^1 L1 + 2^0 L0$$

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(3) END bit

The END bit is set in bit 15 of the melody data. When the output of the last melody data with the END bit set to "1" is started, the melody circuit generates a melody end signal, and stops the melody after the last melody data is output.

13.9.3 Melody Circuit Application Example

The example of outputting the notes shown in Figure 13-5 is given below.

Figure 13-5 Example Melody

Table 13-9 lists the note codes for the melody shown in Figure 13-5.

Table 13-9 List of Note Codes

Note	Note code																Hex value
	First byte								Second byte								
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
	END	—*	L5	L4	L3	L2	L1	L0	N7	N6	N5	N4	N3	N2	N1	N0	
G^2	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0	0	2F50H
D^2	0	0	0	0	1	1	1	1	0	1	1	0	1	0	1	1	0F6BH
G^2	0	0	0	1	0	1	1	1	0	1	0	1	0	0	0	0	1750H
D^2	0	0	0	0	0	1	1	1	0	1	1	0	1	0	1	1	076BH
G^2	0	0	0	1	0	1	1	1	0	1	0	1	0	0	0	0	1750H
A^2	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	1	1747H
B^2	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	3F3FH
G^2	1	0	1	1	1	1	1	1	0	1	0	1	0	0	0	0	BF50H

*: Bit 6 of the first byte can be either "0" or "1", but is shown here as "0".

13.9.4 Melody Output Procedure

The procedure for outputting a melody is basically the same as the method of voice output described in Section 13.7.3. The distinction between voice and melody is made only by the data set in the phrase address management area and the user data area of the voice ROM.

Follow the procedure below to make the settings:

① Set which pin to use for the output among DACOUT/AOUT and MD/MDB.

- Set PD1DIR and PD0DIR (bit 1 and bit 0 of PDDIR) to "1".

- When outputting at MD/MDB: Set PD1 and PD0 (bit 1 and bit 0 of PDD) to "1".

- When outputting at DACOUT/AOUT: Set PD1 to "1" and PD0 to "0".

② Select voice synthesis/external memory transfer instruction.

- Set P82DIR (bit 2 of P8DIR) to "1".

- Set P82 (bit 2 of P8D) to "0".

③ Select the internal voice ROM or the external memory.

- Set P83DIR (bit 3 of P8DIR) to "1".

- When using the internal voice ROM: Set P83 (bit 3 of P8D) to "0".

- When using the external memory: Set P83 to "1".

The procedure hereafter is the same as steps ④ to ⑮ in Section 13.7.3, "Voice Output Procedure."

Figure 13-6 shows the timing of melody output.

13
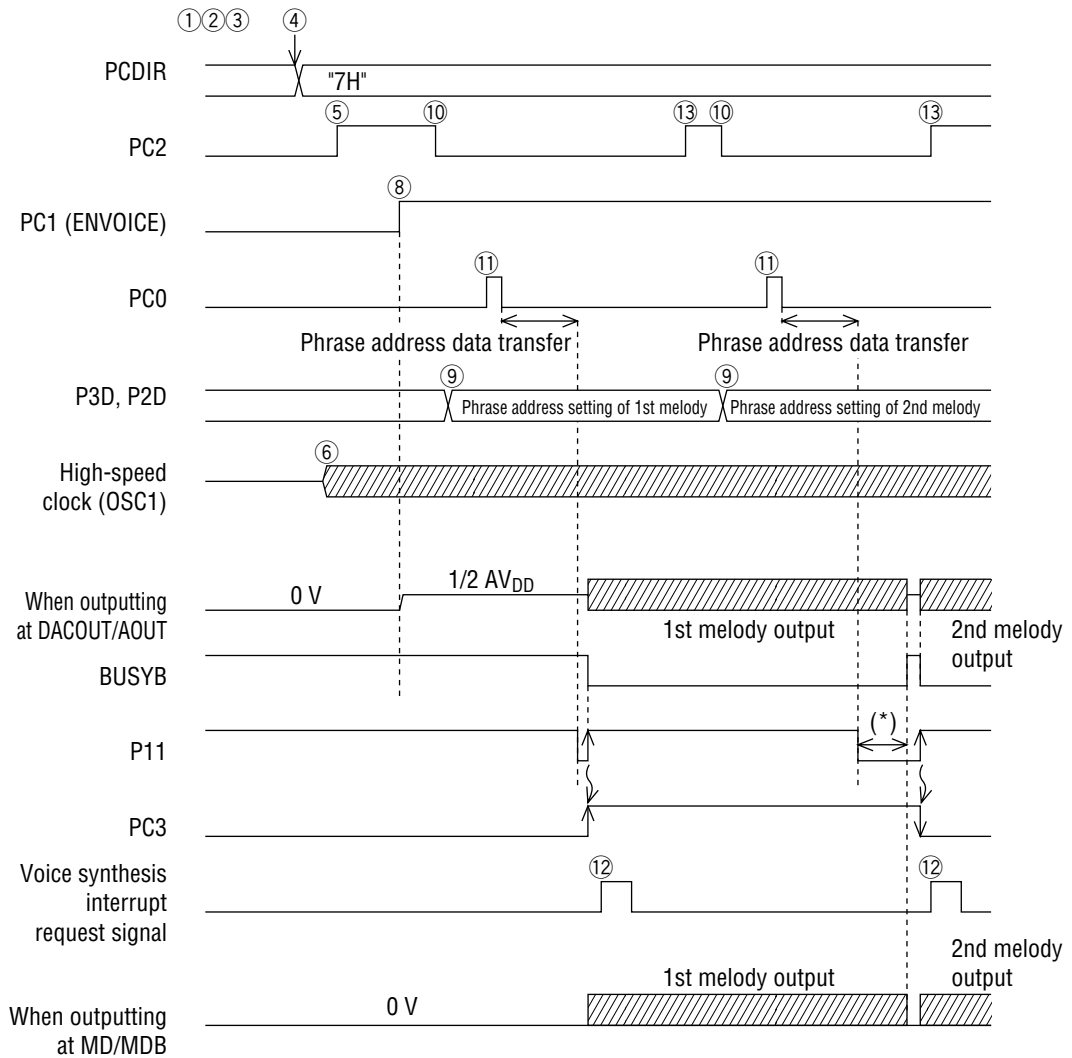
*: P11 maintains the "L" level if the melody output is being made at the time when the phrase data of the 2nd melody is completed (BUSYB = "L"), and goes to the "H" level after the melody output has been completed.

Figure 13-6 Melody Output Timing

13.10 Buzzer

The buzzer output is made at the MD/MDP pins or the DACOUT/AOUT pins when the phrase with the buzzer setting is started from the interface circuit. Buzzer output is available when the frequency and sound type have been set in the phrase address management area.

Inputting the stop code will stop the buzzer output.

Based on the settings made in the phrase management area, the buzzer output frequency can be selected from the 50% duty ratio frequencies of 0.5 kHz, 1.0 kHz, and 2.0 kHz, and the buzzer output mode can be selected from intermittent tone 1, intermittent tone 2, single tone, and continuous tone.

The output waveforms in the different output modes is shown in Figure 13-7. The dark filled parts in the waveform indicate the output frequency signal (0.5, 1.0, or 2.0 kHz).

(a) Intermittent tone 1

(b) Intermittent tone 2

(c) Single tone

(d) Continuous tone
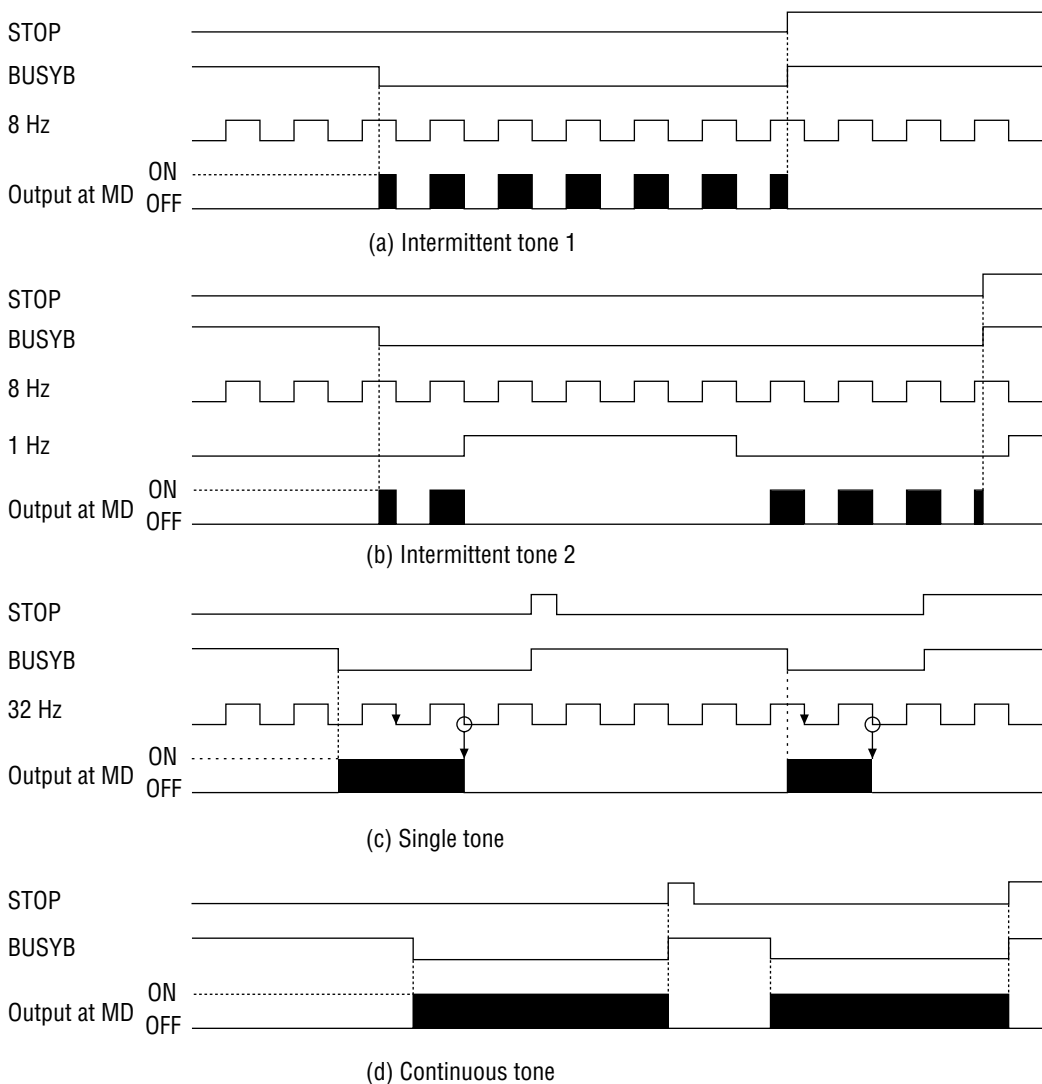
Figure 13-7 Buzzer Driver Output Waveforms in Different Output Modes

13.10.1 Buzzer Output Procedure

Follow the procedure below when making a buzzer output.

① Set which pin to use for the output among DACOUT/AOUT and MD/MDB.

- Set PD1DIR and PD0DIR (bit 1 and bit 0 of PDDIR) to "1".

- When outputting at MD/MDB: Set PD1 and PD0 (bit 1 and bit 0 of PDD) to "1".

- When outputting at DACOUT/AOUT: Set PD1 to "1" and PD0 to "0".

② Select voice synthesis/external memory transfer instruction.

- Set P82DIR (bit 2 of P8DIR) to "1".

- Set P82 (bit 2 of P8D) to "0".

③ Select the internal voice ROM or the external memory.

- Set P83DIR (bit 3 of P8DIR) to "1".

- When using the internal voice ROM: Set P83 (bit 3 of P8D) to "0".

- When using the external memory: Set P83 to "1".

④ Make the setting of PCDIR.

- Set PC2DIR, PC1DIR, and PC0DIR all to "1".

⑤ Set PC2 (bit 2 of PCD) to "1" ($\overline{\text{CS}}$ of the voice synthesis section is disabled).

⑥ Enable high-speed oscillation.

- For the crystal oscillation mode: Set bit 2 and bit 1 of FCON (062H) to "1".

- For the RC oscillation mode: Set bit 1 of FCON (062H) to "1".

Note: Wait for 10 ms for crystal oscillation and 5 ms for RC oscillation so that the high-speed oscillation waveform becomes stable.

⑦ The contents of the program differ depending on the timing of inputting the stop code, etc. When carrying out control using interrupts, make the necessary settings.

⑧ Set PC1 (bit 1 of PCD) to "1" (releasing the reset state of the voice synthesis section).

⑨ Set the phrase address in P3D and P2D. (P33 is the MSB and P20 is the LSB.)

⑩ Set PC2 (bit 2 of PCD) to "0" ($\overline{\text{CS}}$ of the voice synthesis section is enabled).

⑪ First set PC0 (bit 0 of PCD) to "1" and then set it to "0" (start of transfer).

The serial transfer of the phrase address is started.

⑫ The buzzer sound is output.

⑬ The buzzer output is terminated when the stop code is input.

13.11 Example of Connections Made for Extending the Voice Data Area

The ML63326 has an internal 128-Kbyte ROM as the voice synthesis data area.

In addition, the voice synthesis data area can be extended up to a maximum of 640 Kbytes by connecting a 512-Kbyte ROM externally. An example of connections to be made for this expansion is shown in Figure 13-8.
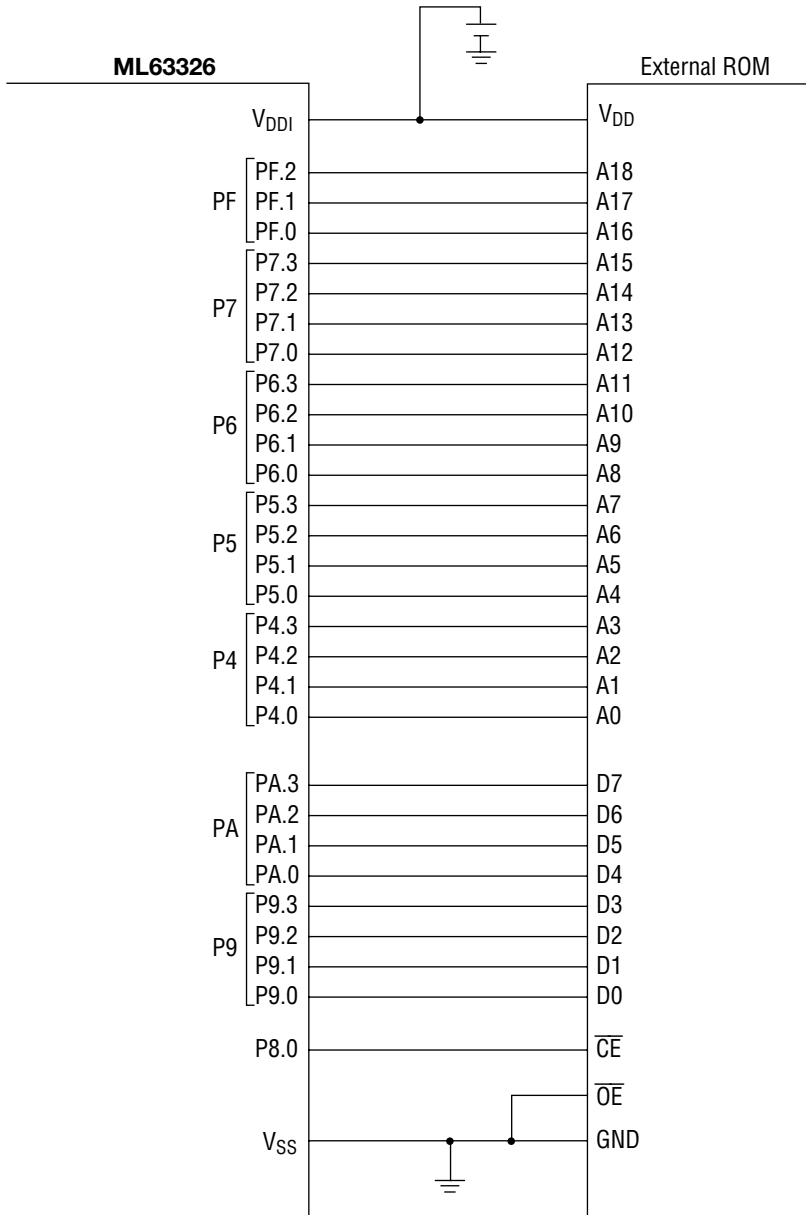
Figure 13-8 Example of Connections Made When an External ROM is Used

13.12 Example of Connections Made When Using a Piezoelectric Speaker

The ML63326 has two built-in amplifiers that can directly drive a piezoelectric speaker. When using this amplifier, it is possible to output the voice and other sounds from a piezoelectric speaker by externally connecting one capacitor and two resistors. An example of connections to be made for using a piezoelectric speaker is shown in Figure 13-9.

The AOUT output amplitude can be varied by changing the ratio R_1:R_2 of the external resistors. In the example below, since R_1 is 50 kΩ and R_2 is 100 kΩ, the amplitude of the AOUT output is increased twofold and is output to the SP(–) and SP(+) pins. When selecting R_1 and R_2, make sure that the sum of R_1 and R_2 is 100 kΩ or more.

By connecting the SPEN pin with the ENVOICE pin as shown below, the amplifiers will also become enabled only when the voice synthesis section is enabled.
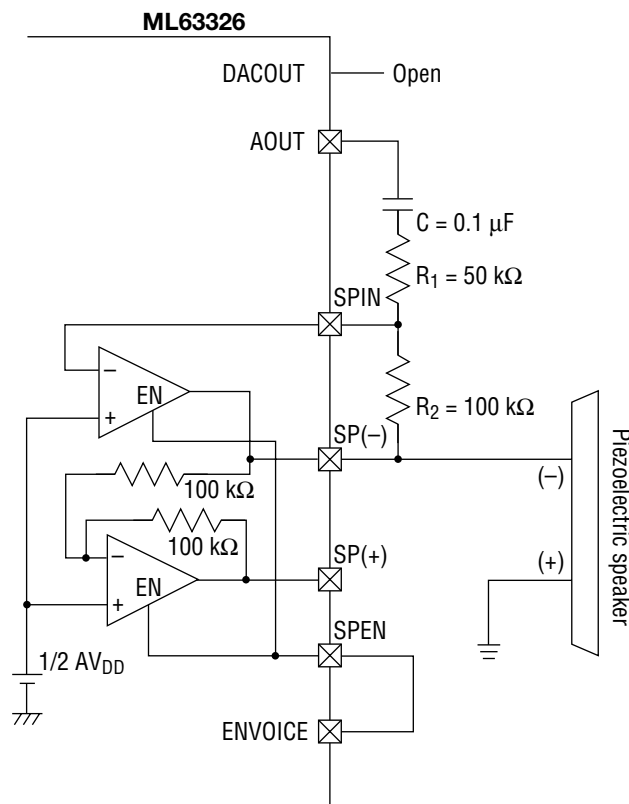
Figure 13-9 Example of Connections Made When Using a Piezoelectric Speaker

⚠️ Note:

- When selecting R_1 and R_2 (external resistors), make sure that their resistance values are
  : $(R_1) + (R_2) \geq 100$ kΩ

- For the (–) and (+) terminals of the piezoelectric speaker, connect either terminal to the SP(–) or SP(+) pin and tie the other to V_{SS}.

Shift Register (SFT)

Chapter 14 Shift Register (SFT)

14.1 Overview

The ML63326 has one internal 8-bit shift register channel for clock synchronous communication.

The shift register is synchronized with the clock specified by the shift register control register 0 (SFTCON0), and can perform 8-bit data send and receive simultaneously. When 8-bit data transfer is completed, a shift register interrupt request is generated.

14.2 Shift Register Configuration

The shift register configuration is shown in Figure 14-1.

PE.0/SIN, PE1/SOUT and PE.2/SCLK are the shift data input pin, the shift data output pin and the shift clock input /output pin respectively. Set the secondary function by using port mode register.
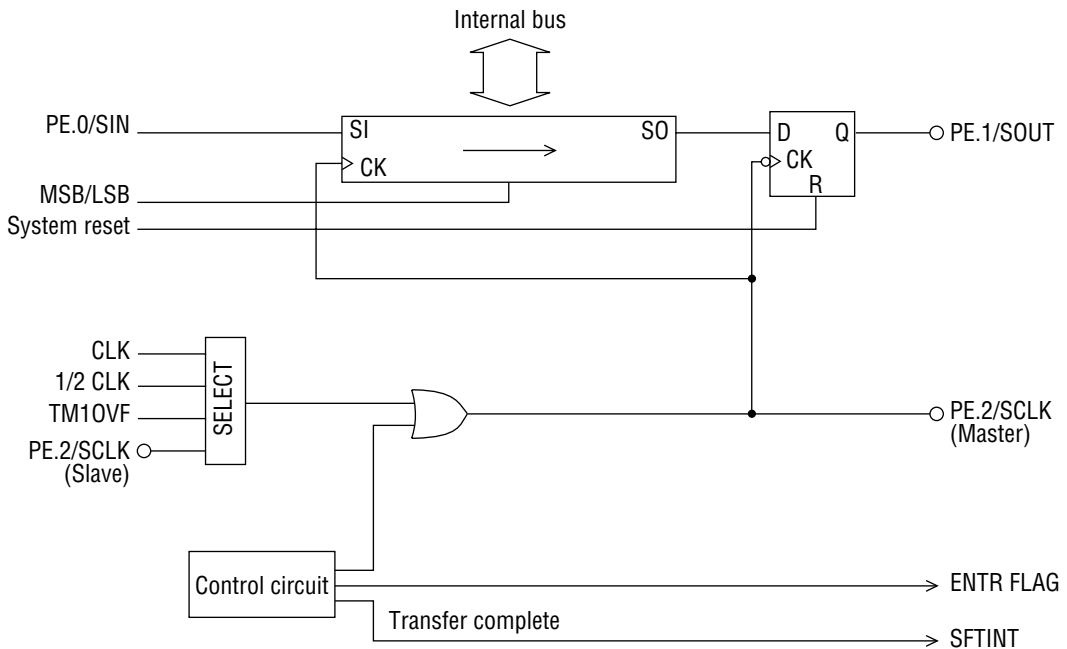
Figure 14-1 Shift Register Configuration

14.3 Shift Registers

(1) Shift register L/H (SFTRL, SFTRH)

SFTRL and SFTRH are 4-bit special function registers (SFRs) used to write shift register send data and to read receive data.

	bit 3	bit 2	bit 1	bit 0
SFTRL (0A0H) (R/W)	SD3	SD2	SD1	SD0
	bit 3	bit 2	bit 1	bit 0
SFTRH (0A1H) (R/W)	SD7	SD6	SD5	SD4

SFTRL and SFTRH are set to "0" at system reset.

(2) Shift register control registers (SFTCON0, SFTCON1)

SFTCON0 and SFTCON1 are 4-bit special function registers (SFRs) that control shift register operation. At system reset both are initialized to "0".

	bit 3	bit 2	bit 1	bit 0
SFTCON0 (0A2H) (R/W)	—	SDIR	SELCK1	SELCK0

LSB/MSB first select
 1 : MSB first (initial value)
 0 : LSB first

Shift clock select
 bit 1 bit 0
   0   0 : CLK (initial value)
   0   1 : 1/2 CLK
   1   0 : Timer 1 overflow
   1   1 : External clock
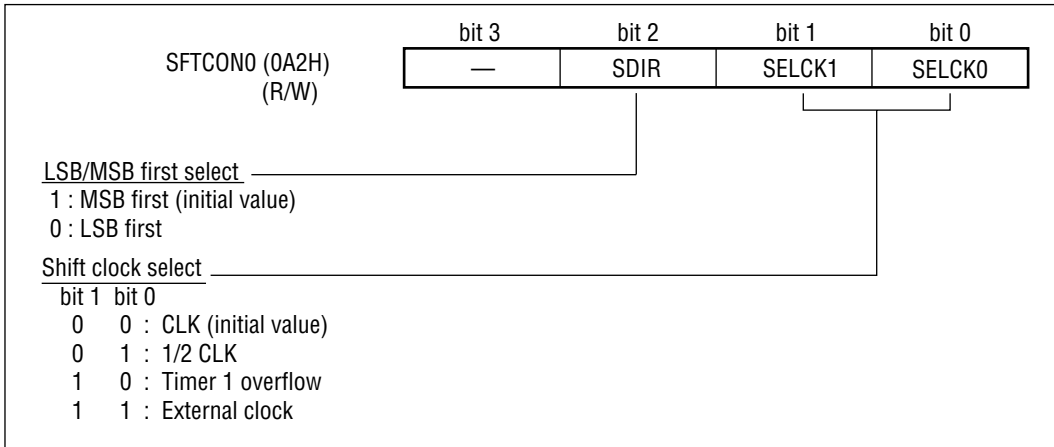
bit 2: SDIR

   This bit selects the transfer order for 8-bit send/receive data.

   When the SDIR bit is "0" it means MSB first, and when "1", LSB first.

bit 1, 0: SELCK1, SELCK0

   These bits select the shift clock.

   If set to CLK, 1/2 CLK or timer 1 overflow the system operates in master mode. If set to external clock the system operates in slave mode.

	bit 3	bit 2	bit 1	bit 0
SFTCON1 (0A3H) (R/W)	—	—	—	ENTR

Transfer start flag
 0 : Transfer end (initial value)
 1 : Transfer start
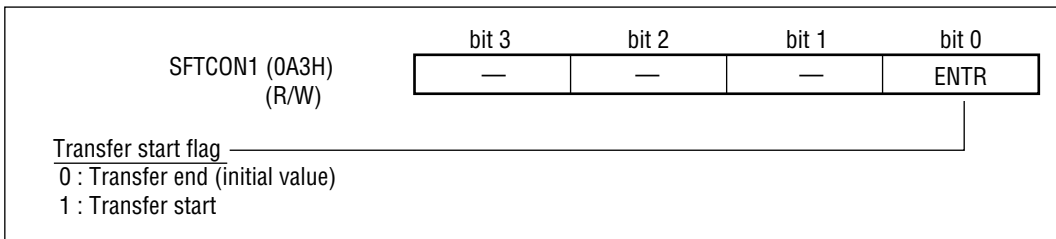
bit 0: ENTR

   When ENTR is set to "1", transfer starts, and when 8-bit transfer ends, it is automatically set to "0".

14.4 Shift Register Operation

The shift register can be set to master or slave mode, and to MSB first or LSB first. The send data is written to the shift register (SFTRL, SFTRH), and transfer is started by setting bit 0 (ENTR) of the shift control register 1 (SFTCON1) to "1". After 8-bit data transfer (send/receive), operation ends.

Bits 1, 0 (SELCK1, SELCK0) of the shift control register 0 (SFTCON0) can set the shift clock to CLK, 1/2 CLK or timer 1 overflow. This operation is master mode and the shift clock is output to the PE.2/SCLK pin.

When the shift clock is set to external clock, the system operates in slave mode, and operation is to the clock input through the PE.2/SCLK pin. If eight or more clocks are input consecutively, the ninth and following clocks are ignored.

In both master and slave modes, the shift register is synchronized to the shift clock falling edge, and shift-out data is output from the first bit through the PE.1/SOUT pin. In synchronization with the shift clock rising edge, shift-in data is input from the first bit through the PE.0/SIN pin.

For external devices, shift-in data changes on the falling edge of the shift clock, and shift-out data changes on the rising edge of the shift clock.

When 8-bit data transfer is complete, bit 0 (ENTR) of SFTCON1 is cleared to "0". When transfer is completed, the interrupt request signal (SFTINT) is generated (see Figure 14-2).

The output pin state at system reset and between transfers (from the end of one 8-bit transfer until the next transfer starts) is shown in Table 14-1 (when set to the output secondary function).

Table 14-1 Output Pin States

Pin name	At system reset	Between transfers
PE.2/SCLK	"H"	"H"
PE.1/SOUT	"L"	Last transfer data of transfer

MSB/LSB first is set to bit 2 (SDIR) of SFTCON0.

• SDIR = 0 : MSB first mode

Input ⟶ | SD0 | SD1 | SD2 | SD3 | SD4 | SD5 | SD6 | SD7 | ⟶ Output

SFTRL ——— SFTRH

• SDIR = 1 : LSB first mode

Input ⟶ | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | ⟶ Output

SFTRH ——— SFTRL
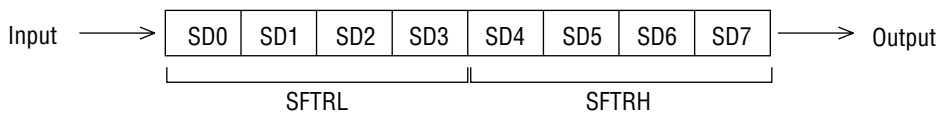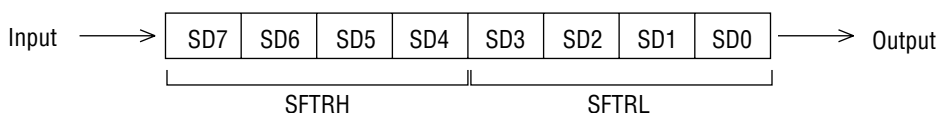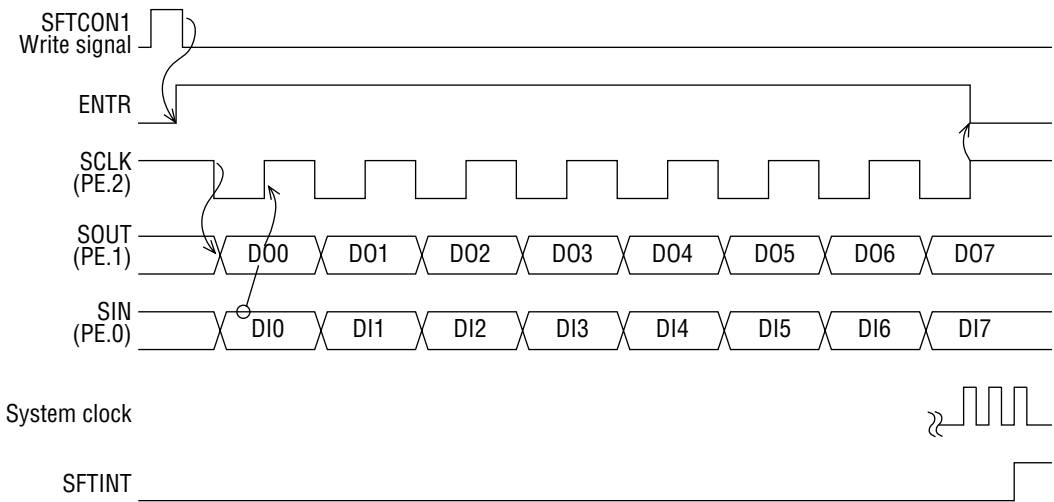
Figure 14-2 Shift Register Operation Timing

⚠ Note :

Setting the ENTR bit to "1" in the slave mode should be done when the PE.2/SCLK pin is high.

If SFTRL/SFTRH are written during transfer, the transfer data (send and receive) is destroyed. In this case, terminate the transfer and start over again.

Even when receiving only, transfer begins with setting the ENTR bit to "1".

14.5 Shift Register Application Example

An example of register setting for clock synchronous communication using shift register is described below.

(1) Set the supported port modes (secondary function).

Port control register	Master mode	
PEMOD	Bit 2 = "1"	(PE.2/SCLK)
	Bit 1 = "1"	(PE.1/SOUT)
	Bit 0 = "1"	(PE.0/SIN)

(2) Select the shift clock with SELCK1, SELCK0 (SFTCON0 bits 1, 0)(master/slave mode select).

(3) Select MSB first or LSB first with SDIR (SFTCON0 bit 2). ("0" for MSB first, "1" for LSB first).

(4) Set ESFT (IE3 bit 2) to "1" and enable the shift register interrupt.

(5) Set the MIE (master interrupt enable flag) to "1", and enable all interrupts.

(6) Write send data to SFTRL and SFTRH.

(7) Set ENTR (bit 0 of SFTCON1) to "1", and start the transfer.

With the above settings the shift register begins to operate, and the CPU receives the shift register interrupt. Whether 8-bit transfer has been completed can be checked by monitoring QSFT (bit 2 of IRQ3) or ENTR (bit 0 of SFTCON1).

LCD Driver (LCD)

Chapter 15 LCD Driver (LCD)

15.1 Overview

The ML63326 has an internal dot matrix LCD driver. The ML63326 has 64 segment outputs and can drive up to 1024 (64 seg. $\times$ 16 com.) dots.   The LCD driver can be software-selected to all OFF, all ON or power down mode, 1/4 or 1/5 bias, selectable duty from 1/1 to 1/16, and adjustable (16-tone) contrast.

15.2 LCD Driver Configuration

The LCD driver configuration is shown in Figure 15-1.
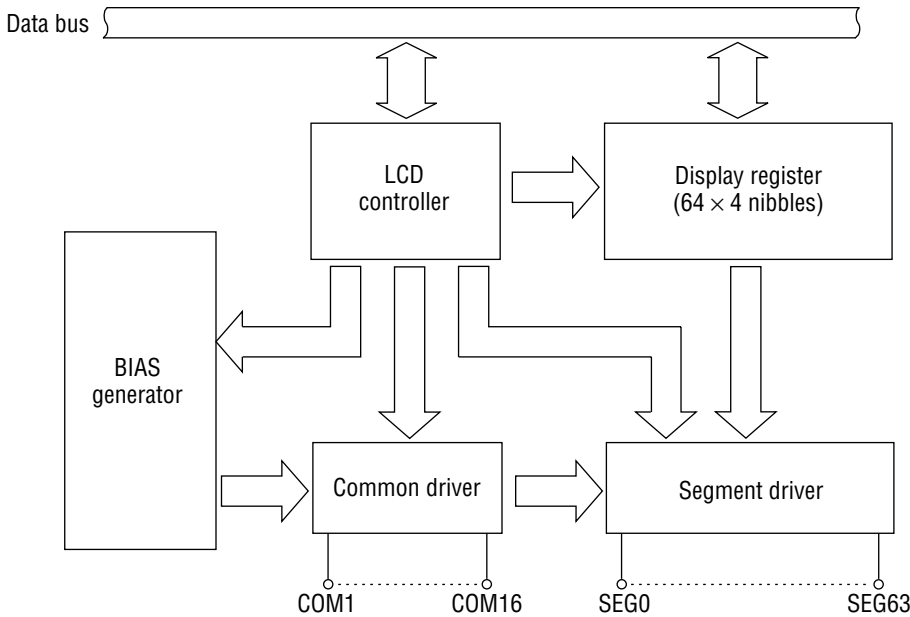
Figure 15-1 LCD Driver Configuration

15.3 LCD Driver Registers

(1) Display control register (DSPCON0)

DSPCON0 is a 4-bit special function register (SFR) controlling LCD driver operation.

	bit 3	bit 2	bit 1	bit 0
DSPCON0 (090H) (R/W)	BISEL	PDWN	ALLON	LCDON

LCD bias select
 0 : 1/5 bias (initial value)
 1 : 1/4 bias

LCD power down mode
 0 : Normal operation mode (initial value)
 1 : Power down mode

All-ON mode
 0 : Normal operation mode (initial value)
 1 : All-ON mode

LCD display select
 0 : All OFF (initial value)
 1 : Normal operation mode
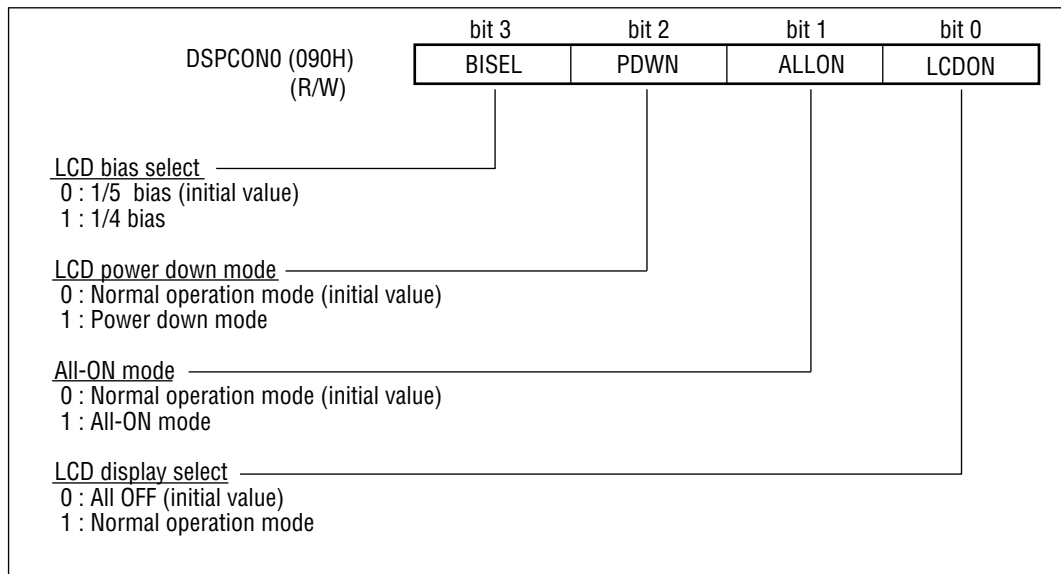
bit 3: BISEL
This bit selects 1/4 or 1/5 bias.
At system reset it is "0", selecting 1/5 bias.

bit 2: PDWN
This bit selects the LCD power down mode. When PDWN is set to "1", the bias generation circuit stops its voltage lowering/raising operation and pins COM1–16 and SEG0–63 are all set to the V_{SS} level, reducing supply current. At system reset it is cleared to "0".

bit 1: ALLON
When ALLON is set to "1" all segment drivers are turned on. The ALLON bit has priority over the LCDON bit. At system reset it is cleared to "0".

bit 0: LCDON
When the LCDON bit is set to "1", the display data in the display register is output to the segment drivers. At system reset it is cleared to "0", and all segment drivers are turned off.

(2) Display control register (DSPCON1)

DSPCON1 is a 4-bit special function register (SFR) used to select the LCD driver duty.

At system reset, bits of DSPCON1 are initialized to "0".

	bit 3	bit 2	bit 1	bit 0
DSPCON1 (091H) (R/W)	DT3	DT2	DT1	DT0

Duty select
bit 3 bit 2 bit 1 bit 0
```
0   0   0   0 : 1/16 duty (initial value)
0   0   0   1 : 1/1 duty
0   0   1   0 : 1/2 duty
0   0   1   1 : 1/3 duty
0   1   0   0 : 1/4 duty
0   1   0   1 : 1/5 duty
0   1   1   0 : 1/6 duty
0   1   1   1 : 1/7 duty
1   0   0   0 : 1/8 duty
1   0   0   1 : 1/9 duty
1   0   1   0 : 1/10 duty
1   0   1   1 : 1/11 duty
1   1   0   0 : 1/12 duty
1   1   0   1 : 1/13 duty
1   1   1   0 : 1/14 duty
1   1   1   1 : 1/15 duty
```
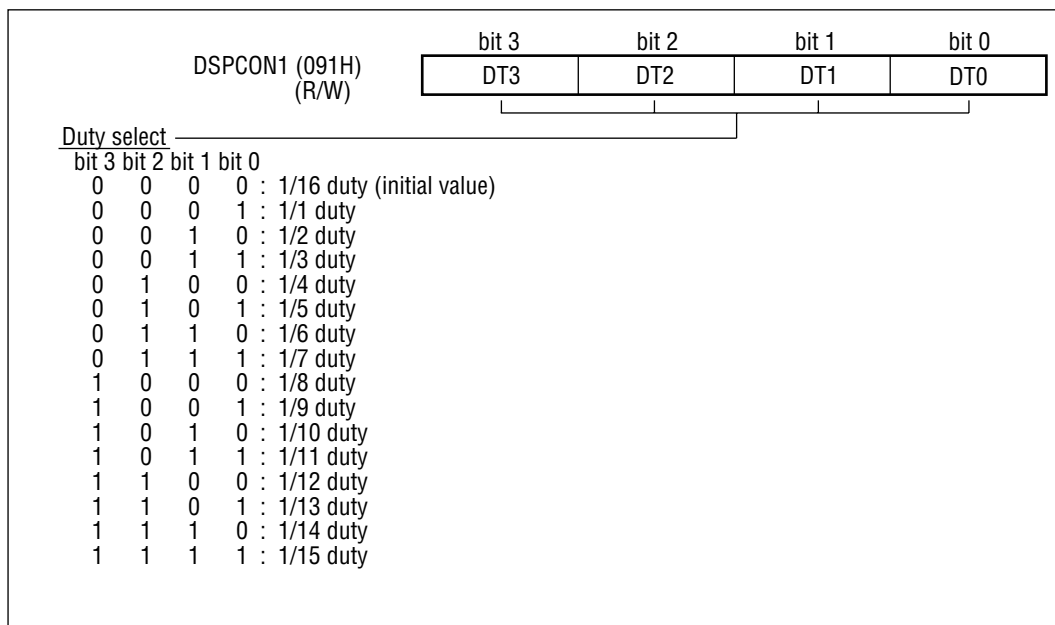
(3) Display contrast register (DSPCNT)

DSPCNT is a 4-bit special function register (SFR) used to adjust display contrast.

At system reset, bits of DSPCON1 are initialized to "0".

	bit 3	bit 2	bit 1	bit 0
DSPCNT (092H) (R/W)	CN3	CN2	CN1	CN0

Contrast select
bit 3 bit 2 bit 1 bit 0
```
0   0   0   0 : Light (initial value)
0   0   0   1 :
0   0   1   0 :
0   0   1   1 :
0   1   0   0 :
0   1   0   1 :
0   1   1   0 :
0   1   1   1 :
1   0   0   0 :
1   0   0   1 :
1   0   1   0 :
1   0   1   1 :
1   1   0   0 :
1   1   0   1 :
1   1   1   0 :
1   1   1   1 : Dark
```

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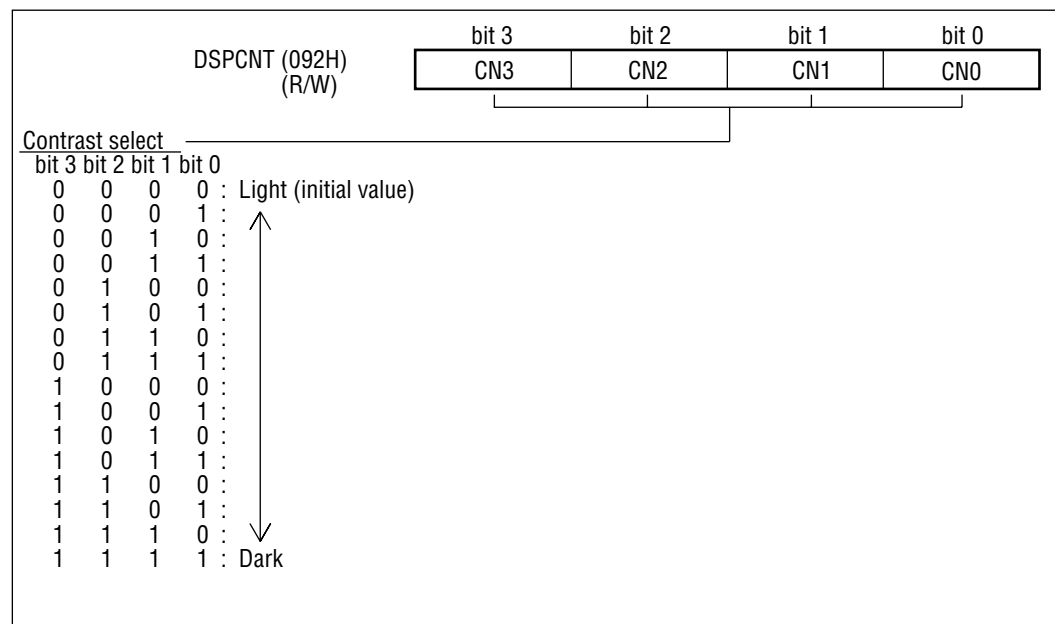
(4) Display registers (DSPR0 to DSPR255)

DSPR0 to DSPR255 are segment output data registers for the dot matrix LCD driver allocated to RAM BANK 1. The correspondence between display registers and segment outputs is shown below.

	bit 3	bit 2	bit 1	bit 0	
DSPR0 (100H) (R/W)	COM4	COM3	COM2	COM1	
DSPR1 (101H) (R/W)	COM8	COM7	COM6	COM5	Segment 0 output data
DSPR2 (102H) (R/W)	COM12	COM11	COM10	COM9	
DSPR3 (103H) (R/W)	COM16	COM15	COM14	COM13	
DSPR4 (104H) (R/W)	COM4	COM3	COM2	COM1	
DSPR5 (105H) (R/W)	COM8	COM7	COM6	COM5	Segment 1 output data
DSPR6 (106H) (R/W)	COM12	COM11	COM10	COM9	
DSPR7 (107H) (R/W)	COM16	COM15	COM14	COM13	
DSPR252 (1FCH) (R/W)	COM4	COM3	COM2	COM1	
DSPR253 (1FDH) (R/W)	COM8	COM7	COM6	COM5	Segment 63 output data
DSPR254 (1FEH) (R/W)	COM12	COM11	COM10	COM9	
DSPR255 (1FFH) (R/W)	COM16	COM15	COM14	COM13	

⚠ Notes:

• When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.

• To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.

• At system reset the display registers (DSPR0 to DSPR255) are undefined and should be initialized.

15.4 LCD Driver Operation

The display duty is selected from 1/1 to 1/16 using DSPCON. The frame frequency for each duty ratio is indicated in Table 15-1. Depending on the duty selected, the common signal (COM1 to COM16) is generated, and data written in synchronization with that common signal to the display registers (DSPR0 to DSPR255) is output to the segment driver. The segment driver uses bits 0, 1 (ALLON, LCDON) of the display control register 0 (DSPCON0) to control all OFF or all ON mode.

When PDWN (bit 2 of DSPCON0) is set to "1", the LCD power down mode is enabled. In the LCD power-down mode the bias generation circuit operation stops, and COM1–16 and SEG0–63 pins are all output at the V_{SS} level to reduce supply current.

BISEL (bit3 of DSPCON0) selects 1/4 or 1/5 bias.

DSPCNT controls the LCD contrast of 16 tones (V_{DDH} = 2.4 V or more).

When the LCD driver is not used, select the power-down mode and set all the bits of the display control register (DSPCNT) to "0" to save the supply current.

Table 15-1 Frame Frequency for Each Duty

DSPCON1					Duty	Frame frequency
DT3–0	DT3	DT2	DT1	DT0		
0H	0	0	0	0	1/16	64 Hz
1H	0	0	0	1	1/1	1024 Hz
2H	0	0	1	0	1/2	512 Hz
3H	0	0	1	1	1/3	approx. 341 Hz
4H	0	1	0	0	1/4	256 Hz
5H	0	1	0	1	1/5	approx. 205 Hz
6H	0	1	1	0	1/6	approx. 171 Hz
7H	0	1	1	1	1/7	approx. 146 Hz
8H	1	0	0	0	1/8	128 Hz
9H	1	0	0	1	1/9	approx. 114 Hz
0AH	1	0	1	0	1/10	approx. 102 Hz
0BH	1	0	1	1	1/11	approx. 93 Hz
0CH	1	1	0	0	1/12	approx. 85 Hz
0DH	1	1	0	1	1/13	approx. 79 Hz
0EH	1	1	1	0	1/14	approx. 73 Hz
0FH	1	1	1	1	1/15	approx. 68 Hz

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15.5 Bias Generator (BIAS)

The bias generator is used to multiply and divide the voltage (V_{DD2}) generated in the constant voltage circuit with an external capacitor connected to pins C1, C2 to generate V_{DD1} to V_{DD5} bias voltages for the LCD driver.

The LCD power down mode stops the voltage lowering/raising operation of the bias generation circuit in order to reduce supply current.

Figure 15-2 shows the bias generator configuration for 1/5 bias, and Figure 15-3 shows the configuration for 1/4 bias.

For details of the voltage doubler circuit and the constant-voltage circuit, see Chapter 17, "Power Supply Circuit."

Tables 15-2 and 15-3 list the display contrast adjusting voltages.

Figure 15-2 Bias Generator Configuration for 1/5 Bias

Figure 15-3 Bias Generator Configuration for 1/4 Bias

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Table 15-2 Display Contrast Adjusting Voltages (V_{DD2})

(Ta = 25°C, V_{SS} = 0 V)

DSPCNT					V_{DD2} Voltage (V)			Contrast
CN3–0	**CN3**	**CN2**	**CN1**	**CN0**	**Min.**	**Typ.**	**Max.**	
0H	0	0	0	0	1.70	1.80	1.90	Light
1H	0	0	0	1	1.74	1.84	1.94	
2H	0	0	1	0	1.78	1.88	1.98	
3H	0	0	1	1	1.82	1.92	2.02	
4H	0	1	0	0	1.86	1.96	2.06	
5H	0	1	0	1	1.90	2.00	2.10	
6H	0	1	1	0	1.94	2.04	2.14	
7H	0	1	1	1	1.98	2.08	2.18	
8H	1	0	0	0	2.02	2.12	2.22	
9H	1	0	0	1	2.06	2.16	2.26	
0AH	1	0	1	0	2.10	2.20	2.30	
0BH	1	0	1	1	2.14	2.24	2.34	
0CH	1	1	0	0	2.18	2.28	2.38	
0DH	1	1	0	1	2.22	2.32	2.42	
0EH	1	1	1	0	2.26	2.36	2.46	
0FH	1	1	1	1	2.30	2.40	2.50	Dark

Table 15-3 Display Contrast Adjusting Voltages (V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5})

(V_{SS} = 0 V)

BISEL	Mode	Power supply	Voltage (V)		
			Min.	**Typ.**	**Max.**
0	1/5 bias	V_{DD1}	Typ. – 0.1	$1/2 \times V_{DD2}$*	Typ. + 0.1
		V_{DD3}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD4}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.4
		V_{DD5}	Typ. – 0.5	$5/2 \times V_{DD2}$*	Typ. + 0.5
1	1/4 bias	V_{DD1}	Typ. – 0.1	$1/2 \times V_{DD2}$*	Typ. + 0.1
		V_{DD3}	Typ. – 0.2	V_{DD2}*	Typ. + 0.2
		V_{DD4}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD5}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.4

V_{DD2}*: Typical V_{DD2} in Table 15-2

15.6 LCD Driver Output Waveform

Figures 15-4 (a) and 15-4 (b) show the output waveforms for 1/16 duty and 1/5 bias, and Figures 15-5 (a) and 15-5 (b) show the output waveforms for 1/8 duty and 1/4 bias.
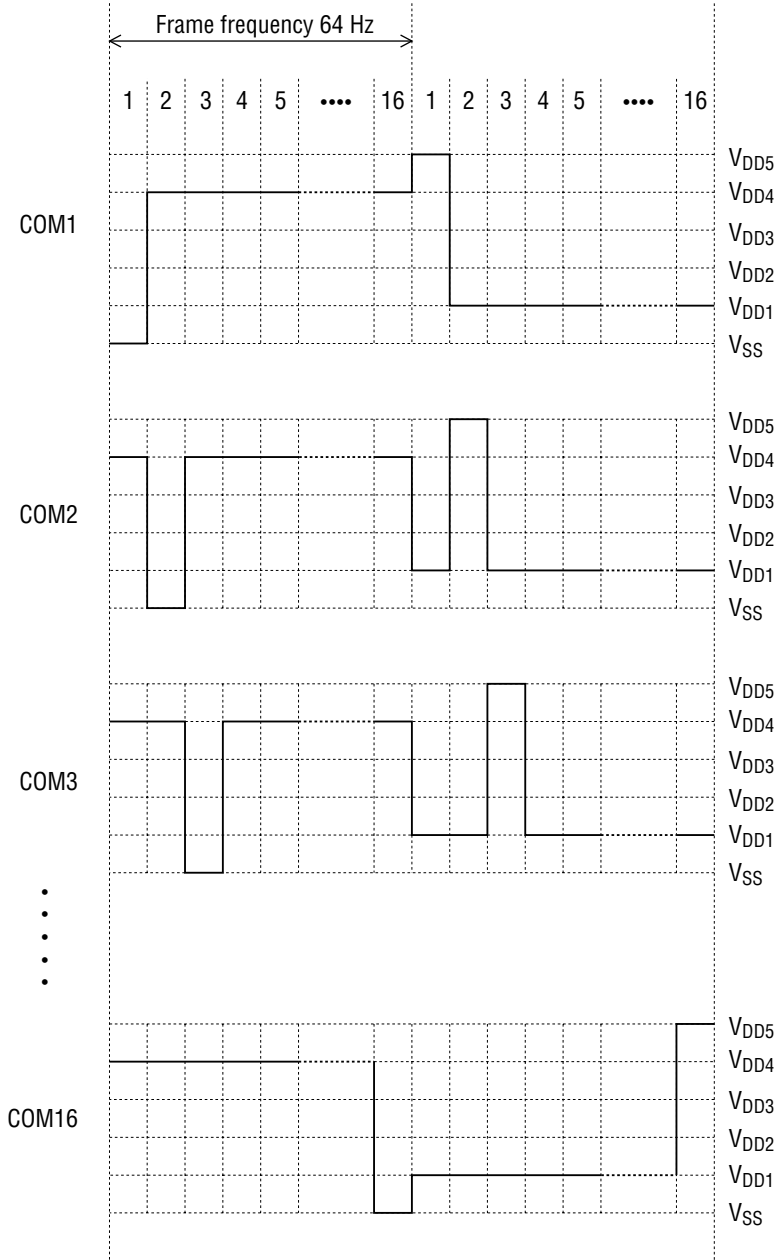
Figure 15-4 (a) 1/16 Duty, 1/5 Bias Common Output Waveform

Figure 15-4 (b) 1/16 Duty, 1/5 Bias Segment Output Waveform
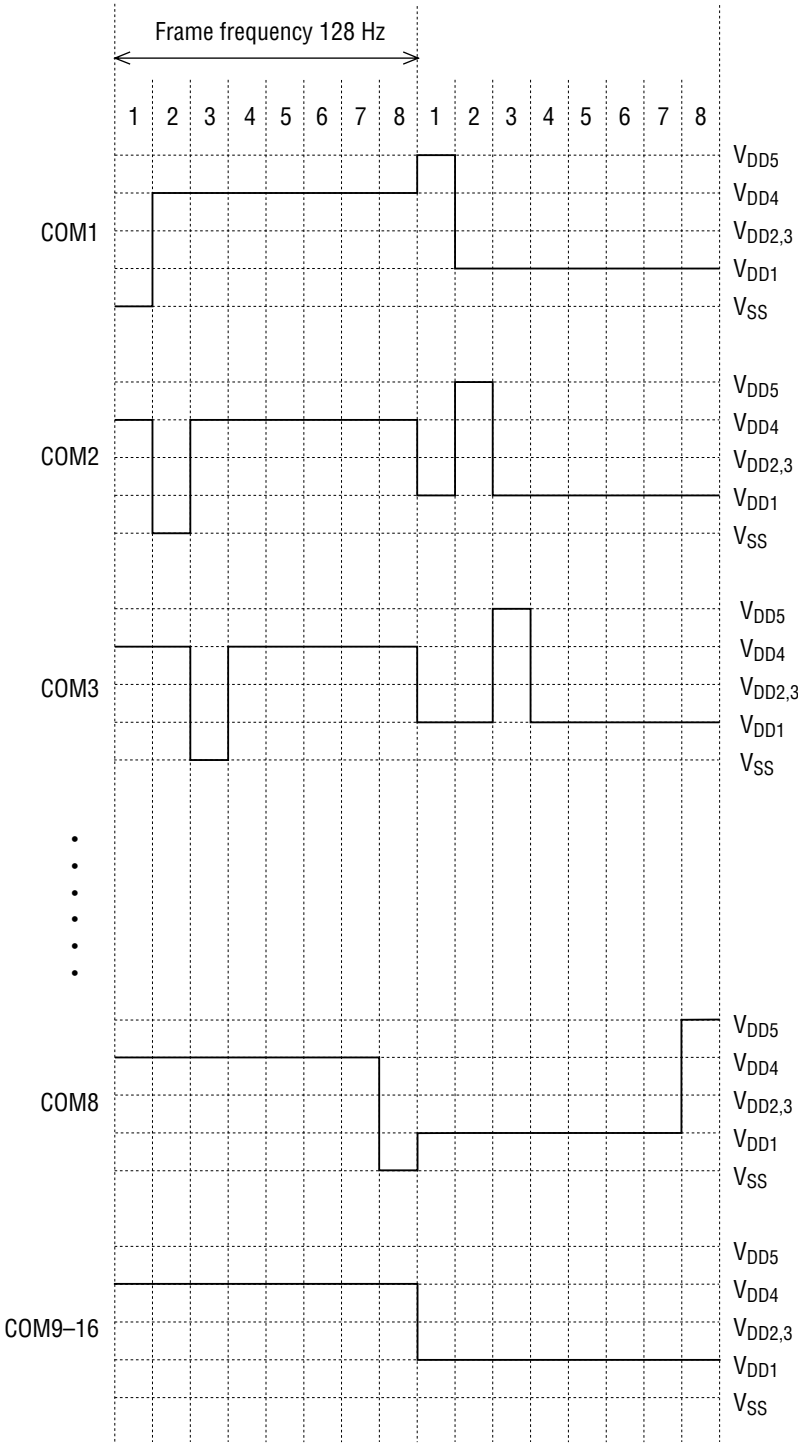
Figure 15-5 (a) 1/8 Duty, 1/4 Bias Common Output Waveform
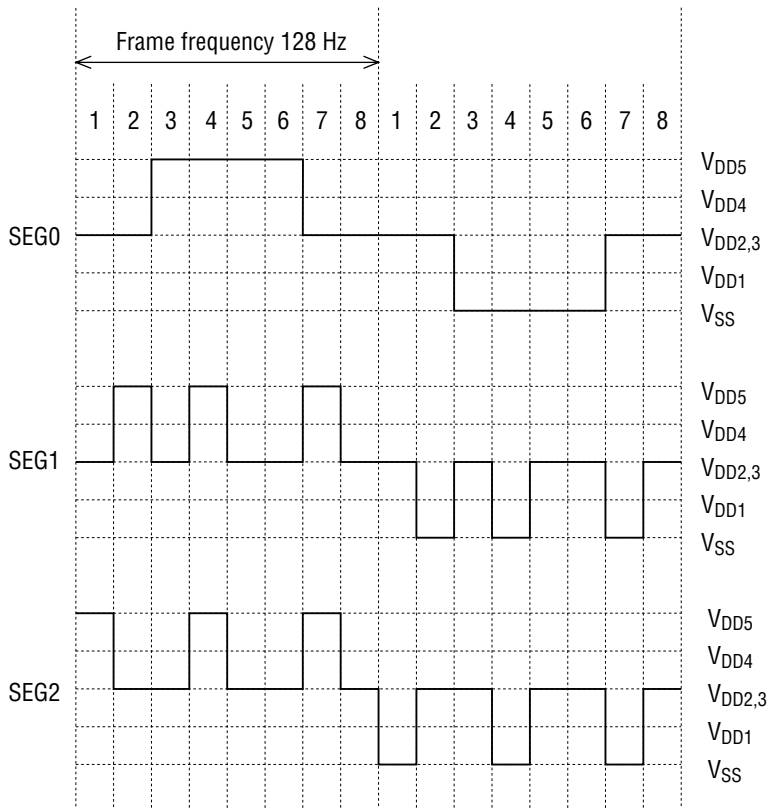
Figure 15-5 (b) 1/8 Duty, 1/4 Bias Segment Output Waveform

Battery Low Detect Circuit (BLD)

Chapter 16 Battery Low Detect Circuit (BLD)

16.1 Overview

The ML63326 contains a battery low detect circuit (BLD).

The battery low detect circuit detects when the battery voltage (supply voltage V_{DD}) falls below the judgment voltage value. Three levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values (Ta = 25°C): 2.00 ±0.10 V, 2.20 ±0.10 V, 2.40 ±0.10 V

⚠ Note:

- When verifying BLD operation, the operation must be verified with an evaluation sample device.

  The development support tool (EASE63180) does not support BLD.

16.2 Battery Low Detect Circuit Configuration

The battery low detect circuit consists of a judgment circuit and a judgment voltage select circuit. Figure 16-1 shows the circuit configuration.
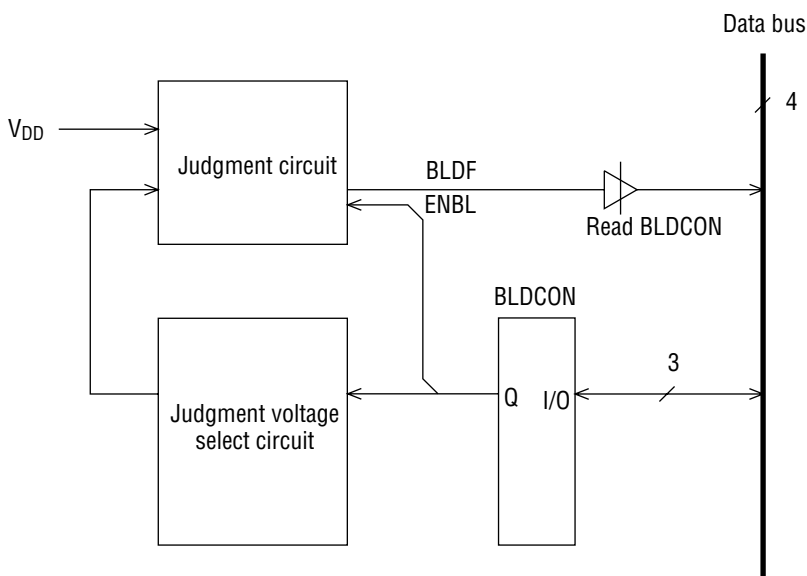
Figure 16-1 Battery Low Detect Circuit

16.3 Judgment Voltage

The value of the judgment voltage is selected by the software by setting the LD1 (bit 1 of BLDCON) and LD0 (bit 0 of BLDCON) bits.

Table 16-1 lists judgment voltage and precision values.

Table 16-1 Judgment Voltage

LD1	LD0	Judgment voltage (V)	Precision (V)	Remarks
0	0	—	—	Undefined
0	1	2.00	±0.10	Ta = 25°C
1	0	2.20	±0.10	Ta = 25°C
1	1	2.40	±0.10	Ta = 25°C

16.4 Battery Low Detect Circuit Register

- Battery low detect control register (BLDCON)
  BLDCON is a 4-bit special function register (SFR) that controls the battery low detect circuit.
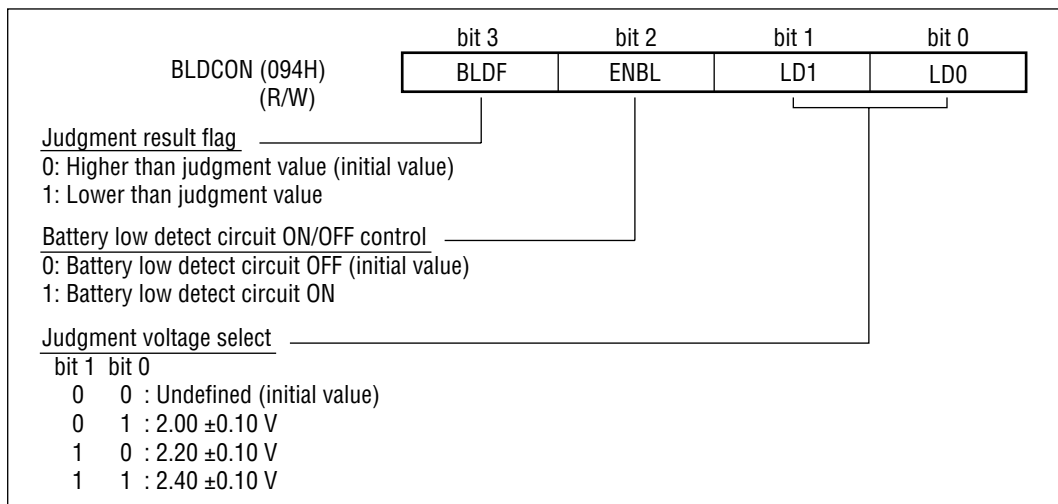
bit 3: BLDF
> This flag indicates the judgement result of the battery low detect circuit.
> This bit is set to "1" when V_{DD} is lower than the judgment voltage selected by LD0 and LD1, and is set to "0" when V_{DD} is higher. This bit is "0" when the BLD circuit stops operation.
> This bit is read-only and writes are invalid.

bit 2: ENBL
> This bit turns the battery low detect circuit ON or OFF.
> When ENBL is set to "1", the battery low detect circuit is ON. When ENBL is set to "0", the battery low detect circuit is OFF.
> At system reset, this bit is cleared to "0".

bit 1, 0: LD1, LD0
> These bits select the judgment voltage.
> At system reset, these bits are cleared to "0".

16.5 Battery Low Detect Circuit Operation

The battery low detect circuit is turned ON or OFF by ENBL (bit 2 of BLDCON), and outputs to BLDF (bit 3 of BLDCON) the result of a comparison with the judgment voltage.

ENBL is the enable control bit for the battery low detect circuit. Setting ENBL to "1" turns ON the battery low detect circuit. Setting ENBL to "0" turns OFF the battery low detect circuit and BLD current supply drops to zero.

BLDF is the judgment result flag. If BLDF is "1", the power supply voltage is lower than the judgment voltage. If BLDF is "0", the power supply voltage is higher than the judgment voltage. BLDF is valid when ENBL is "1".

The judgment circuit of the battery low detect circuit requires time to become stable. Therefore, after setting ENBL to "1", wait at least 1 ms before reading BLDF. No load should be applied to the power supply voltage during the detection.

Figure 16-2 shows an example operation timing.
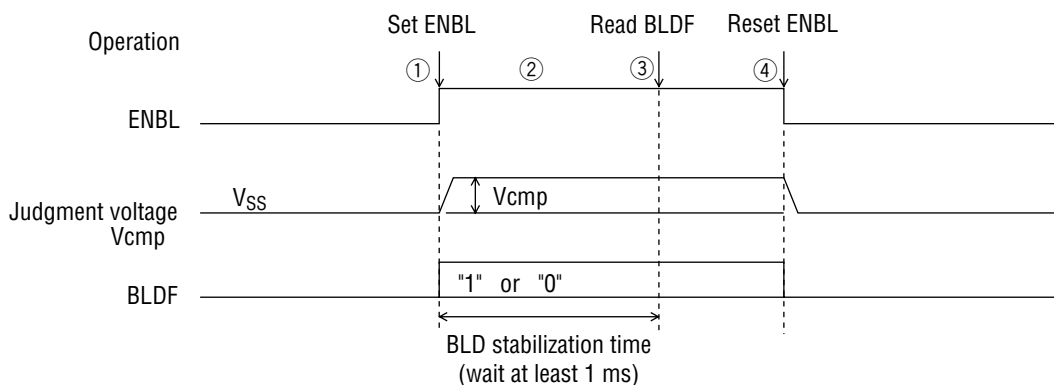
Figure 16-2 Operation Timing Example

Figure 16-2 shows the following operations.

    ① ENBL is set to "1" to turn ON the BLD.

    ② Operation starts with no load applied to power supply system and waits for BLD stabilization time interval (at least 1 ms).

    ③ Judgment result flag (BLDF) is read.

    ④ ENBL is cleared to "0".

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Power Supply Circuit (POWER)

Chapter 17 Power Supply Circuit (POWER)

17.1 Overview

The ML63326 contains a constant voltage circuit for the internal logic power supply (V_{DDL}), a constant voltage circuit for the LCD bias reference power supply (V_{DD2}), and a voltage doubler circuit for the power supply for high-speed oscillation (V_{DDH}).

17.2 Power Supply Circuit Configuration

Figure 17-1 shows the power supply circuit configuration.

Figure 17-1 Power Supply Circuit Configuration

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17.3 Power Supply Circuit Operation

The V_{DDL} output of the power supply for the internal logic circuits is automatically switched to the V_{DD} level when the time base counter is reset, and changes to 1.7 V immediately after the reset state is released. Further, the V_{DDL} output is switched to the V_{DD} level when ENOSC (bit 1 of FCON) is set to "1", and returns to 1.7 V when ENOSC is set to "0".

The V_{DD2} output of the LCD bias reference power supply is automatically switched to the V_{DD} level when the time base counter is reset, and changes to the voltage (1.8V to 2.4 V) selected by the display contrast register (DSPCNT) immediately after the reset state is released.

The V_{DDH} output of the power supply for high-speed oscillation becomes about 1.2 V after the time base counter is reset and while the high-speed oscillations have been stopped (ENOSC = "0") because it is connected via V_{DD2} and a diode. When the high-speed oscillations are started (ENOSC = "1"), the voltage doubler circuit starts operating and V_{DDH} becomes a voltage equal to about two times V_{DD2}.
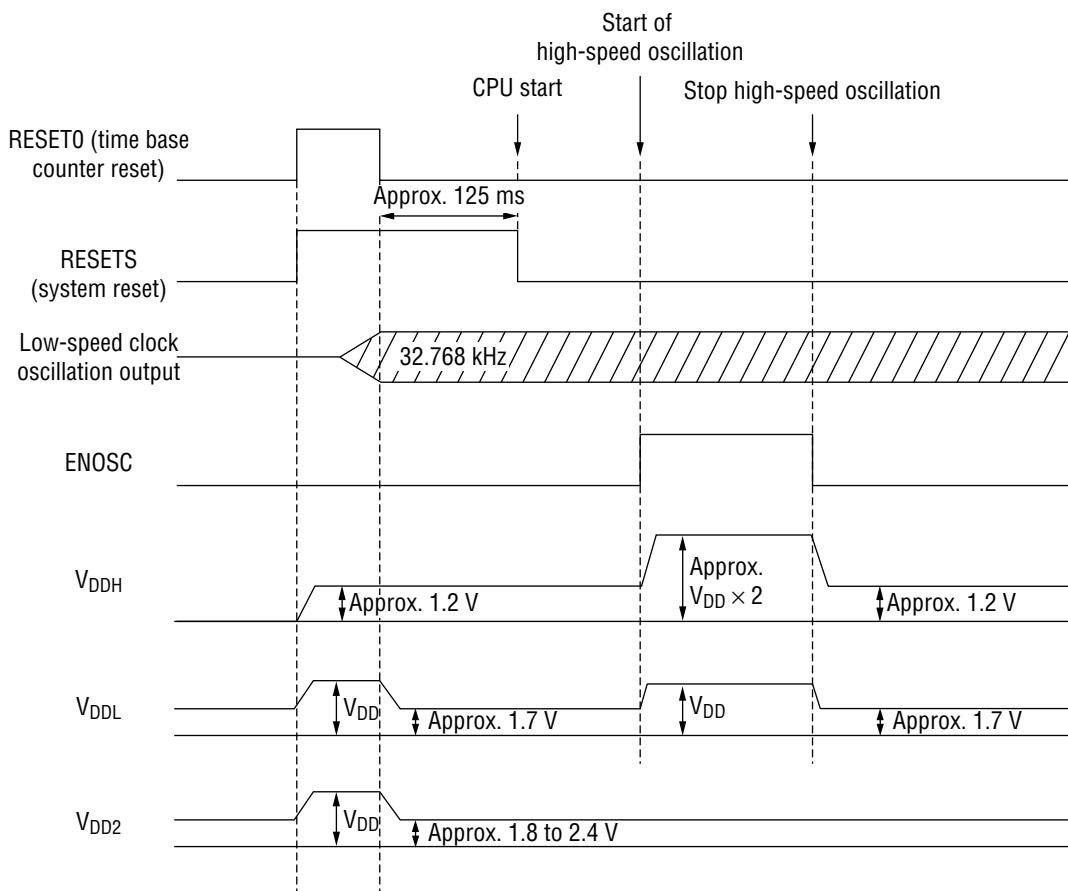
Figure 17-2 Power Supply Circuit Operation Waveforms

Appendixes

Appendix A List of Special Function Registers

The Special Function Registers of the ML63326 are listed in Table A.

Table A Special Function Register List

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Port 0 data register	P0D	000H	P03	P02	P01	P00	R	Undefined
Port 1 data register	P1D	001H	—	—	P11	P10	R	0FH
Port 2 data register	P2D	002H	P23	P22	P21	P20	R/W	0H
Port 3 data register	P3D	003H	P33	P32	P31	P30	R/W	0H
Port 4 data register	P4D	004H	P43	P42	P41	P40	R/W	0H
Port 5 data register	P5D	005H	P53	P52	P51	P50	R/W	0H
Port 6 data register	P6D	006H	P63	P62	P61	P60	R/W	0H
Port 7 data register	P7D	007H	P73	P72	P71	P70	R/W	0H
Port 8 data register	P8D	008H	P83	P82	P81	P80	R/W	0H
Port 9 data register	P9D	009H	P93	P92	P91	P90	R/W	0H
Port A data register	PAD	00AH	PA3	PA2	PA1	PA0	R/W	0H
Port B data register	PBD	00BH	PB3	PB2	PB1	PB0	R/W	0H
Port C data register	PCD	00CH	PC3[*1]	PC2	PC1	PC0	R/W	0H
Port D data register	PDD	00DH	PD3[*1]	—	PD1	PD0	R/W	0CH
Port E data register	PED	00EH	PE3	PE2	PE1	PE0	R/W	0H
Port F data register	PFD	00FH	PF3	PF2	PF1	PF0	R/W	0H
Port 0 control register 0	P0CON0	010H	P03MD	P02MD	P01MD	P00MD	R/W	0H
Port 0 control register 1	P0CON1	011H	—	—	P0PUD	P0F	R/W	0CH
Port 0 interrupt enable register	P0IE	012H	P03IE	P02IE	P01IE	P00IE	R/W	0H
Port 1 control register 0	P1CON0	013H	—	—	P11MD	P10MD	W	—
Reserved		014H to 019H						
Port 4 control register 0	P4CON0	01AH	P41MD1	P41MD0	P40MD1	P40MD0	R/W	0H
Port 4 control register 1	P4CON1	01BH	P43MD1	P43MD0	P42MD1	P42MD0	R/W	0H
Port 5 control register 0	P5CON0	01CH	P51MD1	P51MD0	P50MD1	P50MD0	R/W	0H
Port 5 control register 1	P5CON1	01DH	P53MD1	P53MD0	P52MD1	P52MD0	R/W	0H
Port 6 control register 0	P6CON0	01EH	P61MD1	P61MD0	P60MD1	P60MD0	R/W	0H
Port 6 control register 1	P6CON1	01FH	P63MD1	P63MD0	P62MD1	P62MD0	R/W	0H

⚠ Note:

*1: The bit PC3 can only be read out. The bit PD3 can only be written in.

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Port 7 control register 0	P7CON0	020H	P71MD1	P71MD0	P70MD1	P70MD0	R/W	0H
Port 7 control register 1	P7CON1	021H	P73MD1	P73MD0	P72MD1	P72MD0	R/W	0H
Port 47 mode register	P47MOD	022H	P7MOD	P6MOD	P5MOD	P4MOD	R/W	0H
Port 8 control register 0	P8CON0	023H	P81MD1	P81MD0	P80MD1	P80MD0	R/W	0H
Reserved		024H						
Port 8 direction register	P8DIR	025H	P83DIR	P82DIR	P81DIR	P80DIR	R/W	0H
Port 8 mode register	P8MOD	026H	—	—	P81MOD	P80MOD	R/W	0CH
Port 9 control register 0	P9CON0	027H	P91MD1	P91MD0	P90MD1	P90MD0	R/W	0H
Port 9 control register 1	P9CON1	028H	P93MD1	P93MD0	P92MD1	P92MD0	R/W	0H
Port 9 direction register	P9DIR	029H	P93DIR	P92DIR	P91DIR	P90DIR	R/W	0H
Port A control register 0	PACON0	02AH	PA1MD1	PA1MD0	PA0MD1	PA0MD0	R/W	0H
Port A control register 1	PACON1	02BH	PA3MD1	PA3MD0	PA2MD1	PA2MD0	R/W	0H
Port A direction register	PADIR	02CH	PA3DIR	PA2DIR	PA1DIR	PA0DIR	R/W	0H
Port 9A mode register	P9AMOD	02DH	—	—	PAMOD	P9MOD	R/W	0CH
Port B control register 0	PBCON0	02EH	PB1MD1	PB1MD0	PB0MD1	PB0MD0	R/W	0H
Port B control register 1	PBCON1	02FH	PB3MD1	PB3MD0	PB2MD1	PB2MD0	R/W	0H
Port B direction register	PBDIR	030H	PB3DIR	PB2DIR	PB1DIR	PB0DIR	R/W	0H
Port B interrupt enable register	PBIE	031H	PB3IE	PB2IE	PB1IE	PB0IE	R/W	0H
Port B mode register	PBMOD	032H	PBF	—	PB1MOD	PB0MOD	R/W	4H
Reserved		033H						
Port C control register 1	PCCON1	034H	PC3MD1	PC3MD0	—	—	W	—
Port C direction register	PCDIR	035H	PC3DIR	PC2DIR	PC1DIR	PC0DIR	W	—
Port C interrupt enable register	PCIE	036H	PC3IE	—	—	—	R/W	7H
Port C mode register 0	PCMOD0	037H	—	—	—	PCF	R/W	0EH
Reserved		038H 039H 03AH						
Port D direction register	PDDIR	03BH	PD3DIR	—	PD1DIR	PD0DIR	W	—
Reserved		03CH						
Port E control register 0	PECON0	03DH	PE1MD1	PE1MD0	PE0MD1	PE0MD0	R/W	0H
Port E control register 1	PECON1	03EH	PE3MD1	PE3MD0	PE2MD1	PE2MD0	R/W	0H
Port E direction register	PEDIR	03FH	PE3DIR	PE2DIR	PE1DIR	PE0DIR	R/W	0H

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Port E mode register	PEMOD	040H	PEF	PE2MOD	PE1MOD	PE0MOD	R/W	0H
Port F control register 0	PFCON0	041H	PF1MD1	PF1MD0	PF0MD1	PF0MD0	R/W	0H
Port F control register 1	PFCON1	042H	PF3MD1	PF3MD0	PF2MD1	PF2MD0	R/W	0H
Port F direction register	PFDIR	043H	PF3DIR	PF2DIR	PF1DIR	PF0DIR	R/W	0H
Port F interrupt enable register	PFIE	044H	PF3IE	PF2IE	PF1IE	PF0IE	R/W	0H
Port F mode register	PEMOD	045H	—	—	—	PFF	R/W	0EH
Reserved		046H to 04FH						
Interrupt enable register 0	IE0	050H	EVI	EXI0	EMD	—	R/W	1H
Interrupt enable register 1	IE1	051H	EXI5	—	EXI3	EXI2	R/W	4H
Interrupt enable register 2	IE2	052H	ETM3	ETM2	ETM1	ETM0	R/W	0H
Interrupt enable register 3	IE3	053H	E10Hz	ESFT	—	—	R/W	3H
Interrupt enable register 4	IE4	054H	E2Hz	E4Hz	E16Hz	E32Hz	R/W	0H
Interrupt request register 0	IRQ0	055H	QVI	QXI0	QMD	QWDT	R/W	0H
Interrupt request register 1	IRQ1	056H	QXI5	—	QXI3	QXI2	R/W	4H
Interrupt request register 2	IRQ2	057H	QTM3	QTM2	QTM1	QTM0	R/W	0H
Interrupt request register 3	IRQ3	058H	Q10Hz	QSFT	—	—	R/W	3H
Interrupt request register 4	IRQ4	059H	Q2Hz	Q4Hz	Q16Hz	Q32Hz	R/W	0H
Reserved		05AH to 05FH						
Time base counter register 0	TBCR0	060H	16Hz	32Hz	64Hz	128Hz	R/W	0H
Time base counter register 1	TBCR1	061H	1Hz	2Hz	4Hz	8Hz	R/W	0H
Frequency control register	FCON	062H	—	OSCSEL	ENOSC	CPUCLK	R/W	8H
Reserved		063H						
100 Hz timer counter register	T100CR	064H	100C3	100C2	100C1	100C0	R/W	Undefined
10 Hz timer counter register	T10CR	065H	10C3	10C2	10C1	10C0	R/W	0H
100 Hz timer counter control register	T100CON	066H	—	—	—	ECNT	R/W	0EH
Reserved		067H						
Timer 0 data register L	TM0DL	068H	T0D3	T0D2	T0D1	T0D0	R/W	0H
Timer 0 data register H	TM0DH	069H	T0D7	T0D6	T0D5	T0D4	R/W	0H
Timer 1 data register L	TM1DL	06AH	T1D3	T1D2	T1D1	T1D0	R/W	0H
Timer 1 data register H	TM1DH	06BH	T1D7	T1D6	T1D5	T1D4	R/W	0H
Timer 0 counter register L	TM0CL	06CH	T0C3	T0C2	T0C1	T0C0	R/W	0H
Timer 0 counter register H	TM0CH	06DH	T0C7	T0C6	T0C5	T0C4	R/W	0H
Timer 1 counter register L	TM1CL	06EH	T1C3	T1C2	T1C1	T1C0	R/W	0H
Timer 1 counter register H	TM1CH	06FH	T1C7	T1C6	T1C5	T1C4	R/W	0H

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Timer 0 control register 0	TM0CON0	070H	—	FMEAS0	TM0ECAP	TM0RUN	R/W	8H
Timer 0 control register 1	TM0CON1	071H	—	—	TM0CL1	TM0CL0	R/W	0CH
Timer 1 control register 0	TM1CON0	072H	—	—	TM1ECAP	TM1RUN	R/W	0CH
Timer 1 control register 1	TM1CON1	073H	—	—	TM1CL1	TM1CL0	R/W	0CH
Timer 0 status register	TM0STAT	074H	—	—	TM0CAP	TM0OVF	R	0CH
Timer 1 status register	TM1STAT	075H	—	—	TM1CAP	TM1OVF	R	0CH
Timer 2 data register L	TM2DL	076H	T2D3	T2D2	T2D1	T2D0	R/W	0H
Timer 2 data register H	TM2DH	077H	T2D7	T2D6	T2D5	T2D4	R/W	0H
Timer 3 data register L	TM3DL	078H	T3D3	T3D2	T3D1	T3D0	R/W	0H
Timer 3 data register H	TM3DH	079H	T3D7	T3D6	T3D5	T3D4	R/W	0H
Timer 2 counter register L	TM2CL	07AH	T2C3	T2C2	T2C1	T2C0	R/W	0H
Timer 2 counter register H	TM2CH	07BH	T2C7	T2C6	T2C5	T2C4	R/W	0H
Timer 3 counter register L	TM3CL	07CH	T3C3	T3C2	T3C1	T3C0	R/W	0H
Timer 3 counter register H	TM3CH	07DH	T3C7	T3C6	T3C5	T3C4	R/W	0H
Timer 2 control register 0	TM2CON0	07EH	—	FMEAS2	—	TM2RUN	R/W	0AH
Timer 2 control register 1	TM2CON1	07FH	—	—	TM2CL1	TM2CL0	R/W	0CH
Timer 3 control register 0	TM3CON0	080H	—	—	—	TM3RUN	R/W	0EH
Timer 3 control register 1	TM3CON1	081H	—	—	TM3CL1	TM3CL0	R/W	0CH
Timer 2 status register	TM2STAT	082H	—	—	—	TM2OVF	R	0EH
Timer 3 status register	TM3STAT	083H	—	—	—	TM3OVF	R	0EH
Reserved		084H to 08FH						
Display control register 0	DSPCON0	090H	BISEL	PDWN	ALLON	LCDON	R/W	0H
Display control register 1	DSPCON1	091H	DT3	DT2	DT1	DT0	R/W	0H
Display contrast register	DSPCNT	092H	CN3	CN2	CN1	CN0	R/W	0H
Reserved		093H						
Battery low detect control register	BLDCON	094H	BLDF	ENBL	LD1	LD0	R/W	0H
Reserved		095H						
Tempo register	TEMPO	096H	TMP3	TMP2	TMP1	TMP0	R/W	0H
Melody driver control register	MDCON	097H	MSF	EMBD	MBM1	MBM0	R/W	0H
Reserved		098H to 09EH						
Watchdog timer control register	WDTCON	09FH	d3	d2	d1	d0	W	—

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Shift register L	SFTRL	0A0H	SD3	SD2	SD1	SD0	R/W	0H
Shift register H	SFTRH	0A1H	SD7	SD6	SD5	SD4	R/W	0H
Shift register control register 0	SFTCON0	0A2H	—	SDIR	SELCK1	SELCK0	R/W	8H
Shift register control register 1	SFTCON1	0A3H	—	—	—	ENTR	R/W	0EH
Reserved		0A4H to 0F1H						
RA register 0	RA0	0F2H	a3	a2	a1	a0	R/W	0H
RA register 1	RA1	0F3H	a7	a6	a5	a4	R/W	0H
RA register 2	RA2	0F4H	a11	a10	a9	a8	R/W	0H
RA register 3	RA3	0F5H	a15	a14	a13	a12	R/W	0H
Register stack pointer	RSP	0F6H	rsp3	rsp2	rsp1	rsp0	R/W	0H
Stack pointer	SP	0F7H	sp3	sp2	sp1	sp0	R	0H
Reserved		0F8H						
Y register	Y	0F9H	y3	y2	y1	y0	R/W	0H
X register	X	0FAH	x3	x2	x1	x0	R/W	0H
L register	L	0FBH	l3	l2	l1	l0	R/W	0H
H register	H	0FCH	h3	h2	h1	h0	R/W	0H
Current bank register	CBR	0FDH	c3	c2	c1	c0	R/W	0H
Extra bank register	EBR	0FEH	e3	e2	e1	e0	R/W	0H
Master interrupt enable flag register	MIEF	0FFH	—	—	—	MIE	R	0EH

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 0	DSPR0	100H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 1	DSPR1	101H	SEG0	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 2	DSPR2	102H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 3	DSPR3	103H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 4	DSPR4	104H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 5	DSPR5	105H	SEG1	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 6	DSPR6	106H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 7	DSPR7	107H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 8	DSPR8	108H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 9	DSPR9	109H	SEG2	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 10	DSPR10	10AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 11	DSPR11	10BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 12	DSPR12	10CH		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 13	DSPR13	10DH	SEG3	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 14	DSPR14	10EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 15	DSPR15	10FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 16	DSPR16	110H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 17	DSPR17	111H	SEG4	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 18	DSPR18	112H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 19	DSPR19	113H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 20	DSPR20	114H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 21	DSPR21	115H	SEG5	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 22	DSPR22	116H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 23	DSPR23	117H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 24	DSPR24	118H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 25	DSPR25	119H	SEG6	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 26	DSPR26	11AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 27	DSPR27	11BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 28	DSPR28	11CH		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 29	DSPR29	11DH	SEG7	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 30	DSPR30	11EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 31	DSPR31	11FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 32	DSPR32	120H		COM4	COM3	COM2	COM1	R/W	Undefined
Display register 33	DSPR33	121H	SEG8	COM8	COM7	COM6	COM5	R/W	Undefined
Display register 34	DSPR34	122H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 35	DSPR35	123H		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 36	DSPR36	124H	SEG9	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 37	DSPR37	125H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 38	DSPR38	126H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 39	DSPR39	127H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 40	DSPR40	128H	SEG10	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 41	DSPR41	129H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 42	DSPR42	12AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 43	DSPR43	12BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 44	DSPR44	12CH	SEG11	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 45	DSPR45	12DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 46	DSPR46	12EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 47	DSPR47	12FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 48	DSPR48	130H	SEG12	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 49	DSPR49	131H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 50	DSPR50	132H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 51	DSPR51	133H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 52	DSPR52	134H	SEG13	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 53	DSPR53	135H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 54	DSPR54	136H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 55	DSPR55	137H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 56	DSPR56	138H	SEG14	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 57	DSPR57	139H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 58	DSPR58	13AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 59	DSPR59	13BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 60	DSPR60	13CH	SEG15	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 61	DSPR61	13DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 62	DSPR62	13EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 63	DSPR63	13FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 64	DSPR64	140H	SEG16	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 65	DSPR65	141H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 66	DSPR66	142H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 67	DSPR67	143H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 68	DSPR68	144H	SEG17	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 69	DSPR69	145H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 70	DSPR70	146H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 71	DSPR71	147H		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 72	DSPR72	148H	SEG18	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 73	DSPR73	149H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 74	DSPR74	14AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 75	DSPR75	14BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 76	DSPR76	14CH	SEG19	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 77	DSPR77	14DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 78	DSPR78	14EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 79	DSPR79	14FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 80	DSPR80	150H	SEG20	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 81	DSPR81	151H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 82	DSPR82	152H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 83	DSPR83	153H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 84	DSPR84	154H	SEG21	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 85	DSPR85	155H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 86	DSPR86	156H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 87	DSPR87	157H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 88	DSPR88	158H	SEG22	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 89	DSPR89	159H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 90	DSPR90	15AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 91	DSPR91	15BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 92	DSPR92	15CH	SEG23	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 93	DSPR93	15DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 94	DSPR94	15EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 95	DSPR95	15FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 96	DSPR96	160H	SEG24	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 97	DSPR97	161H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 98	DSPR98	162H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 99	DSPR99	163H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 100	DSPR100	164H	SEG25	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 101	DSPR101	165H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 102	DSPR102	166H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 103	DSPR103	167H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 104	DSPR104	168H	SEG26	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 105	DSPR105	169H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 106	DSPR106	16AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 107	DSPR107	16BH		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 108	DSPR108	16CH	SEG27	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 109	DSPR109	16DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 110	DSPR110	16EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 111	DSPR111	16FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 112	DSPR112	170H	SEG28	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 113	DSPR113	171H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 114	DSPR114	172H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 115	DSPR115	173H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 116	DSPR116	174H	SEG29	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 117	DSPR117	175H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 118	DSPR118	176H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 119	DSPR119	177H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 120	DSPR120	178H	SEG30	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 121	DSPR121	179H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 122	DSPR122	17AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 123	DSPR123	17BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 124	DSPR124	17CH	SEG31	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 125	DSPR125	17DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 126	DSPR126	17EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 127	DSPR127	17FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 128	DSPR128	180H	SEG32	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 129	DSPR129	181H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 130	DSPR130	182H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 131	DSPR131	183H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 132	DSPR132	184H	SEG33	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 133	DSPR133	185H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 134	DSPR134	186H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 135	DSPR135	187H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 136	DSPR136	188H	SEG34	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 137	DSPR137	189H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 138	DSPR138	18AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 139	DSPR139	18BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 140	DSPR140	18CH	SEG35	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 141	DSPR141	18DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 142	DSPR142	18EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 143	DSPR143	18FH		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 144	DSPR144	190H	SEG36	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 145	DSPR145	191H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 146	DSPR146	192H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 147	DSPR147	193H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 148	DSPR148	194H	SEG37	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 149	DSPR149	195H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 150	DSPR150	196H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 151	DSPR151	197H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 152	DSPR152	198H	SEG38	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 153	DSPR153	199H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 154	DSPR154	19AH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 155	DSPR155	19BH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 156	DSPR156	19CH	SEG39	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 157	DSPR157	19DH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 158	DSPR158	19EH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 159	DSPR159	19FH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 160	DSPR160	1A0H	SEG40	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 161	DSPR161	1A1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 162	DSPR162	1A2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 163	DSPR163	1A3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 164	DSPR164	1A4H	SEG41	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 165	DSPR165	1A5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 166	DSPR166	1A6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 167	DSPR167	1A7H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 168	DSPR168	1A8H	SEG42	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 169	DSPR169	1A9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 170	DSPR170	1AAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 171	DSPR171	1ABH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 172	DSPR172	1ACH	SEG43	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 173	DSPR173	1ADH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 174	DSPR174	1AEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 175	DSPR175	1AFH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 176	DSPR176	1B0H	SEG44	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 177	DSPR177	1B1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 178	DSPR178	1B2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 179	DSPR179	1B3H		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 180	DSPR180	1B4H	SEG45	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 181	DSPR181	1B5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 182	DSPR182	1B6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 183	DSPR183	1B7H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 184	DSPR184	1B8H	SEG46	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 185	DSPR185	1B9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 186	DSPR186	1BAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 187	DSPR187	1BBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 188	DSPR188	1BCH	SEG47	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 189	DSPR189	1BDH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 190	DSPR190	1BEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 191	DSPR191	1BFH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 192	DSPR192	1C0H	SEG48	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 193	DSPR193	1C1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 194	DSPR194	1C2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 195	DSPR195	1C3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 196	DSPR196	1C4H	SEG49	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 197	DSPR197	1C5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 198	DSPR198	1C6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 199	DSPR199	1C7H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 200	DSPR200	1C8H	SEG50	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 201	DSPR201	1C9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 202	DSPR202	1CAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 203	DSPR203	1CBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 204	DSPR204	1CCH	SEG51	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 205	DSPR205	1CDH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 206	DSPR206	1CEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 207	DSPR207	1CFH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 208	DSPR208	1D0H	SEG52	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 209	DSPR209	1D1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 210	DSPR210	1D2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 211	DSPR211	1D3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 212	DSPR212	1D4H	SEG53	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 213	DSPR213	1D5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 214	DSPR214	1D6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 215	DSPR215	1D7H		COM16	COM15	COM14	COM13	R/W	Undefined

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset
Display register 216	DSPR216	1D8H	SEG54	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 217	DSPR217	1D9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 218	DSPR218	1DAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 219	DSPR219	1DBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 220	DSPR220	1DCH	SEG55	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 221	DSPR221	1DDH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 222	DSPR222	1DEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 223	DSPR223	1DFH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 224	DSPR224	1E0H	SEG56	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 225	DSPR225	1E1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 226	DSPR226	1E2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 227	DSPR227	1E3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 228	DSPR228	1E4H	SEG57	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 229	DSPR229	1E5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 230	DSPR230	1E6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 231	DSPR231	1E7H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 232	DSPR232	1E8H	SEG58	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 233	DSPR233	1E9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 234	DSPR234	1EAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 235	DSPR235	1EBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 236	DSPR236	1ECH	SEG59	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 237	DSPR237	1EDH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 238	DSPR238	1EEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 239	DSPR239	1EFH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 240	DSPR240	1F0H	SEG60	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 241	DSPR241	1F1H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 242	DSPR242	1F2H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 243	DSPR243	1F3H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 244	DSPR244	1F4H	SEG61	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 245	DSPR245	1F5H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 246	DSPR246	1F6H		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 247	DSPR247	1F7H		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 248	DSPR248	1F8H	SEG62	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 249	DSPR249	1F9H		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 250	DSPR250	1FAH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 251	DSPR251	1FBH		COM16	COM15	COM14	COM13	R/W	Undefined
Display register 252	DSPR252	1FCH	SEG63	COM4	COM3	COM2	COM1	R/W	Undefined
Display register 253	DSPR253	1FDH		COM8	COM7	COM6	COM5	R/W	Undefined
Display register 254	DSPR254	1FEH		COM12	COM11	COM10	COM9	R/W	Undefined
Display register 255	DSPR255	1FFH		COM16	COM15	COM14	COM13	R/W	Undefined

Appendix B Package Dimensions

ML63326-xxxTC

(Unit : mm)
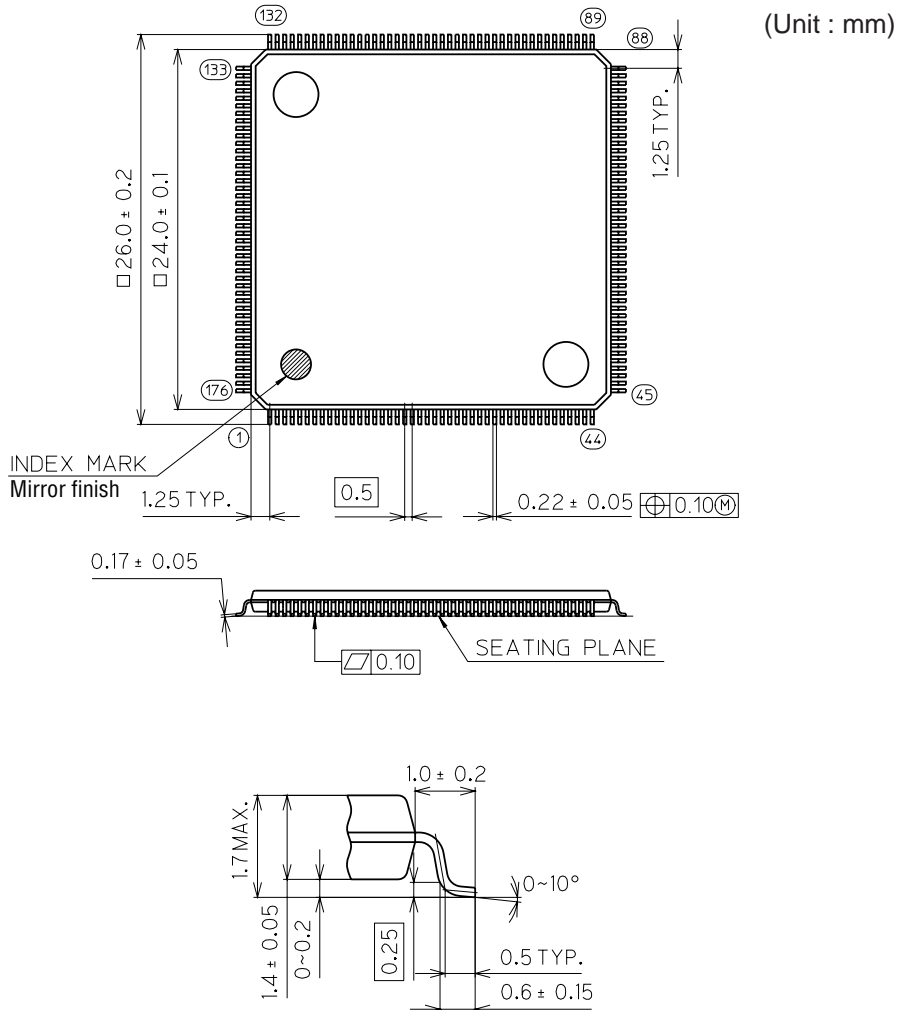
Figure B-1 176-Pin LQFP (LQFP176-P-2424-0.50-BK)

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

Appendix C Input/Output Circuit Configuration

(1) I/O Port (P8.0, P8.1, P9.0–P9.3, PA.0–PA.3, PB.0–PB.3, PE.0–PE.3, PF.0–PF.3)
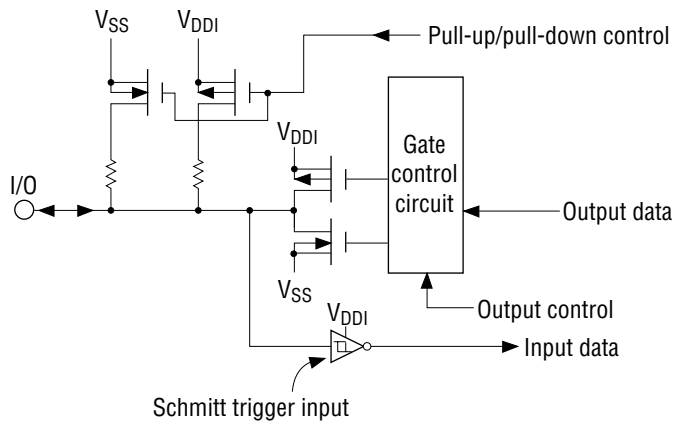
(2) Input Port (P0.0–P0.3)
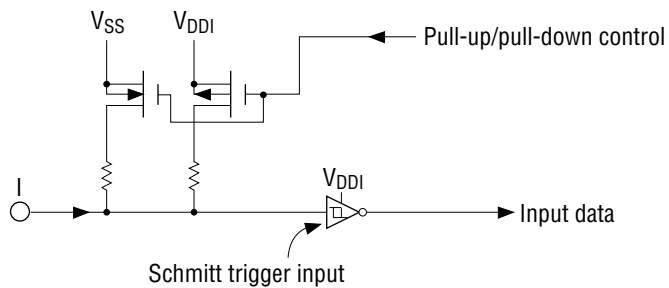
(3) Output Port (P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)
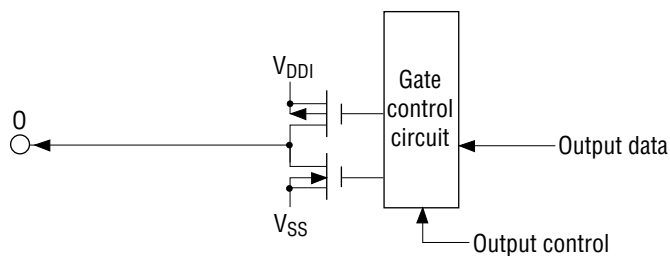
(3) Low-Speed Clock Generator
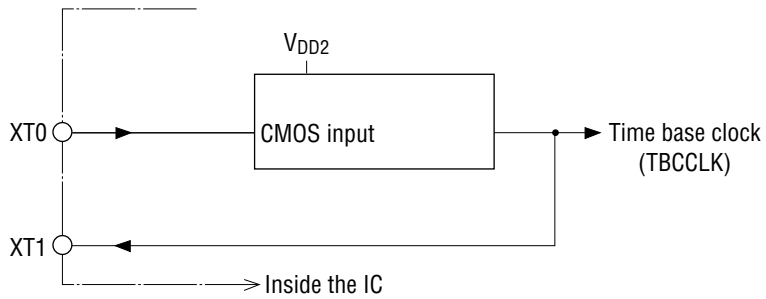
(4) High-Speed Clock Generator
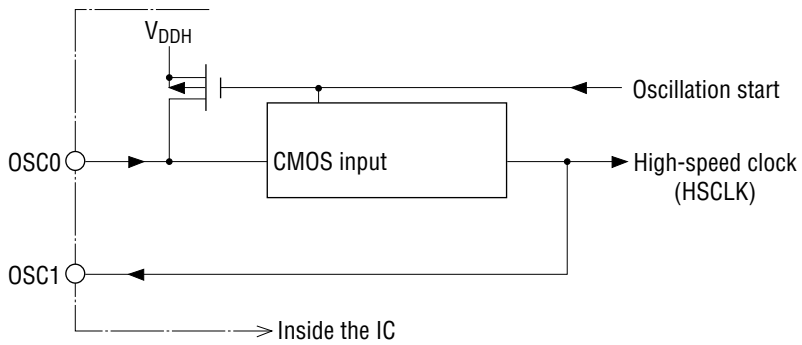
(5) RESET, TST1, TST2, VTEST, and SPEN Inputs
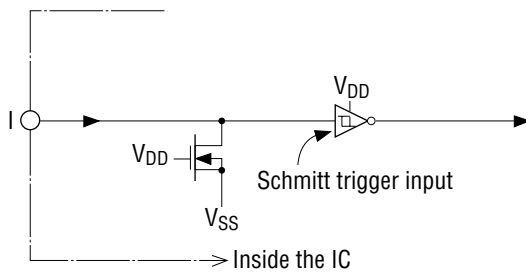
Appendix D Peripheral Circuit Examples
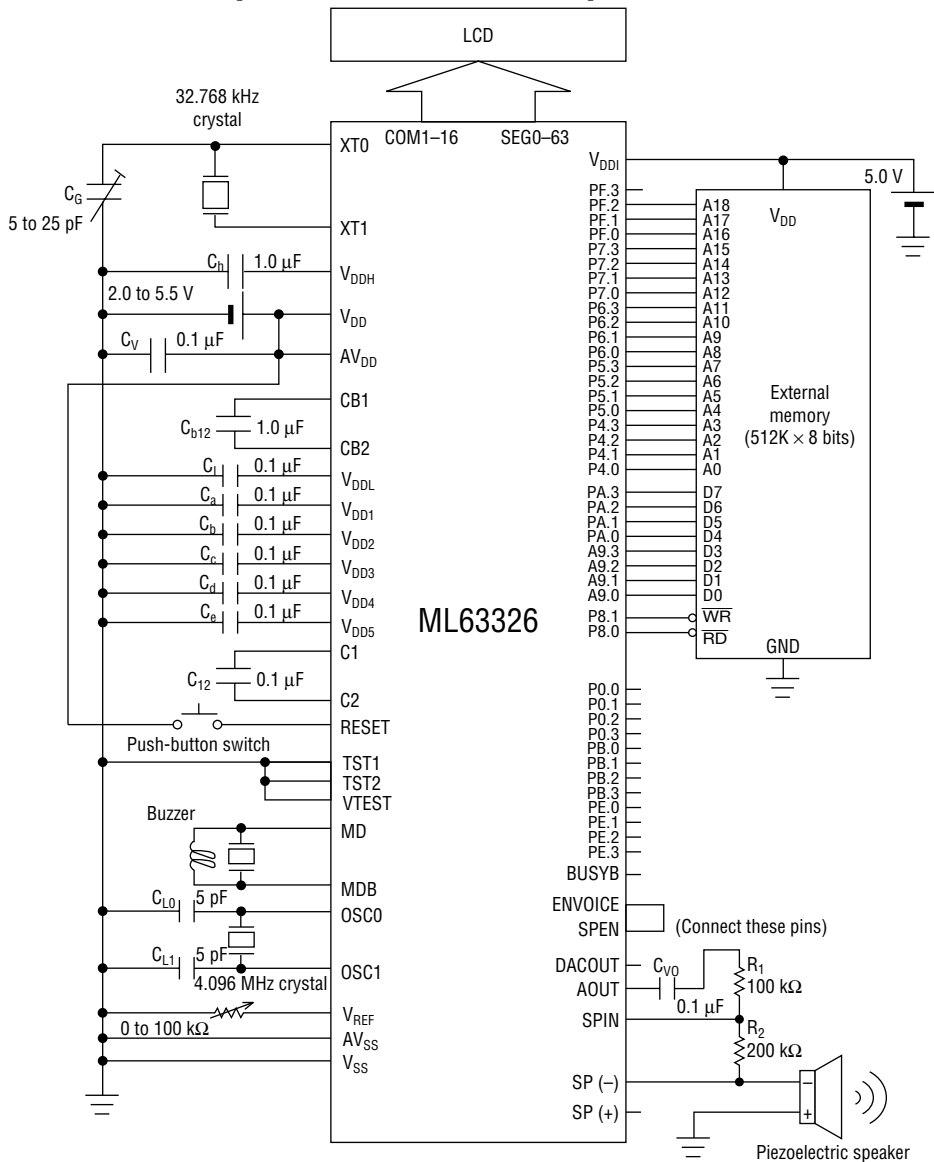
- Crystal oscillation is selected by mask option for low-speed oscillation.
- Crystal oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, C_V, C_{L0}, C_{L1}, C_{VO}, and C_G are only for reference.

Figure D-1 Example 1 of Peripheral Circuit (low-speed side: crystal oscillation, high-speed side: crystal oscillation)

⚠ Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.
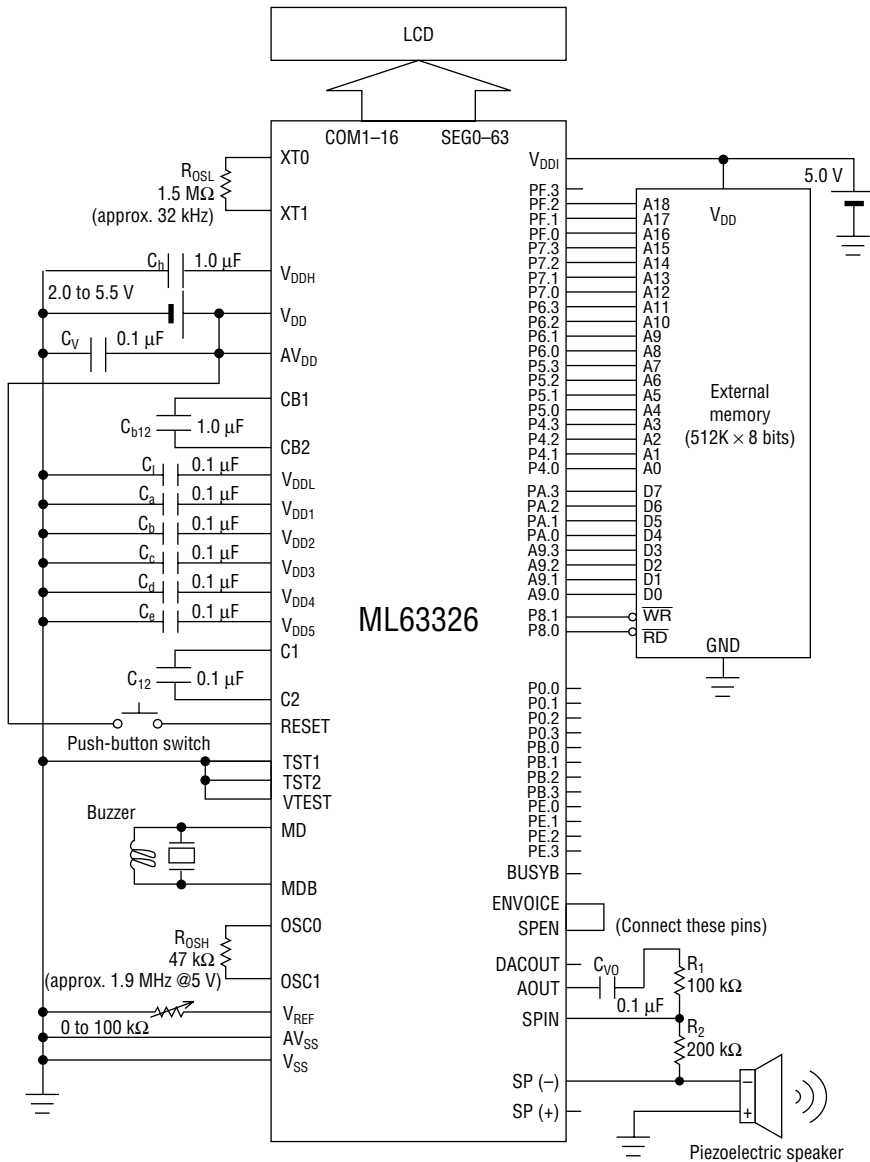
- RC oscillation is selected by mask option for low-speed oscillation.
- RC oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, C_V, and C_{VO} are only for reference.

Figure D-2 Example 2 of Peripheral Circuit (low-speed side: RC oscillation, high-speed side: RC oscillation)

⚠ Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.
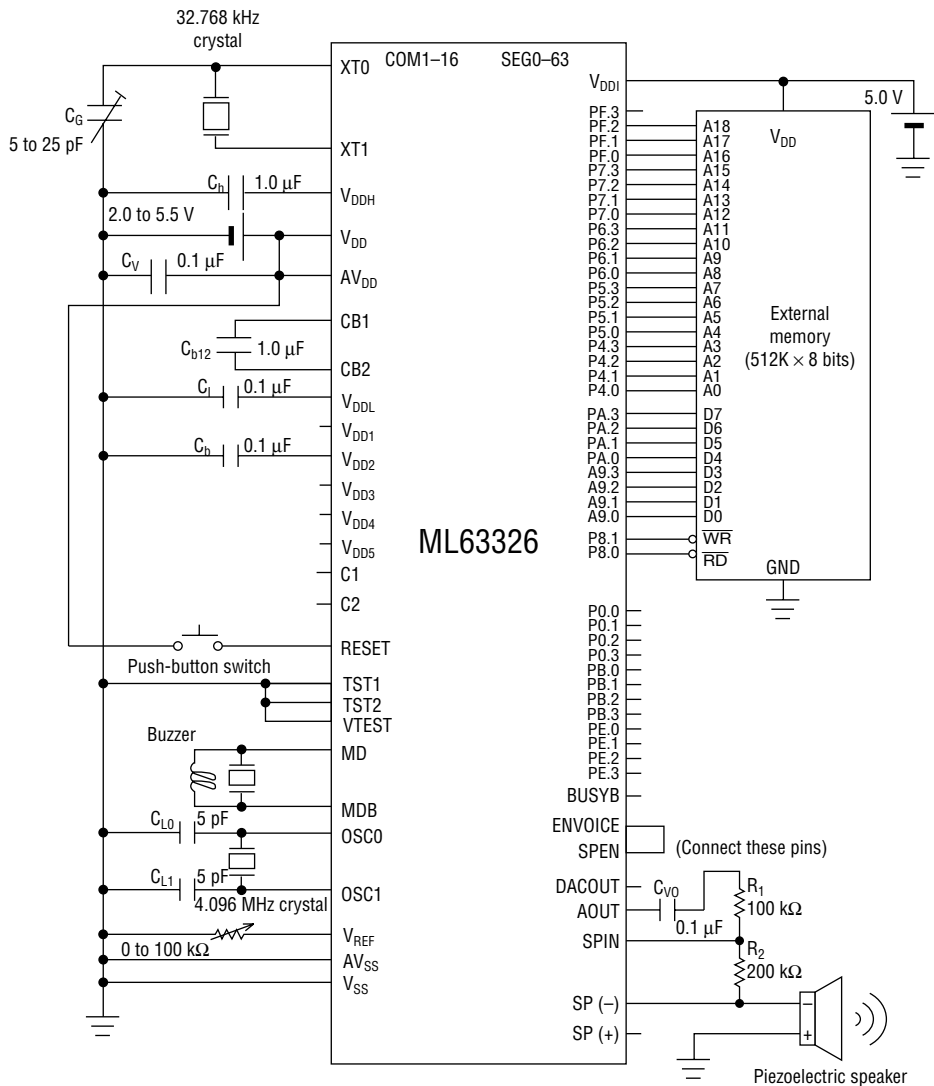
- Crystal oscillation is selected by mask option for low-speed oscillation.
- Crystal oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- Capacitance values for C_b, C_l, C_{b12}, C_h C_V, C_{L0}, C_{L1}, C_{VO}, and C_G are only for reference.

Figure D-3   Example 3 of Peripheral Circuit (low-speed side: crystal oscillation, high-speed side: crystal oscillation, when LCD driver is not used)

⚠ Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.
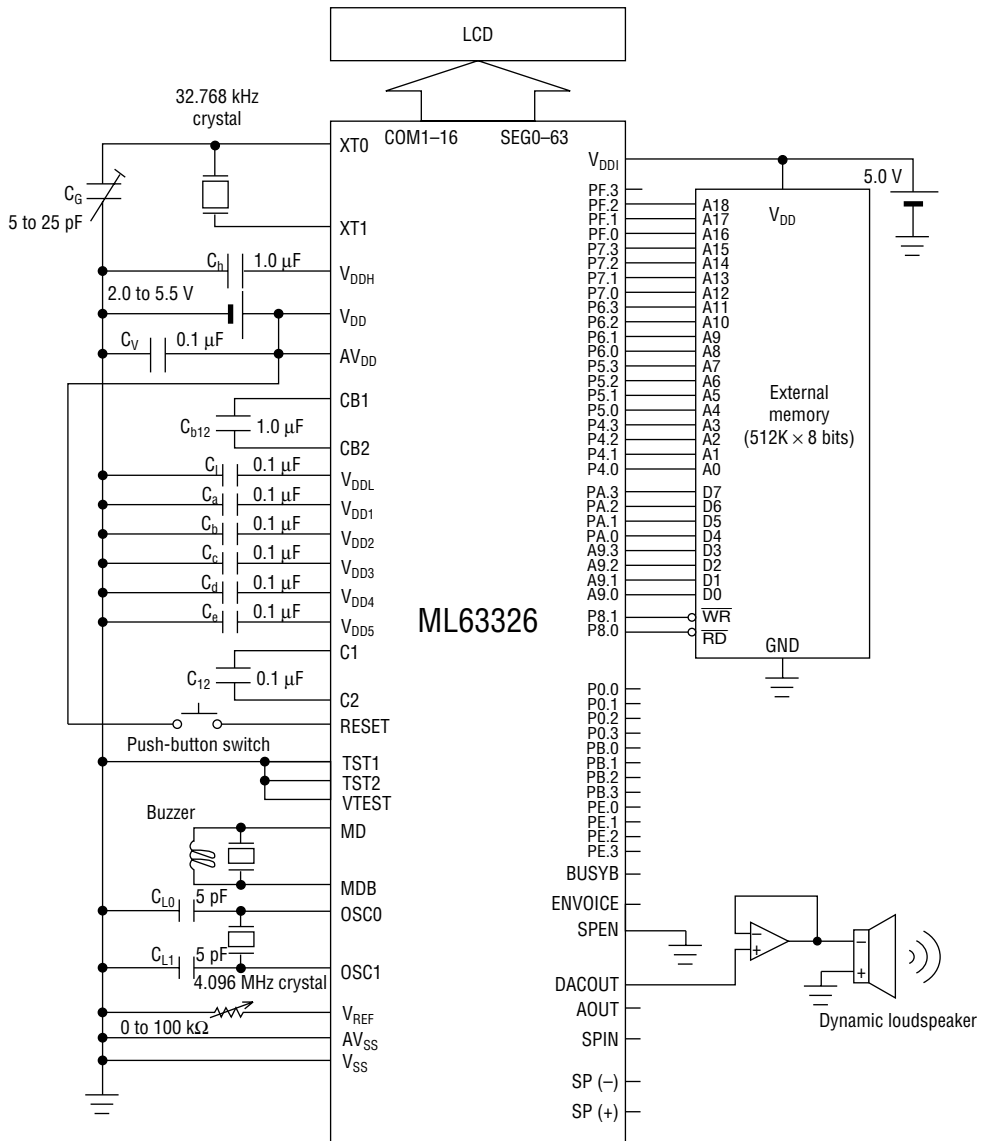
- Crystal oscillation is selected by mask option for low-speed oscillation.
- Crystal oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, C_V, C_{L0}, C_{L1}, and C_G are only for reference.

Figure D-4 Example 4 of Peripheral Circuit (low-speed side: crystal oscillation, high-speed side: crystal oscillation, when the built-in amplifiers in the voice synthesis section are not used)

⚠ Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.
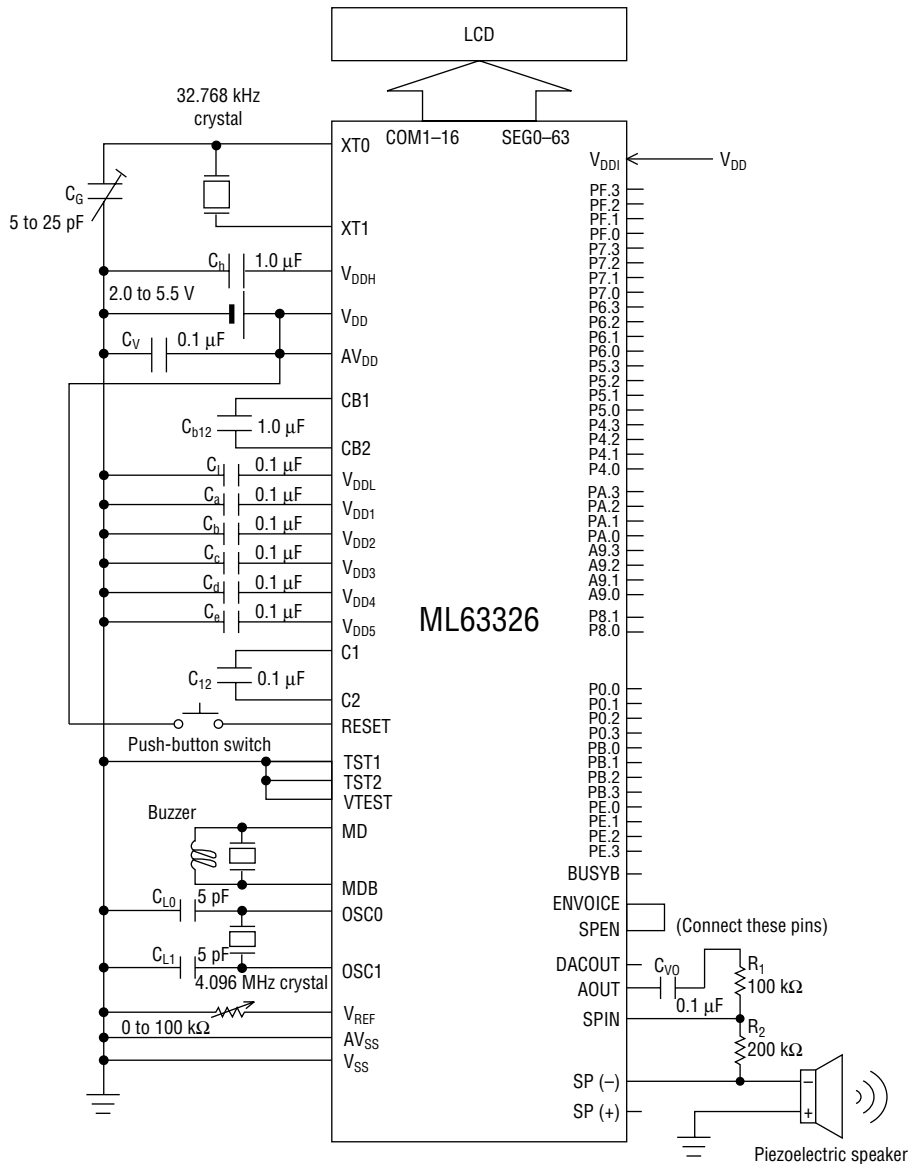
- Crystal oscillation is selected by mask option for low-speed oscillation.
- Crystal oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, C_V, C_{L0}, C_{L1}, C_{VO}, and C_G are only for reference.

Figure D-5 Example 5 of Peripheral Circuit (low-speed side: crystal oscillation, high-speed side: crystal oscillation, when the external memory is not used)

⚠ Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.

Appendix E Electrical Characteristics (Preliminary)

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD1}	Ta = 25°C	−0.3 to +1.6	V
Power Supply Voltage 2	V_{DD2}	Ta = 25°C	−0.3 to +2.9	V
Power Supply Voltage 3	V_{DD3}	Ta = 25°C	−0.3 to +4.2	V
Power Supply Voltage 4	V_{DD4}	Ta = 25°C	−0.3 to +5.5	V
Power Supply Voltage 5	V_{DD5}	Ta = 25°C	−0.3 to +6.8	V
Power Supply Voltage 6	V_{DD}	Ta = 25°C	−0.3 to +6.0	V
Power Supply Voltage 7	V_{DDI}	Ta = 25°C	−0.3 to +6.0	V
Power Supply Voltage 8	V_{DDH}	Ta = 25°C	−0.3 to +6.0	V
Power Supply Voltage 9	V_{DDL}	Ta = 25°C	−0.3 to +6.0	V
Power Supply Voltage 10	AV_{DD}	Ta = 25°C	−0.3 to +6.0	V
Power Supply Voltage 11	V_{REF}	Ta = 25°C	−0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} input, Ta = 25°C	−0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} output, Ta = 25°C	−0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} output, Ta = 25°C	−0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} output, Ta = 25°C	−0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} output, Ta = 25°C	−0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} output, Ta = 25°C	−0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD} output, Ta = 25°C	−0.3 to V_{DD} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDI} output, Ta = 25°C	−0.3 to V_{DDI} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDH} output, Ta = 25°C	−0.3 to V_{DDH} + 0.3	V
Output Voltage 9	V_{OUT9}	AV_{DD} output, Ta = 25°C	−0.3 to AV_{DD} + 0.3	V
Power Dissipation	P_D	Ta = 25°C	100	mW
Storage Temperature	T_{STG}	—	−55 to +150	°C

Recommended Operating Conditions

$(V_{SS} = 0 \text{ V})$

Parameter	Symbol	Condition		Range	Unit
Operating Temperature	T_{op}	—		−20 to +70	℃
Operating Voltage	V_{DD}	—		2.0 to 5.5	V
	V_{DDI}	—		2.0 to 5.5	
	AV_{DD}	—		2.0 to 5.5	
	V_{REF}	—		0.5 to $(AV_{DD} − 1.0 \text{ V})$	
Crystal Oscillation Frequency	f_{XT}	$C_G = 5$ to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	$R_{OSL} = 1.5 \text{ M}\Omega$		32 ±30%	kHz
		$R_{OSL} = 700 \text{ k}\Omega$		60 ±30%	
		$R_{OSL} = 400 \text{ k}\Omega$		80 ±30%	
High-speed Crystal Oscillation Frequency	f_{CM}	$V_{DDH} = 3.6$ to 5.5 V		4.096	MHz
High-speed RC Oscillation Frequency	f_{ROSH}	$V_{DDH} = 3.6$ to 5.0 V	$R_{OSH} = 47 \text{ k}\Omega$	1.8 ±30%	MHz
			$R_{OSH} = 39 \text{ k}\Omega$	2.0 ±30%	

• Typical characteristics of low-speed RC oscillation
  When V_{DD2} = 1.8 V

Reference data

f_{ROSL} [kHz] vs R_{OSL} [kΩ]
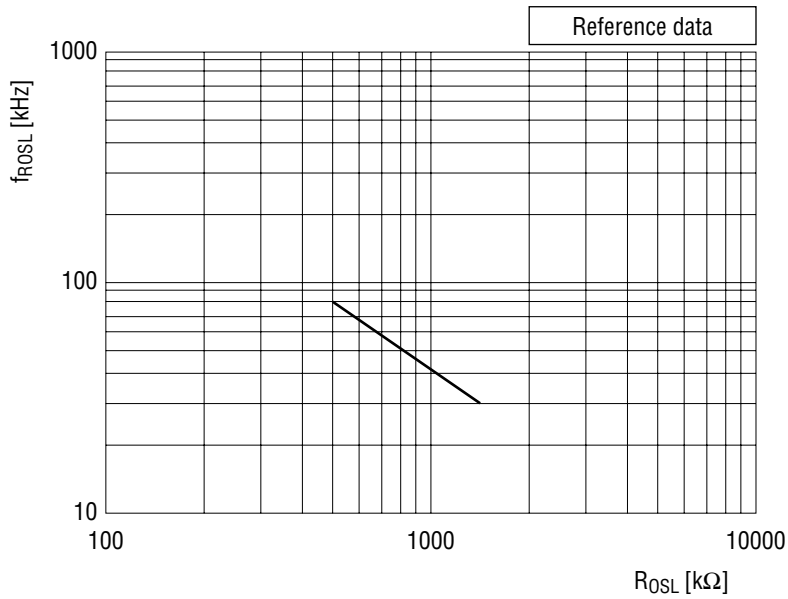
• Typical characteristics of high-speed RC oscillation
  When V_{DDH} = 3.6 V

Reference data

f_{ROSH} [kHz] vs R_{OSH} [kΩ]
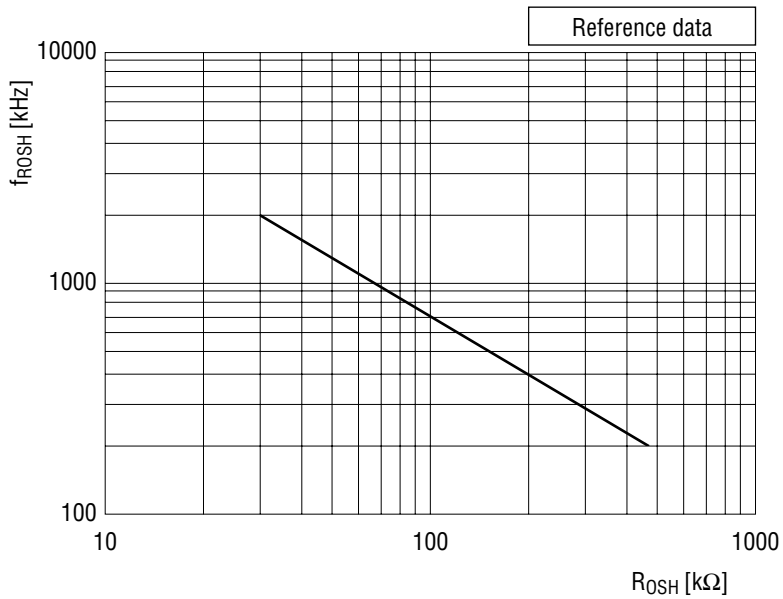
DC Characteristics

$(V_{DD} = V_{DDI} = AV_{DD} = 2.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, Ta $= -20$ to $+70$°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias (Ta = 25°C)	1.7	1.8	1.9	V	
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	−4	—	mV/°C	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ.− 0.1	$1/2 \times V_{DD2}$	Typ.+ 0.1	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ.− 0.3	$3/2 \times V_{DD2}$	Typ.+ 0.3	V	
		1/4 bias (connect V_{DD3} and V_{DD2})	Typ.− 0.2	V_{DD2}	Typ.+ 0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ.− 0.4	$2 \times V_{DD2}$	Typ.+ 0.4	V	
		1/4 bias	Typ.− 0.3	$3/2 \times V_{DD2}$	Typ.+ 0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ.− 0.5	$5/2 \times V_{DD2}$	Typ.+ 0.5	V	
		1/4 bias	Typ.− 0.4	$2 \times V_{DD2}$	Typ.+ 0.4		
V_{DDH} Voltage	V_{DDH}	High-speed clock oscillation stopped $V_{DD} = 1.8$ V	—	1.2	—	V	1
		High-speed clock oscillation $V_{DD} = 1.8$ V	2.0	3.6	3.7	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.2	1.7	2.2	V	
		High-speed clock oscillation ($V_{DD} = 2.0$ to 5.5 V)	2.0	—	5.5	V	
V_{REF} Voltage	V_{REF}	$AV_{DD} = 3.0$ V	0.6	—	2.4	V	
		$AV_{DD} = 5.0$ V	1.0	—	4.0		
Low-speed Crystal Oscillation Start Voltage	V_{STAL}	Oscillation start time: within 5 seconds	2.0	—	—	V	
High-speed Crystal Oscillation Start Voltage	V_{STAH}	Oscillation start time: within 10 milliseconds	2.0	—	—	V	
Low-speed & High-speed Crystal Oscillation Hold Voltage	V_{HOLD}	—	1.8	—	—	V	
Low-speed Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
Low-speed External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Low-speed Internal Crystal Oscillator Capacitance	C_D	—	20	25	30	pF	
High-speed External Crystal Oscillator Capacitance	$C_{L0, 1}$	AT-49 4.096 MHz (Daishinku Corp.-make) used, $V_{DD} = 5.0$ V	5	8	20	pF	
High-speed Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = AV_{DD} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = −20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
POR Voltage	V_{POR1}	V_{DD} = 2.0 V	0.0	—	0.5	V	1
		V_{DD} = 3.0 V	0.0	—	0.7		
		V_{DD} = 5.0 V	0.0	—	1.5		
Non-POR Voltage	V_{POR2}	V_{DD} = 2.0 V	1.5	—	2.0	V	
		V_{DD} = 3.0 V	2.0	—	3.0		
		V_{DD} = 5.0 V	3.5	—	5.0		
BLD Judgment Voltage	V_{BLDC}	LD1 = 1, LD0 = 1, Ta = 25°C	2.3	2.4	2.5	V	—
		LD1 = 1, LD0 = 0, Ta = 25°C	2.1	2.2	2.3		
		LD1 = 0, LD0 = 1, Ta = 25°C	1.9	2.0	2.1		
BLD Judgment Voltage Temperature Deviation	ΔV_{BLDC}	V_{BLDC} = 2.40 V (LD1 = 1, LD0 = 1)	—	−3.5	—	mV/°C	
		V_{BLDC} = 2.20 V (LD1 = 1, LD0 = 0)	—	−3.0	—		
		V_{BLDC} = 2.00 V (LD1 = 0, LD0 = 1)	—	−2.5	—		

Notes: 1. "V_{DD2}" changes in the range from 1.8 V to 2.4 V according to the value of Display Contrast register (DSPCNT).

2. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.

3. "POR" denotes Power On Reset.

4. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.

5. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (continued)

(V_{DD} = V_{DDI} = AV_{DD} = 3.0 V, V_{SS} = AV_{SS} = 0 V, 1/5 bias, Ta = −20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = −20 to +50°C	—	2	6	μA	
			Ta = −20 to +70°C	—	2	12		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = −20 to +50°C	—	1.5	3.0	μA	
			Ta = −20 to +70°C	—	1.5	10.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = −20 to +50°C	—	8	12	μA	1
			Ta = −20 to +70°C	—	8	15	μA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, R_{OSH} = 47 kΩ)		—	500	650	μA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Crystal oscillation, 4.096 MHz)		—	800	1000	μA	
Supply Current 6	I_{DD6}	CPU is in operation at high-speed oscillation (Crystal oscillation, 4.096 MHz) The state in which voice is being output		—	5	10	mA	

DC Characteristics (continued)

$(V_{DD} = V_{DDI} = V_{DDH} = AV_{DD} = 3.0$ V, $V_{DD1} = 1.1$ V, $V_{DD2} = 2.2$ V, $V_{DD3} = 3.3$ V, $V_{DD4} = 4.4$ V,
$V_{DD5} = 5.5$ V, $V_{SS} = AV_{SS} = 0$ V, Ta = -20 to $+70°C$ unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) (P7.0 to P7.3) (P8.0, P8.1) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3) (PF.0 to PF.3) (BUSYB) (ENVOICE)	I_{OH1}	$V_{OH1} = V_{DDI} - 0.5$ V	$V_{DDI} = 3.0$ V	-6.0	-3.5	-1.0	mA	
			$V_{DDI} = 5.0$ V	-8.5	-5.0	-1.5	mA	
	I_{OL1}	$V_{OL1} = 0.5$ V	$V_{DDI} = 3.0$ V	1.0	3.0	6.0	mA	
			$V_{DDI} = 5.0$ V	1.5	3.7	8.5	mA	
Output Current 2 (MD, MDB)	I_{OH2}	$V_{OH2} = AV_{DD} - 0.7$ V	$AV_{DD} = 3.0$ V	-11.0	-6.0	-2.0	mA	
			$AV_{DD} = 5.0$ V	-14.0	-9.0	-4.0	mA	
	I_{OL2}	$V_{OL2} = 0.7$ V	$AV_{DD} = 3.0$ V	2.0	5.5	11.0	mA	
			$AV_{DD} = 5.0$ V	4.0	7.0	14.0	mA	
Output Current 3 (SEG0 to SEG63) (COM1 to COM16)	I_{OH3}	$V_{OH3} = V_{DD5} - 0.2$ V (V_{DD5} level)		—	—	-4	µA	2
	I_{OHM3}	$V_{OHM3} = V_{DD4} + 0.2$ V (V_{DD4} level)		4	—	—	µA	
	I_{OHM3S}	$V_{OHM3S} = V_{DD4} - 0.2$ V (V_{DD4} level)		—	—	-4	µA	
	I_{OMH3}	$V_{OMH3} = V_{DD3} + 0.2$ V (V_{DD3} level)		4	—	—	µA	
	I_{OMH3S}	$V_{OMH3S} = V_{DD3} - 0.2$ V (V_{DD3} level)		—	—	-4	µA	
	I_{OML3}	$V_{OML3} = V_{DD2} + 0.2$ V (V_{DD2} level)		4	—	—	µA	
	I_{OML3S}	$V_{OML3S} = V_{DD2} - 0.2$ V (V_{DD2} level)		—	—	-4	µA	
	I_{OLM3}	$V_{OLM3} = V_{DD1} + 0.2$ V (V_{DD1} level)		4	—	—	µA	
	I_{OLM3S}	$V_{OLM3S} = V_{DD1} - 0.2$ V (V_{DD1} level)		—	—	-4	µA	
	I_{OL3}	$V_{OL3} = V_{SS} + 0.2$ V (V_{SS} level)		4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	$V_{OH4R} = V_{DDH} - 0.5$ V (RC oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	-2.5	-1.3	-0.25	mA	
			$V_{DD} = V_{DDH} = 5.0$ V	-3.5	-1.7	-0.5	mA	
	I_{OL4R}	$V_{OL4R} = 0.5$ V (RC oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	0.25	1.5	2.5	mA	
			$V_{DD} = V_{DDH} = 5.0$ V	0.5	1.8	3.5	mA	
	I_{OH4C}	$V_{OH4C} = V_{DDH} - 0.5$ V (crystal oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	-500	-250	-100	µA	
			$V_{DD} = V_{DDH} = 5.0$ V	-800	-350	-200	µA	
	I_{OL4C}	$V_{OL4C} = 0.5$ V (crystal oscillation)	$V_{DD} = V_{DDH} = 3.0$ V	200	500	800	µA	
			$V_{DD} = V_{DDH} = 5.0$ V	400	700	1000	µA	

DC Characteristics (continued)

$(V_{DD} = V_{DDI} = V_{DDH} = AV_{DD} = 3.0 \text{ V}, V_{DD1} = 1.1 \text{ V}, V_{DD2} = 2.2 \text{ V}, V_{DD3} = 3.3 \text{ V}, V_{DD4} = 4.4 \text{ V},$
$V_{DD5} = 5.5 \text{ V}, V_{SS} = AV_{SS} = 0 \text{ V}, Ta = -20 \text{ to} +70°C \text{ unless otherwise specified})$

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Leakage Current (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) (P7.0 to P7.3) (P8.0, P8.1)	I_{OOH}	$V_{OH} = V_{DDI}$		—	—	0.3	µA	2
(P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3) (PF.0 to PF.3)	I_{OOL}	$V_{OL} = V_{SS}$		−0.3	—	—	µA	
Output Current 6 (DACOUT)	I_{OH6}	$V_{OH6} = AV_{DD} - 0.3 \text{ V}$		−2.4	−1.2	−0.6	mA	
	I_{OL6}	$V_{OL6} = 1.5 \text{ V}, AV_{DD} = 3 \text{ V}$		50	100	200	µA	
Output Current 7 (AOUT)	I_{OH7}	$V_{OH7} = AV_{DD} - 0.3 \text{ V}$		−400	−200	−100	µA	
	I_{OL7}	$V_{OL7} = 1.0 \text{ V}$		100	200	400		
Output Current 8 (SP(−), SP(+))	I_{OH8}	$V_{OH8} = AV_{DD} - 0.3 \text{ V}$		−4	−2	−1	mA	
	I_{OL8}	$V_{OL8} = 1.0 \text{ V}$		1	2	4		
Input Current 1 (P0.0 to P0.3) (P8.0, P8.1) (P9.0 to P9.3)	I_{IH1}	$V_{IH1} = V_{DDI}$ (when pulled down)	$V_{DDI} = 3.0 \text{ V}$	30	120	260	µA	3
			$V_{DDI} = 5.0 \text{ V}$	70	350	650	µA	
(PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3)	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	$V_{DDI} = 3.0 \text{ V}$	−260	−120	−30	µA	
(PF.0 to PF.3)			$V_{DDI} = 5.0 \text{ V}$	−600	−250	−70	µA	
	I_{IH1Z}	$V_{IH1} = V_{DDI}$ (in a high impedance state)		0.0	—	1.0	µA	
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)		−1.0	—	0.0	µA	
Input Current 2 (OSC0)	I_{IL2}	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH} = 3.0 \text{ V}$	−350	−170	−30	µA	
			$V_{DD} = V_{DDH} = 5.0 \text{ V}$	−750	−450	−200	µA	
	I_{IH2R}	$V_{IH2R} = V_{DDH}$ (RC oscillation)		0.0	—	1.0	µA	
	I_{IL2R}	$V_{IL2R} = V_{SS}$ (RC oscillation)		−1.0	—	0.0	µA	
	I_{IH2C}	$V_{IH2C} = V_{DDH}$ (crystal oscillation)	$V_{DD} = V_{DDH} = 3.0 \text{ V}$	0.5	2.0	4.0	µA	
			$V_{DD} = V_{DDH} = 5.0 \text{ V}$	3	6	10	µA	
	I_{IL2C}	$V_{IL2C} = V_{SS}$ (crystal oscillation)	$V_{DD} = V_{DDH} = 3.0 \text{ V}$	−4.0	−2.0	−0.5	µA	
			$V_{DD} = V_{DDH} = 5.0 \text{ V}$	−10	−6	−3	µA	
Input Current 3 (RESET)	I_{IH3}	$V_{IH3} = V_{DD}$	$V_{DD} = 3.0 \text{ V}$	150	1100	2400	µA	
			$V_{DD} = 5.0 \text{ V}$	0.5	2.7	5.0	mA	
	I_{IL3}	$V_{IL3} = V_{SS}$		−1.0	—	0.0	µA	
Input Current 4 (TST1, TST2, VTEST)	I_{IH4}	$V_{IH4} = V_{DD}$	$V_{DD} = 3.0 \text{ V}$	0.5	3.0	5.5	mA	
			$V_{DD} = 5.0 \text{ V}$	2.0	6.5	11.0	mA	
	I_{IL4}	$V_{IL4} = V_{SS}$		−1.0	—	0.0	µA	
Input Current 5 (SPEN)	I_{IH5}	$V_{IH5} = V_{DD}$	$V_{DD} = 3.0 \text{ V}$	30	120	260	µA	
			$V_{DD} = 5.0 \text{ V}$	70	350	650		
	I_{IL5}	$V_{IL5} = V_{SS}$		−1.0	—	0.0		

DC Characteristics (continued)

$(V_{DD} = V_{DDI} = V_{DDH} = AV_{DD} = 3.0$ V, $V_{DD1} = 1.1$ V, $V_{DD2} = 2.2$ V, $V_{DD3} = 3.3$ V, $V_{DD4} = 4.4$ V,
$V_{DD5} = 5.5$ V, $V_{SS} = AV_{SS} = 0$ V, Ta = −20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P8.0, P8.1) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3) (PF.0 to PF.3)	V_{IH1}	$V_{DDI} = 3.0$ V	2.4	—	3.0	V	4
		$V_{DDI} = 5.0$ V	4.0	—	5.0	V	
	V_{IL1}	$V_{DDI} = 3.0$ V	0.0	—	0.6	V	
		$V_{DDI} = 5.0$ V	0.0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	$V_{DD} = V_{DDH} = 3.0$ V	2.4	—	3.0	V	
		$V_{DD} = V_{DDH} = 5.0$ V	4.0	—	5.0	V	
	V_{IL2}	$V_{DD} = V_{DDH} = 3.0$ V	0.0	—	0.6	V	
		$V_{DD} = V_{DDH} = 5.0$ V	0.0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2, VTEST, SPEN)	V_{IH3}	$V_{DD} = 3.0$ V	2.4	—	3.0	V	
		$V_{DD} = 5.0$ V	4.0	—	5.0	V	
	V_{IL3}	$V_{DD} = 3.0$ V	0.0	—	0.6	V	
		$V_{DD} = 5.0$ V	0.0	—	1.0	V	
Hysteresis Width 1 (P0.0 to P0.3) (P8.0, P8.1) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3) (PF.0 to PF.3)	ΔV_{T1}	$V_{DDI} = 3.0$ V	0.2	0.5	1.0	V	
		$V_{DDI} = 5.0$ V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2, SPEN)	ΔV_{T2}	$V_{DD} = 3.0$ V	0.2	0.5	1.0	V	
		$V_{DD} = 5.0$ V	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0 to P0.3) (P8.0, P8.1) (P9.0 to P9.3) (PA.0 to PA.3) (PB.0 to PB.3) (PE.0 to PE.3) (PF.0 to PF.3)	C_{IN}	—	—	—	5	pF	—

Measuring circuit 1

C_a, C_b, C_c, C_d, C_e, C_l, C_{12} : 0.1 μF
C_{b12}, C_h : 1 μF
C_G : 15 pF
C_{L0} : 30 pF
C_{L1} : 30 pF
Crystal unit : AT-49 4.096 MHz
(Daishinku Corp.-make)

*1 RC Oscillator

*2 RC Oscillator

Crystal Oscillator

Crystal Oscillator

32.768 kHz
Crystal
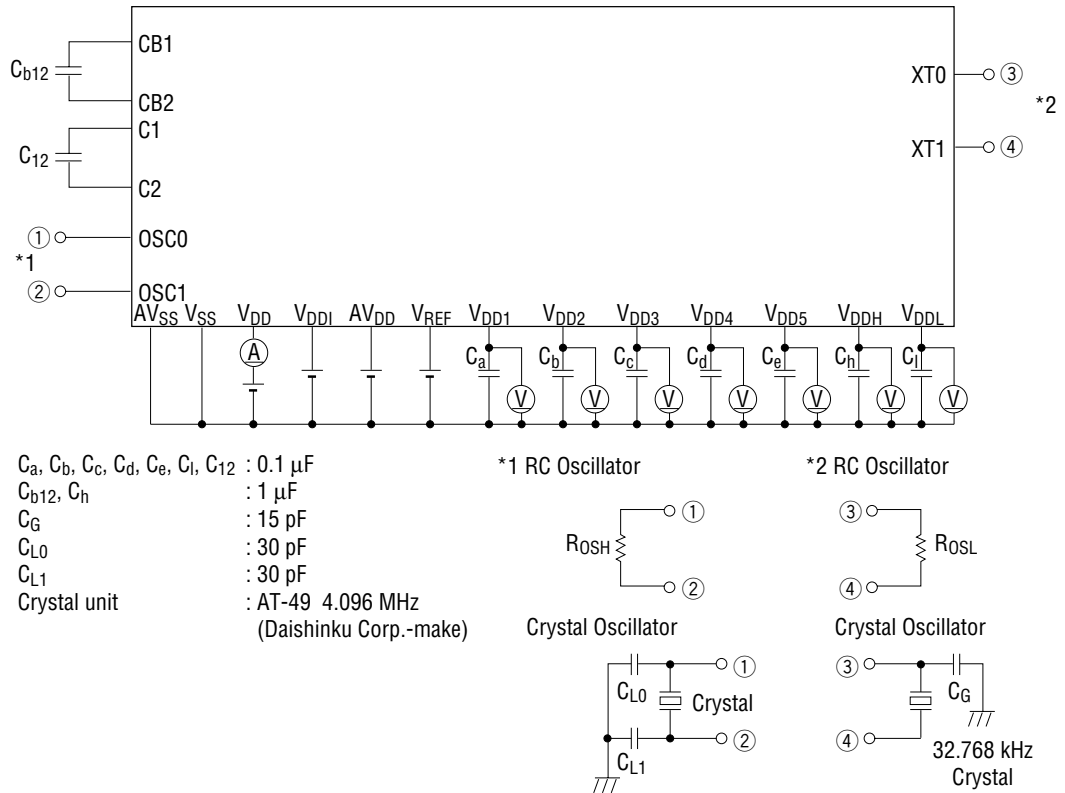
Measuring circuit 2
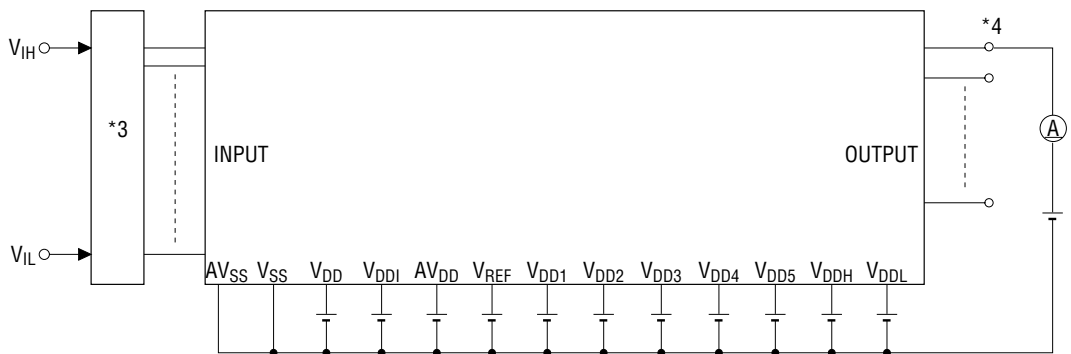
*3 Input logic circuit to determine the specified measuring conditions.
*4 Measured at the specified output pins.

Measuring circuit 3
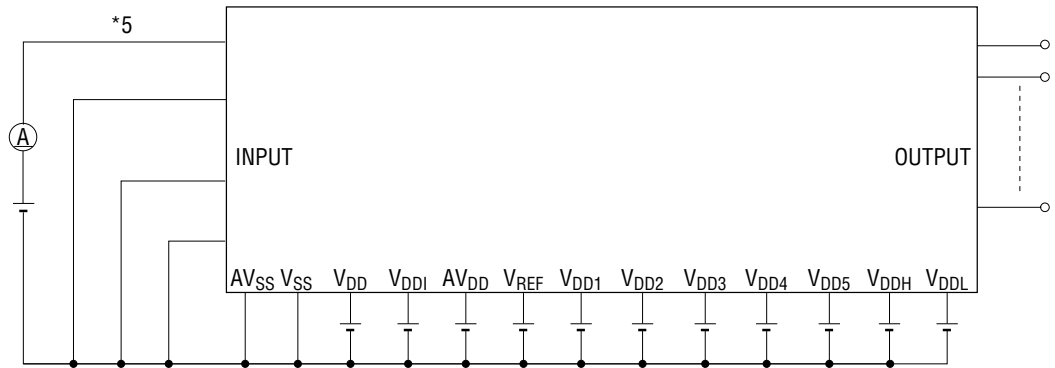
Measuring circuit 4
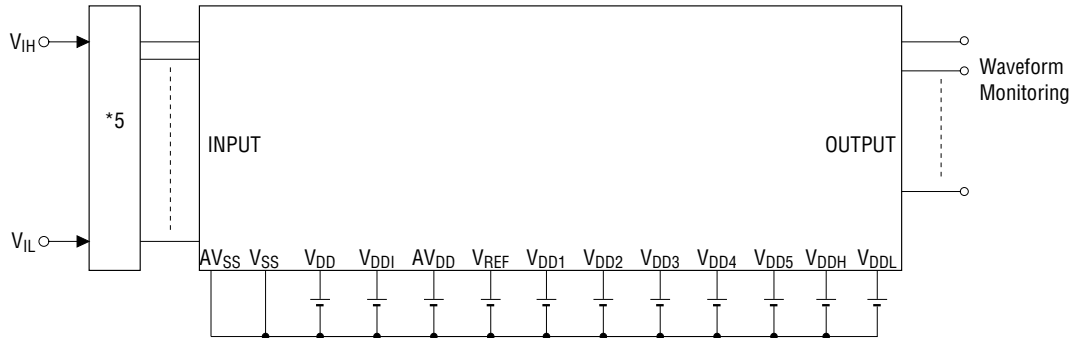
*5 Measured at the specified input pins.

AC Characteristics (Serial Interface, Shift Register) (Target value)

(V_{DD} = AV_{DD} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	µs
SCLK Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
SCLK Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
SCLK Input Cycle Time	t_{CYC}	V_{DDI} = 5 V to V_{DD}	1.8	—	—	µs
SCLK Output Cycle Time	$t_{CYC1(O)}$	CPU in operation state at 32.768 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU in operation at 2 MHz V_{DD} = 2.0 V to 5.5 V	—	0.5	—	µs
SOUT Output Delay Time	t_{DDR}	C_l = 10 pF	—	—	0.4	µs
SIN Input Setup Time	t_{DS}	—	0.5	—	—	µs
SIN Input Hold Time	t_{DH}	—	0.8	—	—	µs

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)
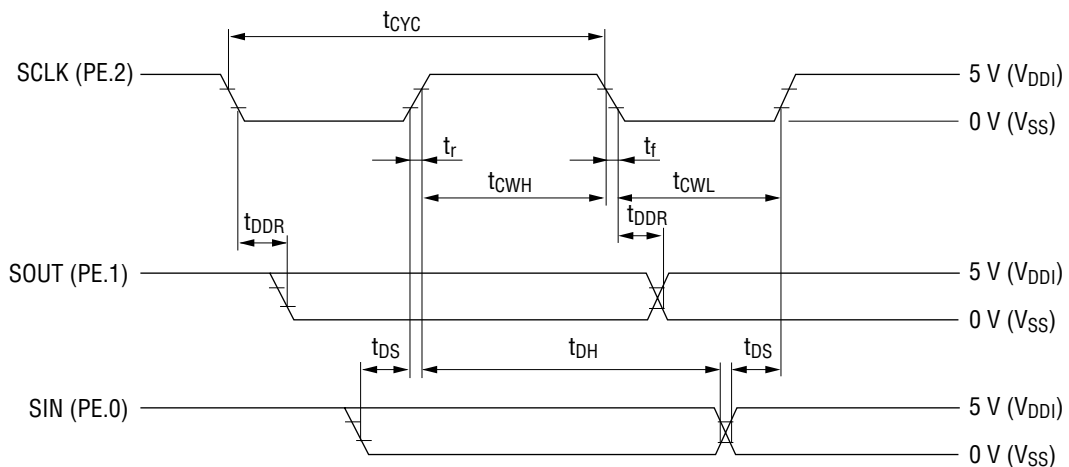
AC Characteristics (External Memory Interface) (Target value)

(V_{DD} = AV_{DD} = 2.0 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Reading from External Memory

   (a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61	—	
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5	
Output Valid Time	t_{OHA}	—	—	—	5	µs
External Memory Output Delay Time	t_{DO}	—	—	—	5	

   (b) When CPU operates at 2 MHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	
Output Valid Time	t_{OHA}	—	—	—	100	ns
External Memory Output Delay Time	t_{DO}	—	—	—	150	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)
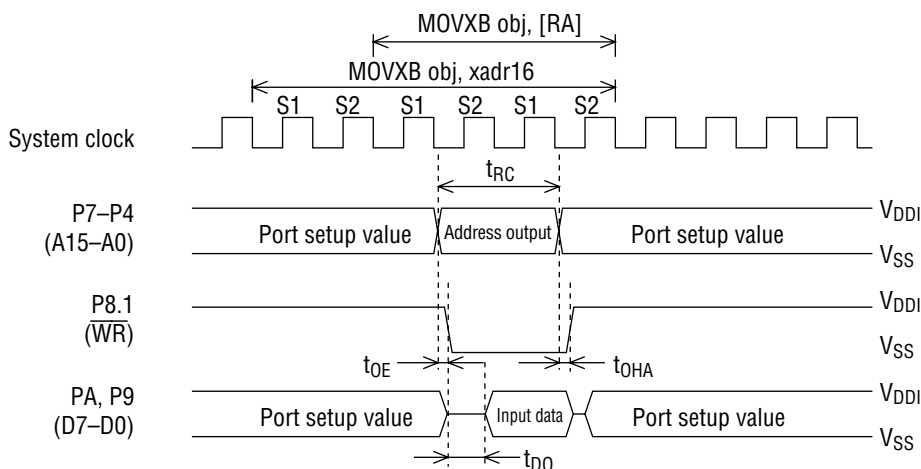
(2) Writing to External Memory

(a) When CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61	—	
Address Setup Time	t_{AS}	—	—	30.5	—	
Write Time	t_W	—	—	15.3	—	
Write Recovery Time	t_{WR}	—	—	15.3	—	μs
Data Setup Time	t_{DS}	—	—	45.8	—	
Data Hold Time	t_{DH}	—	—	15.3	—	

(b) When CPU operates at 2 MHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1	—	—	
Address Setup Time	t_{AS}	—	0.4	—	—	
Write Time	t_W	—	0.2	—	—	
Write Recovery Time	t_{WR}	—	0.2	—	—	μs
Data Setup Time	t_{DS}	—	0.7	—	—	
Data Hold Time	t_{DH}	—	0.2	—	—	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)

Appendix F Instruction List

The format used in the list of instructions is indicated below.

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G

Flags marked with (√) are affected by instruction execution, and those that are not affected with a dash.

Indicates the instruction code content. For a 2-word long instruction, the first row shows the first word, and the second row the second word.

Indicates the number of machine cycles needed to execute the instruction.

Indicates the instruction word length.

Indicates the instruction function.

Indicates the short-form name for the instruction.

Transfer Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOV direct,A	direct←A	1	1	1	1	0	0	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
MOV [HL],A	[HL]←A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	—	—	—
MOV [XY],A	[XY]←A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	—	—	—
MOV E:[HL],A	E:[HL]←A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	—	—	—
MOV E:[XY],A	E:[XY]←A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	—	—	—
MOV [HL+],A	[HL]←A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	—	—	√
MOV [XY+],A	[XY]←A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	—	—	√
MOV E:[HL+],A	E:[HL]←A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	—	—	√
MOV E:[XY+],A	E:[XY]←A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	—	—	√
MOV ¥cur,#i4	cur,A←i4	1	1	0	1	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV [HL],#i4	[HL],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
MOV [XY],#i4	[XY],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
MOV E:[HL],#i4	E:[HL],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV E:[XY],#i4	E:[XY],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
MOV [HL+],#i4	[HL],A←i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
MOV [XY+],#i4	[XY],A←i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
MOV E:[HL+],#i4	E:[HL],A←i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
MOV E:[XY+],#i4	E:[XY],A←i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
MOV A,#i4	A←i4	1	1	0	0	0	0	0	0	0	1	1	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV A,direct	A←direct	1	1	1	1	0	1	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV A,[HL]	A←[HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	√	—	—
MOV A,[XY]	A←[XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	√	—	—
MOV A,E:[HL]	A←E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	√	—	—
MOV A,E:[XY]	A←E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	√	—	—
MOV A,[HL+]	A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	√	—	√
MOV A,[XY+]	A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	√	—	√
MOV A,E:[HL+]	A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	√	—	√
MOV A,E:[XY+]	A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	√	—	√
XCH A,sfr	A↔sfr	1	1	0	0	1	0	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,¥cur	A↔cur	1	1	0	0	1	1	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,[HL]	A↔[HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	—	—	—
XCH A,[XY]	A↔[XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	—	—	—
XCH A,E:[HL]	A↔E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	—	—	—
XCH A,E:[XY]	A↔E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	—	—	—
XCH A,[HL+]	A↔[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	—	—	√
XCH A,[XY+]	A↔[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	—	—	√
XCH A,E:[HL+]	A↔E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	—	—	√
XCH A,E:[XY+]	A↔E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	—	—	√

Rotate Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ROL sfr	$C\leftarrow\{_3sfr_0\}\leftarrow C, A\leftarrow sfr$	1	1	0	0	1	0	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL ¥cur	$C\leftarrow\{_3cur_0\}\leftarrow C, A\leftarrow cur$	1	1	0	0	1	1	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL [HL]	$C\leftarrow\{_3[HL]_0\}\leftarrow C, A\leftarrow[HL]$	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	√	√	—
ROL [XY]	$C\leftarrow\{_3[XY]_0\}\leftarrow C, A\leftarrow[XY]$	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	√	√	—
ROL E:[HL]	$C\leftarrow\{_3E:[HL]_0\}\leftarrow C, A\leftarrow E:[HL]$	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	√	√	—
ROL E:[XY]	$C\leftarrow\{_3E:[XY]_0\}\leftarrow C, A\leftarrow E:[XY]$	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	√	√	—
ROL [HL+]	$C\leftarrow\{_3[HL]_0\}\leftarrow C, A\leftarrow[HL], HL\leftarrow HL+1$	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	√	√	√
ROL [XY+]	$C\leftarrow\{_3[XY]_0\}\leftarrow C, A\leftarrow[XY], XY\leftarrow XY+1$	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	√	√	√
ROL E:[HL+]	$C\leftarrow\{_3E:[HL]_0\}\leftarrow C, A\leftarrow E:[HL], HL\leftarrow HL+1$	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	√	√	√
ROL E:[XY+]	$C\leftarrow\{_3E:[XY]_0\}\leftarrow C, A\leftarrow E:[XY], XY\leftarrow XY+1$	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	√	√	√
ROR sfr	$C\rightarrow\{_3sfr_0\}\rightarrow C, A\leftarrow sfr$	1	1	0	0	1	0	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR ¥cur	$C\rightarrow\{_3cur_0\}\rightarrow C, A\leftarrow cur$	1	1	0	0	1	1	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR [HL]	$C\rightarrow\{_3[HL]_0\}\rightarrow C, A\leftarrow[HL]$	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	√	√	—
ROR [XY]	$C\rightarrow\{_3[XY]_0\}\rightarrow C, A\leftarrow[XY]$	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	√	—
ROR E:[HL]	$C\rightarrow\{_3E:[HL]_0\}\rightarrow C, A\leftarrow E:[HL]$	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	√	√	—
ROR E:[XY]	$C\rightarrow\{_3E:[XY]_0\}\rightarrow C, A\leftarrow E:[XY]$	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	√	√	—
ROR [HL+]	$C\rightarrow\{_3[HL]_0\}\rightarrow C, A\leftarrow[HL], HL\leftarrow HL+1$	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	√	√	√
ROR [XY+]	$C\rightarrow\{_3[XY]_0\}\rightarrow C, A\leftarrow[XY], XY\leftarrow XY+1$	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	√	√	√
ROR E:[HL+]	$C\rightarrow\{_3E:[HL]_0\}\rightarrow C, A\leftarrow E:[HL], HL\leftarrow HL+1$	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	√	√	√
ROR E:[XY+]	$C\rightarrow\{_3E:[XY]_0\}\rightarrow C, A\leftarrow E:[XY], XY\leftarrow XY+1$	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	√	√	√

Increment/Decrement Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
INC sfr	sfr,A←sfr+1	1	1	0	0	1	0	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC ¥cur	cur,A←cur+1	1	1	0	0	1	1	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC [HL]	[HL],A←[HL]+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	√	√	—
INC [XY]	[XY],A←[XY]+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	√	√	—
INC E:[HL]	E:[HL],A←E:[HL]+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	√	√	—
INC E:[XY]	E:[XY],A←E:[XY]+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	√	√	—
INC [HL+]	[HL],A←[HL]+1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	√	√	√
INC [XY+]	[XY],A←[XY]+1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	√	√	√
INC E:[HL+]	E:[HL],A←E:[HL]+1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	√	√	√
INC E:[XY+]	E:[XY],A←E:[XY]+1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	√	√	√
DEC sfr	sfr,A←sfr−1	1	1	0	0	1	0	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC ¥cur	cur,A←cur−1	1	1	0	0	1	1	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC [HL]	[HL],A←[HL]−1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	√	√	—
DEC [XY]	[XY],A←[XY]−1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	√	√	—
DEC E:[HL]	E:[HL],A←E:[HL]−1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	√	√	—
DEC E:[XY]	E:[XY],A←E:[XY]−1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	√	√	—
DEC [HL+]	[HL],A←[HL]−1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	√	√	√
DEC [XY+]	[XY],A←[XY]−1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	√	√	√
DEC E:[HL+]	E:[HL],A←E:[HL]−1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	√	√	√
DEC E:[XY+]	E:[XY],A←E:[XY]−1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	√	√	√

Arithmetic Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADD sfr,A	sfr,A←sfr+A	1	1	0	0	1	0	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD ¥cur,A	cur,A←cur+A	1	1	0	0	1	1	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],A	[HL],A←[HL]+A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	√	√	—
ADD [XY],A	[XY],A←[XY]+A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0	√	√	—
ADD E:[HL],A	E:[HL],A←E:[HL]+A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	√	√	—
ADD E:[XY],A	E:[XY],A←E:[XY]+A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	√	√	—
ADD [HL+],A	[HL],A←[HL]+A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	√	√	√
ADD [XY+],A	[XY],A←[XY]+A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	0	√	√	√
ADD E:[HL+],A	E:[HL],A←E:[HL]+A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	√	√	√
ADD E:[XY+],A	E:[XY],A←E:[XY]+A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	√	√	√
ADD ¥cur,#i4	cur,A←cur+i4	1	1	1	0	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],#i4	[HL],A←[HL]+i4	1	1	0	0	0	0	0	0	0	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
ADD [XY],#i4	[XY],A←[XY]+i4	1	1	0	0	0	0	0	0	0	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
ADD E:[HL],#i4	E:[HL],A←E:[HL]+i4	1	1	0	0	0	0	0	0	0	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
ADD E:[XY],#i4	E:[XY],A←E:[XY]+i4	1	1	0	0	0	0	0	0	0	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
ADD [HL+],#i4	[HL],A←[HL]+i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
ADD [XY+],#i4	[XY],A←[XY]+i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
ADD E:[HL+],#i4	E:[HL],A←E:[HL]+i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
ADD E:[XY+],#i4	E:[XY],A←E:[XY]+i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
ADC sfr,A	sfr,A←sfr+A+C	1	1	0	0	1	0	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC ¥cur,A	cur,A←cur+A+C	1	1	0	0	1	1	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC [HL],A	[HL],A←[HL]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	√	√	—
ADC [XY],A	[XY],A←[XY]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	√	√	—
ADC E:[HL],A	E:[HL],A←E:[HL]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	√	√	—
ADC E:[XY],A	E:[XY],A←E:[XY]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1	√	√	—
ADC [HL+],A	[HL],A←[HL]+A+C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	1	√	√	√
ADC [XY+],A	[XY],A←[XY]+A+C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	√	√	√
ADC E:[HL+],A	E:[HL],A←E:[HL]+A+C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1	√	√	√
ADC E:[XY+],A	E:[XY],A←E:[XY]+A+C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
				INSTRUCTION CODE																FLAG		
ADCD sfr,A	sfr,A←decimal adjustment {sfr+A+C}	1	1	0	0	1	0	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD ¥cur,A	cur,A←decimal adjustment {cur+A+C}	1	1	0	0	1	1	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD [HL],A	[HL],A←decimal adjustment {[HL]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	√	√	—
ADCD [XY],A	[XY],A←decimal adjustment {[XY]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	√	√	—
ADCD E:[HL],A	E:[HL],A←decimal adjustment {E:[HL]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	√	√	—
ADCD E:[XY],A	E:[XY],A←decimal adjustment {E:[XY]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	√	√	—
ADCD [HL+],A	[HL],A←decimal adjustment {[HL]+A+C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	√	√	√
ADCD [XY+],A	[XY],A←decimal adjustment {[XY]+A+C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	√	√	√
ADCD E:[HL+],A	E:[HL],A←decimal adjustment {E:[HL]+A+C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	√	√	√
ADCD E:[XY+],A	E:[XY],A←decimal adjustment {E:[XY]+A+C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	√	√	√
ADCJ ¥cur,n	cur,A←n-ary adjustment {cur+C}	1	1	0	0	0	1	0	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCJ [HL],n	[HL],A←n-ary adjustment {[HL]+C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	n_2	n_1	n_0	√	√	—
ADCJ [XY],n	[XY],A←n-ary adjustment {[XY]+C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	0	n_2	n_1	n_0	√	√	—
ADCJ E:[HL],n	E:[HL],A←n-ary adjustment {E:[HL]+C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	n_2	n_1	n_0	√	√	—
ADCJ E:[XY],n	E:[XY],A←n-ary adjustment {E:[XY]+C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	n_2	n_1	n_0	√	√	—
ADCJ [HL+],n	[HL],A←n-ary adjustment {[HL]+C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0	n_2	n_1	n_0	√	√	√
ADCJ [XY+],n	[XY],A←n-ary adjustment {[XY]+C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	n_2	n_1	n_0	√	√	√
ADCJ E:[HL+],n	E:[HL],A←n-ary adjustment {E:[HL]+C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	n_2	n_1	n_0	√	√	√
ADCJ E:[XY+],n	E:[XY],A←n-ary adjustment {E:[XY]+C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	n_2	n_1	n_0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SUB sfr,A	sfr,A←sfr–A	1	1	0	0	1	0	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB ¥cur,A	cur,A←cur–A	1	1	0	0	1	1	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],A	[HL],A←[HL]–A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	√	√	—
SUB [XY],A	[XY],A←[XY]–A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1	√	√	—
SUB E:[HL],A	E:[HL],A←E:[HL]–A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	√	√	—
SUB E:[XY],A	E:[XY],A←E:[XY]–A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	√	√	—
SUB [HL+],A	[HL],A←[HL]–A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	√	√	√
SUB [XY+],A	[XY],A←[XY]–A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	1	√	√	√
SUB E:[HL+],A	E:[HL],A←E:[HL]–A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	√	√	√
SUB E:[XY+],A	E:[XY],A←E:[XY]–A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	√	√	√
SUB ¥cur,#i4	cur,A←cur–i4	1	1	1	0	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],#i4	[HL],A←[HL]–i4	1	1	0	0	0	0	0	0	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
SUB [XY],#i4	[XY],A←[XY]–i4	1	1	0	0	0	0	0	0	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
SUB E:[HL],#i4	E:[HL],A←E:[HL]–i4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
SUB E:[XY],#i4	E:[XY],A←E:[XY]–i4	1	1	0	0	0	0	0	0	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
SUB [HL+],#i4	[HL],A←[HL]–i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
SUB [XY+],#i4	[XY],A←[XY]–i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
SUB E:[HL+],#i4	E:[HL],A←E:[HL]–i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
SUB E:[XY+],#i4	E:[XY],A←E:[XY]–i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
SBC sfr,A	sfr,A←sfr–A–C	1	1	0	0	1	0	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC ¥cur,A	cur,A←cur–A–C	1	1	0	0	1	1	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC [HL],A	[HL],A←[HL]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	√	√	—
SBC [XY],A	[XY],A←[XY]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	0	√	√	—
SBC E:[HL],A	E:[HL],A←E:[HL]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	√	√	—
SBC E:[XY],A	E:[XY],A←E:[XY]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	0	√	√	—
SBC [HL+],A	[HL],A←[HL]–A–C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	0	√	√	√
SBC [XY+],A	[XY],A←[XY]–A–C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	√	√	√
SBC E:[HL+],A	E:[HL],A←E:[HL]–A–C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	√	√	√
SBC E:[XY+],A	E:[XY],A←E:[XY]–A–C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
									INSTRUCTION CODE											FLAG		
SBCD sfr,A	sfr,A←decimal adjustment {sfr−A−C}	1	1	0	0	1	0	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD ¥cur,A	cur,A←decimal adjustment {cur−A−C}	1	1	0	0	1	1	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD [HL],A	[HL],A←decimal adjustment {[HL]−A−C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	√	√	—
SBCD [XY],A	[XY],A←decimal adjustment {[XY]−A−C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	√	√	—
SBCD E:[HL],A	E:[HL],A←decimal adjustment {E:[HL]−A−C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	√	√	—
SBCD E:[XY],A	E:[XY],A←decimal adjustment {E:[XY]−A−C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	√	√	—
SBCD [HL+],A	[HL],A←decimal adjustment {[HL]−A−C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1	√	√	√
SBCD [XY+],A	[XY],A←decimal adjustment {[XY]−A−C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	√	√	√
SBCD E:[HL+],A	E:[HL],A←decimal adjustment {E:[HL]−A−C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	√	√	√
SBCD E:[XY+],A	E:[XY],A←decimal adjustment {E:[XY]−A−C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1	√	√	√
SBCJ ¥cur,n	cur,A←n-ary adjustment {cur−C}	1	1	0	0	0	1	1	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCJ [HL],n	[HL],A←n-ary adjustment {[HL]−C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	n_2	n_1	n_0	√	√	—
SBCJ [XY],n	[XY],A←n-ary adjustment {[XY]−C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	n_2	n_1	n_0	√	√	—
SBCJ E:[HL],n	E:[HL],A←n-ary adjustment {E:[HL]−C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	n_2	n_1	n_0	√	√	—
SBCJ E:[XY],n	E:[XY],A←n-ary adjustment {E:[XY]−C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	n_2	n_1	n_0	√	√	—
SBCJ [HL+],n	[HL],A←n-ary adjustment {[HL]−C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	1	n_2	n_1	n_0	√	√	√
SBCJ [XY+],n	[XY],A←n-ary adjustment {[XY]−C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1	n_2	n_1	n_0	√	√	√
SBCJ E:[HL+],n	E:[HL],A←n-ary adjustment {E:[HL]−C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	n_2	n_1	n_0	√	√	√
SBCJ E:[XY+],n	E:[XY],A←n-ary adjustment {E:[XY]−C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	n_2	n_1	n_0	√	√	√

Compare Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
							INSTRUCTION CODE													FLAG		
CMP sfr,A	sfr–A	1	1	0	0	1	0	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP ¥cur,A	cur–A	1	1	0	0	1	1	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],A	[HL]–A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	√	√	—
CMP [XY],A	[XY]–A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	√	√	—
CMP E:[HL],A	E:[HL]–A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	√	√	—
CMP E:[XY],A	E:[XY]–A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	√	√	—
CMP [HL+],A	[HL]–A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	√	√	√
CMP [XY+],A	[XY]–A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	√	√	√
CMP E:[HL+],A	E:[HL]–A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	√	√	√
CMP E:[XY+],A	E:[XY]–A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	√	√	√
CMP ¥cur,#i4	cur–i4	1	1	1	0	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],#i4	[HL]–i4	1	1	0	0	0	0	0	1	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
CMP [XY],#i4	[XY]–i4	1	1	0	0	0	0	0	1	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
CMP E:[HL],#i4	E:[HL]–i4	1	1	0	0	0	0	0	1	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
CMP E:[XY],#i4	E:[XY]–i4	1	1	0	0	0	0	0	1	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
CMP [HL+],#i4	[HL]–i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
CMP [XY+],#i4	[XY]–i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
CMP E:[HL+],#i4	E:[HL]–i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
CMP E:[XY+],#i4	E:[XY]–i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√

Logic Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
AND sfr,A	sfr,A←sfr∧A	1	1	0	0	1	0	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND ¥cur,A	cur,A←cur∧A	1	1	0	0	1	1	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],A	[HL],A←[HL]∧A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	√	—	—
AND [XY],A	[XY],A←[XY]∧A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	√	—	—
AND E:[HL],A	E:[HL],A←E:[HL]∧A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	√	—	—
AND E:[XY],A	E:[XY],A←E:[XY]∧A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	√	—	—
AND [HL+],A	[HL],A←[HL]∧A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	1	√	—	√
AND [XY+],A	[XY],A←[XY]∧A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	√	—	√
AND E:[HL+],A	E:[HL],A←E:[HL]∧A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	√	—	√
AND E:[XY+],A	E:[XY],A←E:[XY]∧A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	√	—	√
AND ¥cur,#i4	cur,A←cur∧i4	1	1	0	1	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],#i4	[HL],A←[HL]∧i4	1	1	0	0	0	0	0	1	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
AND [XY],#i4	[XY],A←[XY]∧i4	1	1	0	0	0	0	0	1	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
AND E:[HL],#i4	E:[HL],A←E:[HL]∧i4	1	1	0	0	0	0	0	1	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
AND E:[XY],#i4	E:[XY],A←E:[XY]∧i4	1	1	0	0	0	0	0	1	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
AND [HL+],#i4	[HL],A←[HL]∧i4, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
AND [XY+],#i4	[XY],A←[XY]∧i4, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
AND E:[HL+],#i4	E:[HL],A←E:[HL]∧i4, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
AND E:[XY+],#i4	E:[XY],A←E:[XY]∧i4, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
OR sfr,A	sfr,A←sfr∨A	1	1	0	0	1	0	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR ¥cur,A	cur,A←cur∨A	1	1	0	0	1	1	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],A	[HL],A←[HL]∨A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	√	—	—
OR [XY],A	[XY],A←[XY]∨A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	√	—	—
OR E:[HL],A	E:[HL],A←E:[HL]∨A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	√	—	—
OR E:[XY],A	E:[XY],A←E:[XY]∨A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	√	—	—
OR [HL+],A	[HL],A←[HL]∨A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	√	—	√
OR [XY+],A	[XY],A←[XY]∨A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	0	√	—	√
OR E:[HL+],A	E:[HL],A←E:[HL]∨A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	√	—	√
OR E:[XY+],A	E:[XY],A←E:[XY]∨A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	√	—	√

Logic Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
OR ¥cur,#i4	cur,A←cur∨i4	1	1	0	1	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],#i4	[HL],A←[HL]∨i4	1	1	0	0	0	0	0	0	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
OR [XY],#i4	[XY],A←[XY]∨i4	1	1	0	0	0	0	0	0	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
OR E:[HL],#i4	E:[HL],A←E:[HL]∨i4	1	1	0	0	0	0	0	0	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
OR E:[XY],#i4	E:[XY],A←E:[XY]∨i4	1	1	0	0	0	0	0	0	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
OR [HL+],#i4	[HL],A←[HL]∨i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
OR [XY+],#i4	[XY],A←[XY]∨i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
OR E:[HL+],#i4	E:[HL],A←E:[HL]∨i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
OR E:[XY+],#i4	E:[XY],A←E:[XY]∨i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
XOR sfr,A	sfr,A←sfr∀A	1	1	0	0	1	0	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR ¥cur,A	cur,A←cur∀A	1	1	0	0	1	1	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],A	[HL],A←[HL]∀A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	√	—	—
XOR [XY],A	[XY],A←[XY]∀A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	√	—	—
XOR E:[HL],A	E:[HL],A←E:[HL]∀A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	√	—	—
XOR E:[XY],A	E:[XY],A←E:[XY]∀A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	√	—	—
XOR [HL+],A	[HL],A←[HL]∀A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	√	—	√
XOR [XY+],A	[XY],A←[XY]∀A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	√	—	√
XOR E:[HL+],A	E:[HL],A←E:[HL]∀A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	√	—	√
XOR E:[XY+],A	E:[XY],A←E:[XY]∀A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	√	—	√
XOR ¥cur,#i4	cur,A←cur∀i4	1	1	0	1	1	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],#i4	[HL],A←[HL]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
XOR [XY],#i4	[XY],A←[XY]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
XOR E:[HL],#i4	E:[HL],A←E:[HL]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
XOR E:[XY],#i4	E:[XY],A←E:[XY]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
XOR [HL+],#i4	[HL],A←[HL]∀i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
XOR [XY+],#i4	[XY],A←[XY]∀i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
XOR E:[HL+],#i4	E:[HL],A←E:[HL]∀i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
XOR E:[XY+],#i4	E:[XY],A←E:[XY]∀i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√

Mask Operation Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
																				FLAG		
MTST sfr,A	Testing of all bits in sfr not masked by A	1	1	0	0	1	0	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST ¥cur,A	Testing of all bits in cur not masked by A	1	1	0	0	1	1	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],A	Testing of all bits in [HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	√	—	—
MTST [XY],A	Testing of all bits in [XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	√	—	—
MTST E:[HL],A	Testing of all bits in E:[HL]not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	√	—	—
MTST E:[XY],A	Testing of all bits in E:[XY]not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	√	—	—
MTST [HL+],A	Testing of all bits in [HL] not masked by A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	√	—	√
MTST [XY+],A	Testing of all bits in [XY] not masked by A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	1	√	—	√
MTST E:[HL+],A	Testing of all bits in E:[HL] not masked by A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	√	—	√
MTST E:[XY+],A	Testing of all bits in E:[XY] not masked by A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	√	—	√
MTST ¥cur,#m	Testing of bits in cur not masked by #m	1	1	1	0	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],#m	Testing of all bits in [HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	0	m_3	m_2	m_1	m_0	√	—	—
MTST [XY],#m	Testing of all bits in [XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	1	m_3	m_2	m_1	m_0	√	—	—
MTST E:[HL],#m	Testing of all bits in E:[HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	0	m_3	m_2	m_1	m_0	√	—	—
MTST E:[XY],#m	Testing of all bits in E:[XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	1	m_3	m_2	m_1	m_0	√	—	—
MTST [HL+],#m	Testing of all bits in [HL] not masked by #m, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	m_3	m_2	m_1	m_0	√	—	√
MTST [XY+],#m	Testing of all bits in [XY] not masked by #m, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	m_3	m_2	m_1	m_0	√	—	√
MTST E:[HL+], #m	Testing of all bits in E:[HL] not masked by #m, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	m_3	m_2	m_1	m_0	√	—	√
MTST E:[XY+], #m	Testing of all bits in E:[XY] not masked by #m, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
							INSTRUCTION CODE													FLAG		
MCLR ¥cur,#m	Clearing of all bits in cur not masked by #m, A←cur	1	1	0	1	0	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MCLR [HL],#m	Clearing of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MCLR [XY],#m	Clearing of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[HL],#m	Clearing of all bits in E:[HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[XY],#m	Clearing of all bits in E:[XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MCLR [HL+],#m	Clearing of all bits in [HL] not masked by #m,A←[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MCLR [XY+],#m	Clearing of all bits in [XY] not masked by #m,A←[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[HL+], #m	Clearing of all bits in E:[HL] not masked by #m,A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[XY+], #m	Clearing of all bits in E:[XY] not masked by #m,A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
									INSTRUCTION CODE												FLAG	
MSET ¥cur,#m	Setting of all bits in cur not masked by #m, A←cur	1	1	0	1	1	0	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MSET [HL],#m	Setting of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MSET [XY],#m	Setting of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MSET E:[HL],#m	Setting of all bits in E: [HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MSET E:[XY],#m	Setting of all bits in E: [XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MSET [HL+],#m	Setting of all bits in [HL] not masked by #m, A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MSET [XY+],#m	Setting of all bits in [XY] not masked by #m, A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MSET E:[HL+], #m	Setting of all bits in E: [HL] not masked by #m, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MSET E:[XY+], #m	Setting of all bits in E: [XY] not masked by #m, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
								INSTRUCTION CODE												FLAG		
MNOT ¥cur,#m	Inverting of all bits in cur not masked by #m, A←cur	1	1	0	1	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MNOT [HL],#m	Inverting of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MNOT [XY],#m	Inverting of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[HL],#m	Inverting of all bits in E:[HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[XY],#m	Inverting of all bits in E:[XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MNOT [HL+],#m	Inverting of all bits in [HL] not masked by #m, A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MNOT [XY+],#m	Inverting of all bits in [XY] not masked by #m, A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[HL+], #m	Inverting of all bits in E:[HL] not masked by #m, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[XY+], #m	Inverting of all bits in E:[XY] not masked by #m, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Bit Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BTST ¥cur.n	Bit testing of cur.n	1	1	1	0	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BTST [HL].n	Bit testing of [HL].n	1	1	0	0	0	0	0	1	0	0	1	0	1	0	n_3	n_2	n_1	n_0	√	—	—
BTST [XY].n	Bit testing of [XY].n	1	1	0	0	0	0	0	1	0	0	1	0	1	1	n_3	n_2	n_1	n_0	√	—	—
BTST E:[HL].n	Bit testing of E:[HL].n	1	1	0	0	0	0	0	1	0	0	1	0	0	0	n_3	n_2	n_1	n_0	√	—	—
BTST E:[XY].n	Bit testing of E:[XY].n	1	1	0	0	0	0	0	1	0	0	1	0	0	1	n_3	n_2	n_1	n_0	√	—	—
BTST [HL+].n	Bit testing of [HL].n, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	n_3	n_2	n_1	n_0	√	—	√
BTST [XY+].n	Bit testing of [XY].n, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	n_3	n_2	n_1	n_0	√	—	√
BTST E:[HL+].n	Bit testing of E:[HL].n, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	n_3	n_2	n_1	n_0	√	—	√
BTST E:[XY+].n	Bit testing of E:[XY].n, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	n_3	n_2	n_1	n_0	√	—	√
BCLR ¥cur.n	cur.n←0,A←cur	1	1	0	1	0	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BCLR [HL].n	[HL].n←0,A←[HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BCLR [XY].n	[XY].n←0,A←[XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[HL].n	E:[HL].n←0,A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[XY].n	E:[XY].n←0,A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BCLR [HL+].n	[HL].n←0,A←[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BCLR [XY+].n	[XY].n←0,A←[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[HL+].n	E:[HL].n←0,A←E:[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[XY+].n	E:[XY].n←0,A←E:[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√
BSET ¥cur.n	cur.n←1,A←cur	1	1	0	1	1	0	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BSET [HL].n	[HL].n←1,A←[HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BSET [XY].n	[XY].n←1,A←[XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BSET E:[HL].n	E:[HL].n←1,A←E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BSET E:[XY].n	E:[XY].n←1,A←E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BSET [HL+].n	[HL].n←1,A←[HL], HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BSET [XY+].n	[XY].n←1,A←[XY], XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BSET E:[HL+].n	E:[HL].n←1,A←E:[HL], HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BSET E:[XY+].n	E:[XY].n←1,A←E:[XY], XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

Bit Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BNOT ¥cur.n	cur.n←$\overline{\text{cur.n}}$,A←cur	1	1	0	1	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BNOT [HL].n	[HL].n←$\overline{\text{[HL].n}}$,A←[HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BNOT [XY].n	[XY].n←$\overline{\text{[XY].n}}$,A←[XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[HL].n	E:[HL].n←$\overline{\text{E:[HL].n}}$,A←E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[XY].n	E:[XY].n←$\overline{\text{E:[XY].n}}$,A←E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BNOT [HL+].n	[HL].n←$\overline{\text{[HL].n}}$,A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BNOT [XY+].n	[XY].n←$\overline{\text{[XY].n}}$,A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[HL+].n	E:[HL].n←$\overline{\text{E:[HL].n}}$,A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[XY+].n	E:[XY].n←$\overline{\text{E:[XY].n}}$,A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

ROM Table Reference Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVHB [HL], [RA]	[HL],[HL+1]←(RA)$_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	—	—	—
MOVHB [XY], [RA]	[XY],[XY+1]←(RA)$_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	—	—	—
MOVHB E:[HL], [RA]	E:[HL],E:[HL+1]←(RA)$_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	—	—	—
MOVHB E:[XY], [RA]	E:[XY],E:[XY+1]←(RA)$_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	—	—	—
MOVHB [HL+], [RA]	[HL],[HL+1]←(RA)$_{15-8}$, HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	—	—	√
MOVHB [XY+], [RA]	[XY],[XY+1]←(RA)$_{15-8}$, XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	—	—	√
MOVHB E:[HL+], [RA]	E:[HL],E:[HL+1]←(RA)$_{15-8}$,HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	—	—	√
MOVHB E:[XY+], [RA]	E:[XY],E:[XY+1]←(RA)$_{15-8}$,XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	—	—	√
MOVHB [HL], cadr16	[HL],[HL+1]←(cadr16)$_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY], cadr16	[XY],[XY+1]←(cadr16)$_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL], cadr16	E:[HL],E:[HL+1]←(cadr16)$_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY], cadr16	E:[XY],E:[XY+1]←(cadr16)$_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [HL+], cadr16	[HL],[HL+1]←(cadr16)$_{15-8}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY+], cadr16	[XY],[XY+1]←(cadr16)$_{15-8}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL+], cadr16	E:[HL],E:[HL+1]←(cadr16)$_{15-8}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY+], cadr16	E:[XY],E:[XY+1]←(cadr16)$_{15-8}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

ROM Table Reference Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVLB [HL], [RA]	$[HL],[HL+1]\leftarrow(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	1	—	—	—
MOVLB [XY], [RA]	$[XY],[XY+1]\leftarrow(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	—	—	—
MOVLB E:[HL], [RA]	$E{:}[HL],E{:}[HL+1]\leftarrow (RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	—	—	—
MOVLB E:[XY], [RA]	$E{:}[XY],E{:}[XY+1]\leftarrow (RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	—	—	—
MOVLB [HL+], [RA]	$[HL],[HL+1]\leftarrow(RA)_{7-0},$ $HL\leftarrow HL+2$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	—	—	√
MOVLB [XY+], [RA]	$[XY],[XY+1]\leftarrow(RA)_{7-0},$ $XY\leftarrow XY+2$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	1	—	—	√
MOVLB E:[HL+], [RA]	$E{:}[HL],E{:}[HL+1]\leftarrow (RA)_{7-0},HL\leftarrow HL+2$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	—	—	√
MOVLB E:[XY+], [RA]	$E{:}[XY],E{:}[XY+1]\leftarrow (RA)_{7-0},XY\leftarrow XY+2$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	—	—	√
MOVLB [HL], cadr16	$[HL],[HL+1]\leftarrow (cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY], cadr16	$[XY],[XY+1]\leftarrow (cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL], cadr16	$E{:}[HL],E{:}[HL+1]\leftarrow (cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY], cadr16	$E{:}[XY],E{:}[XY+1]\leftarrow (cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [HL+], cadr16	$[HL],[HL+1]\leftarrow (cadr16)_{7-0},HL\leftarrow HL+2$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY+], cadr16	$[XY],[XY+1]\leftarrow (cadr16)_{7-0},XY\leftarrow XY+2$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL+], cadr16	$E{:}[HL],E{:}[HL+1]\leftarrow (cadr16)_{7-0},HL\leftarrow HL+2$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY+], cadr16	$E{:}[XY],E{:}[XY+1]\leftarrow (cadr16)_{7-0},XY\leftarrow XY+2$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

External Memory Transfer Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
				INSTRUCTION CODE																FLAG		
MOVXB [HL],[RA]	[HL],[HL+1]←(RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0	—	—	—
MOVXB [XY],[RA]	[XY],[XY+1]←(RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	0	—	—	—
MOVXB E:[HL],[RA]	E:[HL],E:[HL+1]←(RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	—	—	—
MOVXB E:[XY],[RA]	E:[XY],E:[XY+1]←(RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	0	—	—	—
MOVXB [HL+],[RA]	[HL],[HL+1]←(RA),HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	—	—	√
MOVXB [XY+],[RA]	[XY],[XY+1]←(RA),XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	—	—	√
MOVXB E:[HL+],[RA]	E:[HL],E:[HL+1]←(RA),HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	—	—	√
MOVXB E:[XY+],[RA]	E:[XY],E:[XY+1]←(RA),XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	0	—	—	√
MOVXB [RA],[HL]	(RA)←[HL],[HL+1]	1	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	—	—	—
MOVXB [RA],[XY]	(RA)←[XY],[XY+1]	1	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	—	—	—
MOVXB [RA],E:[HL]	(RA)←E:[HL],E:[HL+1]	1	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	—	—	—
MOVXB [RA],E:[XY]	(RA)←E:[XY],E:[XY+1]	1	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1	—	—	—
MOVXB [RA],[HL+]	(RA)←[HL],[HL+1],HL←HL+2	1	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	—	—	√
MOVXB [RA],[XY+]	(RA)←[XY],[XY+1],XY←XY+2	1	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	—	—	√
MOVXB [RA],E:[HL+]	(RA)←E:[HL],E:[HL+1],HL←HL+2	1	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	—	—	√
MOVXB [RA],E:[XY+]	(RA)←E:[XY],E:[XY+1],XY←XY+2	1	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	—	—	√

External Memory Transfer Instructions (continued)

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVXB [HL], xadr16	[HL],[HL+1]←(xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY], xadr16	[XY],[XY+1]←(xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL], xadr16	E:[HL],E:[HL+1]←(xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY], xadr16	E:[XY],E:[XY+1]←(xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [HL+], xadr16	[HL],[HL+1]←(xadr16),HL←HL+2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY+], xadr16	[XY],[XY+1]←(xadr16),XY←XY+2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL+], xadr16	E:[HL],E:[HL+1]←(xadr16),HL←HL+2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY+], xadr16	E:[XY],E:[XY+1]←(xadr16),XY←XY+2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, [HL]	(xadr16)←[HL],[HL+1]	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, [XY]	(xadr16)←[XY],[XY+1]	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, E:[HL]	(xadr16)←E:[HL],E:[HL+1]	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, E:[XY]	(xadr16)←E:[XY],E:[XY+1]	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, [HL+]	(xadr16)←[HL],[HL+1],HL←HL+2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, [XY+]	(xadr16)←[XY],[XY+1],XY←XY+2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, E:[HL+]	(xadr16)←E:[HL],E:[HL+1],HL←HL+2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16, E:[XY+]	(xadr16)←E:[XY],E:[XY+1],XY←XY+2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Stack Operation Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
PUSH HL	(RSP)←{FLAG,A,HL}, RSP←RSP+1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	—	—	—
PUSH XY	(RSP)←{CBR,EBR,XY}, RSP←RSP+1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	—	—	—
POP HL	RSP←RSP−1, {FLAG,A,HL}←(RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	√	√	√
POP XY	RSP←RSP−1, {CBR,EBR,XY}←(RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	—	—	—

Flag Operation Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
FCLR G	G←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	—	—	√
FCLR C	C←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	—	√	—
FCLR Z	Z←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	√	—	—
FSET G	G←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	—	√
FSET C	C←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	—	√	—
FSET Z	Z←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	√	—	—

Jump Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LJMP cadr15	PC←cadr15	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMP cadr12	$PC_{11\sim0}$←cadr12	1	1	1	1	1	0	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
SJMP radr8	PC←Next PC+radr8	1	1	0	0	0	0	1	0	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
JMP PC+A	PC←PC+A+1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	—	—	—

Conditional Branch Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
												INSTRUCTION CODE								FLAG		
BC radr8 BLT radr8	if C=1 then PC←Next PC+radr8(<)	1	1	0	0	0	0	1	0	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNC radr8 BGE radr8	if C=0 then PC←Next PC+radr8($\geqq$)	1	1	0	0	0	0	1	0	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BZ radr8 BEQ radr8	if Z=1 then PC←Next PC+radr8(=)	1	1	0	0	0	0	1	1	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNZ radr8 BNE radr8	if Z=0 then PC←Next PC+radr8($\neq$)	1	1	0	0	0	0	1	1	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BLE radr8	if (C=1) $\lor$ (Z=1) then PC←Next PC+radr8($\leqq$)	1	1	0	0	0	0	1	1	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BGT radr8	if (C=0) $\land$ (Z=0) then PC←Next PC+radr8(>)	1	1	0	0	0	0	1	1	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNG radr8	if G=0 then PC←Next PC+radr8	1	1	0	0	0	0	1	0	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—

Call/Return Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
												INSTRUCTION CODE								FLAG		
LCAL cadr15	(SP)←PC,PC←cadr15, SP←SP+1	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1		—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
CAL cadr12	(SP)←PC,PC_{11-0}← cadr12,SP←SP+1	1	1	1	1	1	1	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
RT	PC←(SP)+1,SP←SP−1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	—	—	—
RTI	PC←(SP)+1,SP←SP−1, MIE←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	—	—	—
RTNMI	PC←(SP)+1,SP←SP−1 MIE←status of MIE before an interrupt occurs	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	—	—	—

Control Instructions

MNEMONIC	OPERATION	W	C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
NOP	NO OPERATION	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
HALT	HALT CPU	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	—	—	—
EI	MIE←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	—	—	—
DI	MIE←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	—	—	—
INCB HL	HL←HL+1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	—	—	√
INCB XY	XY←XY+1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	—	—	√
INCW RA	RA←RA+1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	—	—	√
MOV CBR,#i4	CBR←i4	1	1	0	0	0	0	0	0	0	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV EBR,#i4	EBR←i4	1	1	0	0	0	0	0	0	0	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA0,#i4	RA0←i4	1	1	0	0	0	0	0	0	1	0	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA1,#i4	RA1←i4	1	1	0	0	0	0	0	0	1	0	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV RA2,#i4	RA2←i4	1	1	0	0	0	0	0	0	1	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA3,#i4	RA3←i4	1	1	0	0	0	0	0	0	1	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV H,#i4	H←i4	1	1	0	0	0	0	0	0	0	1	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV L,#i4	L←i4	1	1	0	0	0	0	0	0	0	1	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV X,#i4	X←i4	1	1	0	0	0	0	0	0	0	1	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV Y,#i4	Y←i4	1	1	0	0	0	0	0	0	0	1	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MSA cadr15	Melody output starts	2	3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0			
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Appendix G Mask Option

The ML63326 can select the crystal oscillation circuit or the RC oscillation circuit as the oscillation circuit of the low-speed clock generator circuit by mask option.

To use the mask option, assign mask option data in the application program in accordance with the format below.

Assignment of the mask option data does not affect the application program execution area, because the areas for data assignment for each device are out of the program memory area.

• Mask option area for ML63326:   address 5FE0H

ML63326 Mask Option Data Assignment Format

Address	Function	Contents	Data	
5FE0H	Low-speed oscillation clock	Crystal oscillation/ RC oscillation	0: Crystal oscillation	1: RC oscillation

[Example of mask option data generation]

• When the crystal oscillation circuit is specified for the low-speed clock oscillation circuit

```
ORG    5FE0H      ← Use an assembler pseudo-instruction to set the address of option data
                     to 5FE0H.
DW     0          :  Low-speed oscillation clock, crystal oscillation
```

• When the RC oscillation circuit is specified for the low-speed clock oscillation circuit

```
ORG    5FE0H      ← Use an assembler pseudo-instruction to set the address of option data
                     to 5FE0H.
DW     1          :  Low-speed oscillation clock, RC oscillation
```

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