OKI Electronic Components

This version: Dec. 2000

KGL4202/KGL4202C Preliminary

10Gb/s/ 12.5Gb/s 1:8 Demultiplexer

GENERAL DESCRIPTION

The KGL4202/KGL4202C converts high-speed serial data stream into low-speed 8bit parallel data streams up to 10Gb/s/ 12.5Gb/s. Parallel data outputs are synchronized with the internal 1/8 clock generated from an input clock on chip. The device is ideal for use in the 10Gb/s/ 12.5Gb/s optical communication systems.

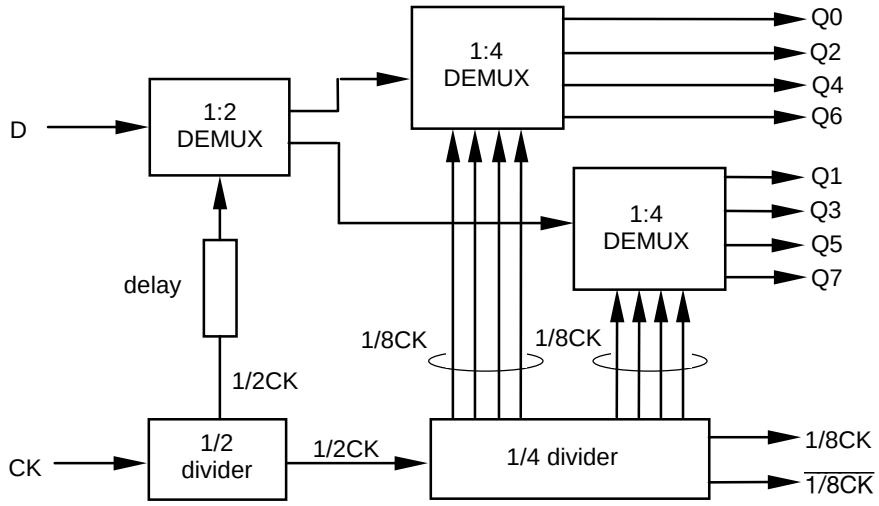
FEATURES

- High speed operation : 10Gb/s for KGL4202
  12.5Gb/s for KGL4202C
- Single power supply voltage : 2V
- Low power dissipation : 3.2W
- Package : 40 pin QFP

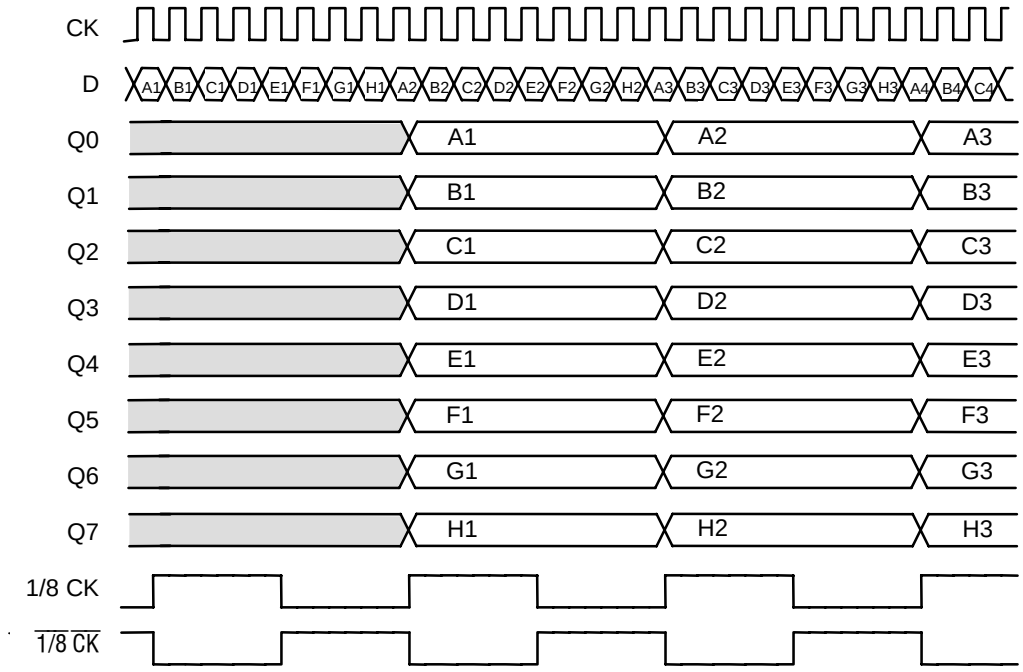
ABSOLUTE MAXIMUM RATINGS

No.	Item	Symbol	Min.	Max.	Unit
1	Supply Voltage for Internal Logic	V_{DD}	–0.3	2.3	V
2	Supply Voltage for Output Buffer	V_B	–0.3	2.3	V
3	Clock Input	CK	–0.3	1.5	V
4	Data Inputs	D	–0.3	1.5	V
5	Temperature at Package Base under Bias	T_s	–45	100	°C
6	Storage Temperature	T_{st}	–45	125	°C

FUNCTIONAL BLOCK DIAGRAM



TIME CHART



RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage for Internal Logic	V_{DD}	1.9	2.0	2.1	V
Power Supply Voltage for Output Buffer	V_B	1.9	2.0	2.1	V
Operating Temperature Range at Package Base	T_s	0		70	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 2 V, V_B = 2 V, Ts = 25°C

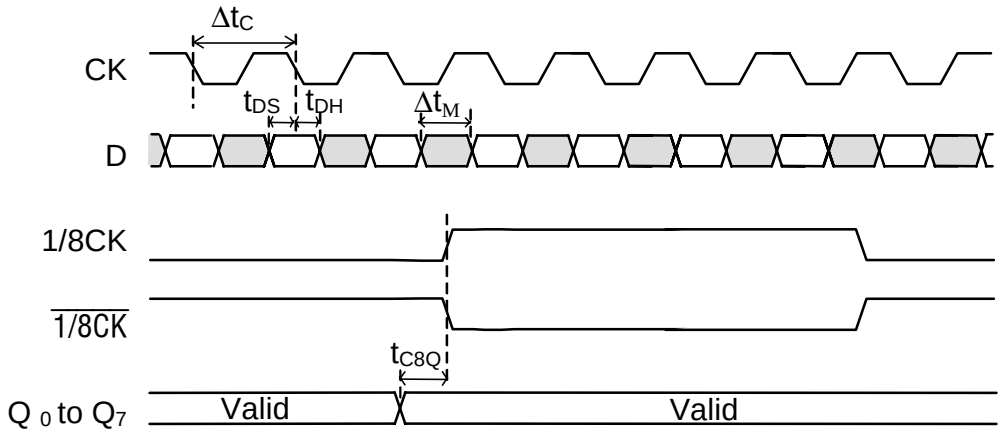
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Dissipation	P		—	3.2	4.0	W
High-level Output Voltage	V_{OH}	50 Ω Load	0.85		1.3	V
Low-level Output Voltage	V_{OL}	50 Ω Load	0.0		0.3	V
Clock Input Voltage Swing	V_{ICK}	Capacitive Coupling	0.5		0.9	Vp-p
Data Input Voltage Swing	V_{ID}	Capacitive Coupling	0.5		0.9	Vp-p

AC Characteristics

V_{DD} = 2 V, V_B = 2 V, Ts = 25°C

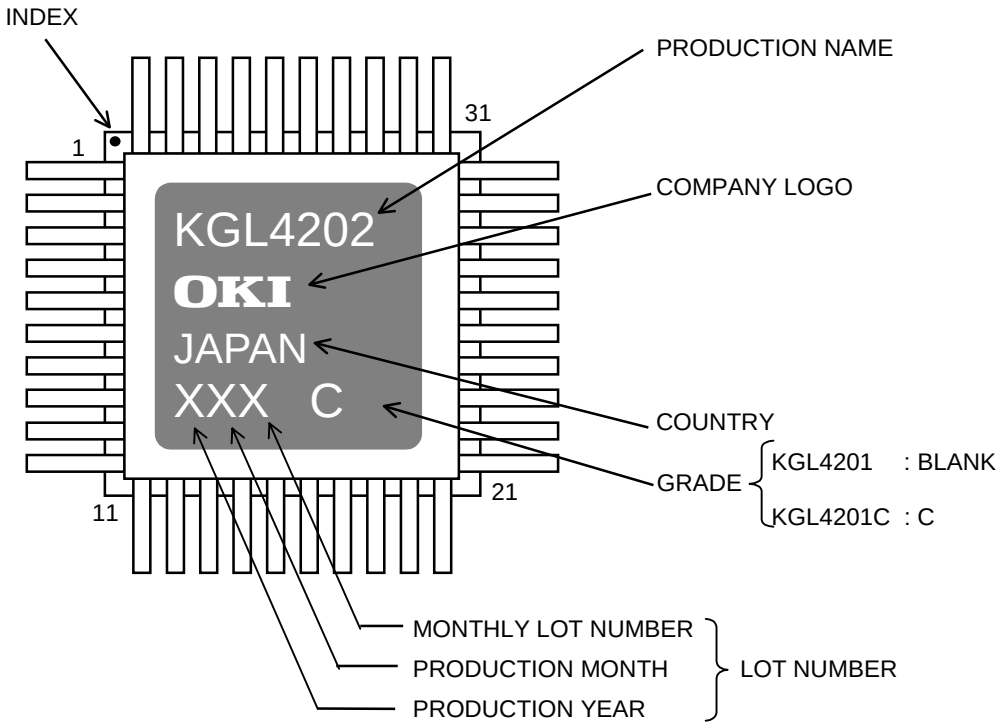
Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Operating	KGL4202	fo		10	—	—	GHz
Clock Frequency	KGL4202C			12.5	—	—	
Set-up Time (D to CK ↓)		t_{DS}		–60	–45	–30	ps
Hold Time (CK ↓ to D)		t_{DH}		65	80	95	ps
CK-D	KGL4202	Δt_M	fo = 10 GHz	50	65		ps
Phase Margin	KGL4202C		fo = 12.5 GHz	40	55		
1/8CK ↑ to Valid Data Delay		t_{C8Q}		–40	–10	20	ps

WAVEFORMS

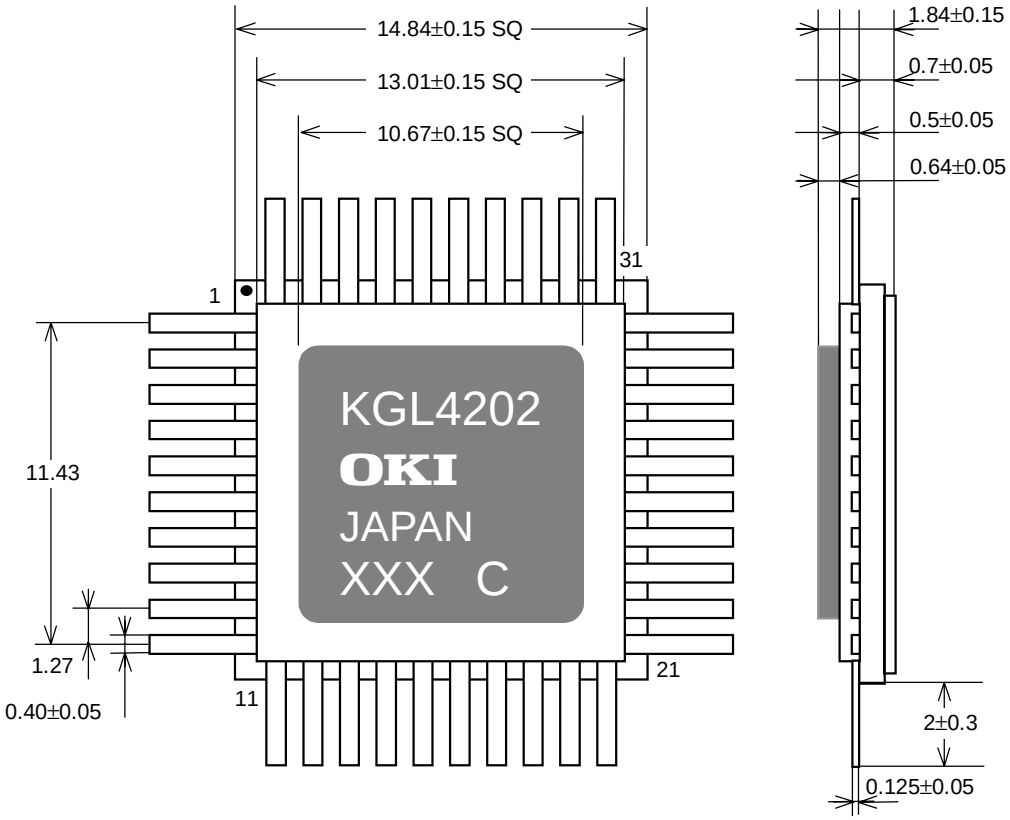


$\Delta t_C = 1/fo$

MARKING



PACKAGE INFORMATION



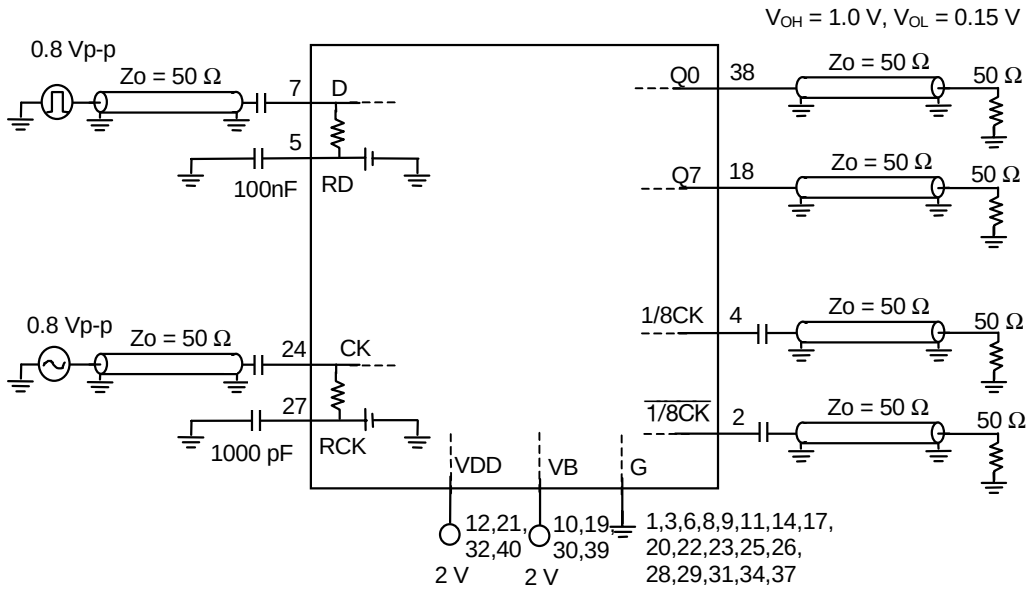
Top View

unit : mm

Pin Assignment

Pin	Symbol	Description	Pin	Symbol	Description
1	G	Ground	21	V_{DD}	Power Supply (Logic)
2	$\overline{1/8CK}$	$\overline{1/8\ Clock}$ Output	22	G	Ground
3	G	Ground	23	G	Ground
4	1/8CK	1/8 Clock Output	24	CK	Clock Input
5	RD	Data Reference Bias	25	G	Ground
6	G	Ground	26	G	Ground
7	D	Data Input	27	RCK	Clock Reference Bias
8	G	Ground	28	G	Ground
9	G	Ground	29	G	Ground
10	V_B	Power Supply (Buffer)	30	V_B	Power Supply (Buffer)
11	G	Ground	31	G	Ground
12	V_{DD}	Power Supply (Logic)	32	V_{DD}	Power Supply (Logic)
13	Q1	Data Output 1	33	Q6	Data Output 6
14	G	Ground	34	G	Ground
15	Q3	Data Output 3	35	Q4	Data Output 4
16	Q5	Data Output 5	36	Q2	Data Output 2
17	G	Ground	37	G	Ground
18	Q7	Data Output 7	38	Q0	Data Output 0
19	V_B	Power Supply (Buffer)	39	V_B	Power Supply (Buffer)
20	G	Ground	40	V_{DD}	Power Supply (Logic)

TYPICAL INTERFACE CONFIGURATION



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