OKI Semiconductor

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MSM7510/7512B Application Notes

ITU-T V.21/ITU-T V.23 Based Single Power Supply FSK Modem

1. GENERAL DESCRIPTION

Single power supplies MSM7510 and MSM7512B are LSIs for modems based on ITU-T V.21 and V.23 respectively.

MSM7510/7512B are upgrades of MSM6926/MSM6927, earlier versions that have been in use for some time. Power supplies that once required two lines (5 V, 12 V) now require only one, and have a wide operation range (2.7 V to 5.5 V). The analog system interface has also been simplified. The resistance hybrid circuit, which was external, is now onboard an LSI so that the 600 Ω transformer can be directly driven.

Single power supply FSK modems can be applied to a wide range of fields, such as telecontrol systems and home security systems.

This instruction manual introduces standard application examples to customers who design modems. This manual does not include the specifications for MSM7510 and MSM7512B. Refer to separate data sheets for that information.

2. FEATURES

2.1 MSM7510

- Based on ITU-T V. 21 (Data transmission rate: 0 to 300 bps, full duplex)
- Built-in ITU-T answer tone (2100 Hz) transmit/receive function

2.2 MSM7512B

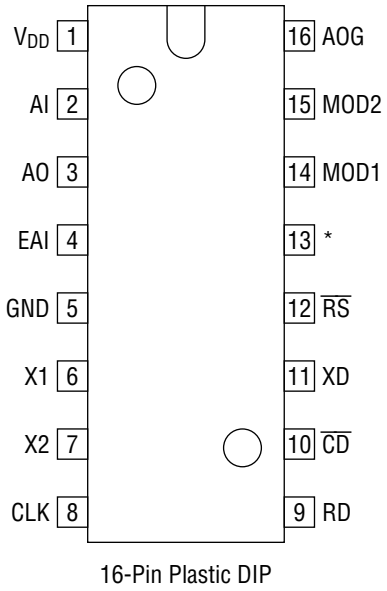
- Based on ITU-T V.23 (Data transmission rate: 0 to 1200 bps, half duplex)
- Built-in ITU-T V.23 backward (75 bps) transmit function
- Built-in NRTS signal (2765 Hz) removal filter

2.3 MSM7510/MSM7512B

- 3 V to 5 V single power supply
- Low power consumption
  During operation: 9 mW (V_{DD} = 3 V), 25 mW (V_{DD} = 5 V)
  Power down: 100 µW
- Built-in resistance hybrid circuit (600 Ω direct drive possible)
- Built-in ALB (Analog Loop Back) test function
- Built-in 3.579545 MHz crystal oscillation circuit
- Digital input/output: TTL compatible
- Package options :

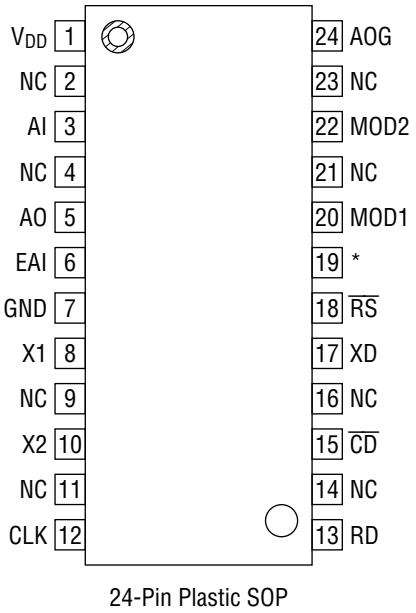
16-pin plastic DIP	(DIP16-P-300-2.54)	(Product name : MSM7510RS)
		(Product name : MSM7512BRS)
24-pin plastic SOP	(SOP24-P-430-1.27-K)	(Product name : MSM7510GS-K)
		(Product name : MSM7510BGS-K)

3. PIN CONFIGURATION (TOP VIEW)



16-Pin Plastic DIP

Figure 3-1 MSM7510/7512BRS



24-Pin Plastic SOP

Figure 3-2 MSM7510/7512BGS-K

* MSM7510 : O/A

MSM7512B : $\overline{\text{TEST}}$

NC : No connect pin

4. PERIPHERAL CIRCUIT EXAMPLES

4.1 When Using Crystal

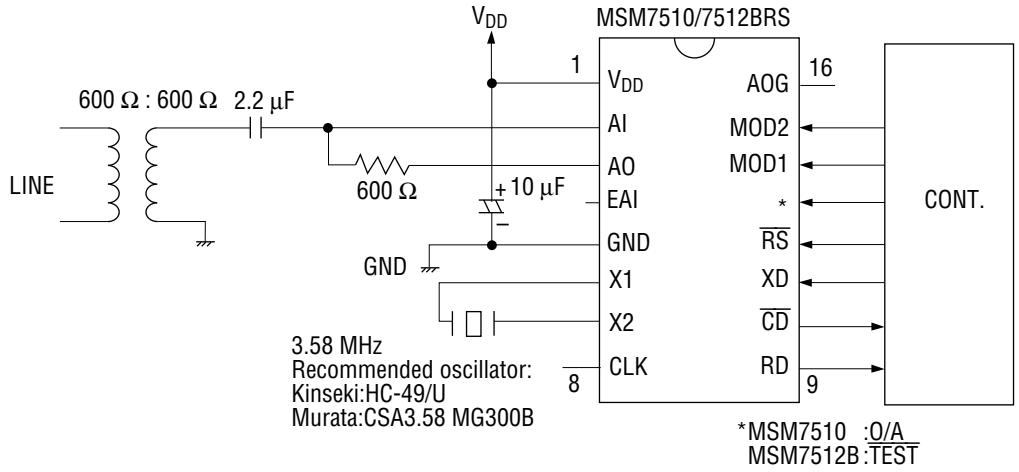


Figure 4.1 Peripheral Circuit 1

Note: Internal Oscillation Circuit

In the MSM7510 and MSM7512B, an approximate 1 MΩ feedback resistance is built-in between X1 and X2, and an approximate 10 pF capacitance is built-in between X1-GND and X2-GND.

4.2 When Using External Oscillator:

When another analog signal has mixed output and the IC has cascade-connections

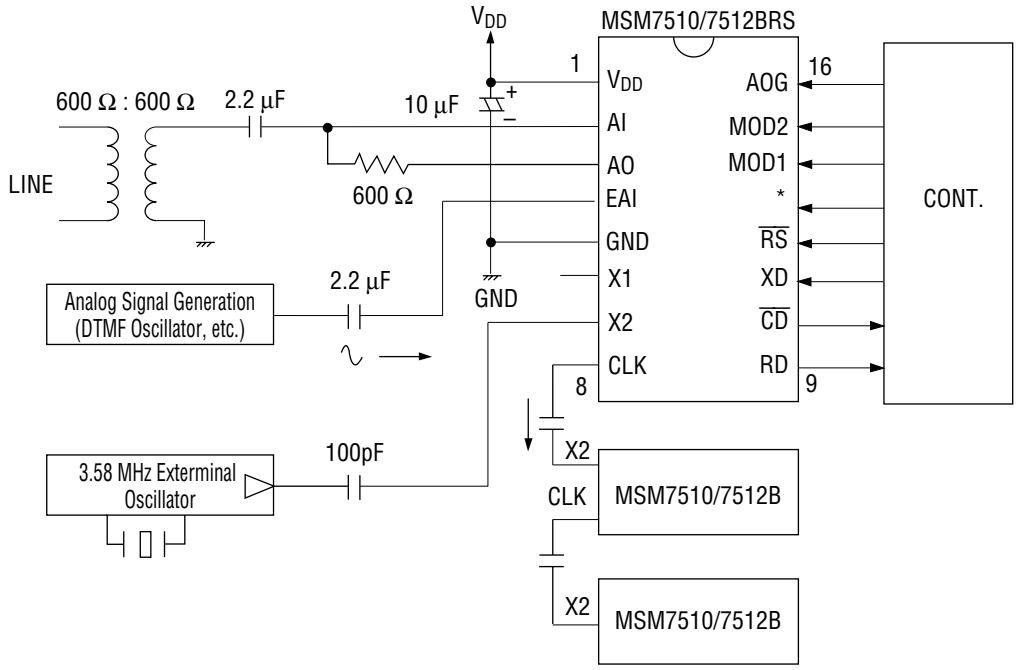


Figure 4-2 Peripheral circuit 2

Note: Input Pins

Digital input pins of the MSM7510 and MSM7512B are pulled up to V_{DD} in LSIs at about 500 kΩ to 1 MΩ of resistance. In power down mode, the current consumption can be minimized by setting all digital input pins to open, or by connecting them to V_{DD}.

All input pins of MSM7510 and MSM7512B are connected to V_{DD} via diodes. If voltage is applied to an input pin without supplying power to the LSI, unnecessary current flows into the LSI from the pin. Therefore, if power is not supplied to the LSI, leave all input pins open or set to the GND potential.

4.3 When Externally Adjusting Transmit/Receive Levels

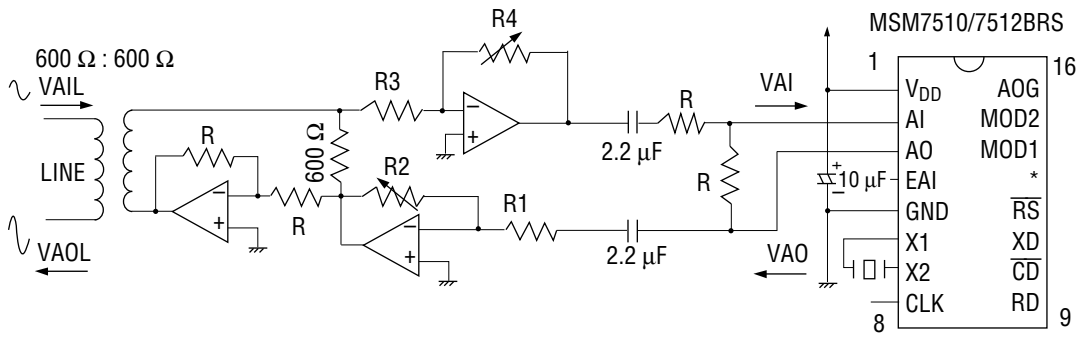


Figure 4-3 Peripheral Circuit 3

Note: If the transmit/receive level of each AO/AI pin of an LSI is set to VAO/VAI, and the transmit/receive level on LINE is set to VAOL/VAIL, the transmit level to LINE and the receive level of an LSI can be independently set. (This is possible when the telephone line impedance is adjusted, and transformer attenuation is zero.)

LINE transmit level: $VAOL = VAO \times (R2/R1)$
LSI receive level: $VAI = VAIL/2 \times (R4/R3)$

Since transmit signal VAO enters input pin AI as VAO/2, that signal theoretically is zero due to the LSI resistance hybrid circuit (See 4.4). In reality, however, the signal does not completely become zero due to the unmatched telephone line impedance and dispersion of individual components. To avoid this, the bandpass filter on the LSI attenuates the signal element outside the band at about 40 dB, preventing erroneous operation during full duplex mode.

Example

Figure 4.4 shows the level at each point when this application circuit example is actually used.

(R1 = 72 kΩ, R2 = 51 kΩ, R3 = 20 kΩ, R4 = 51 kΩ, transformer loss = 2 dB.)

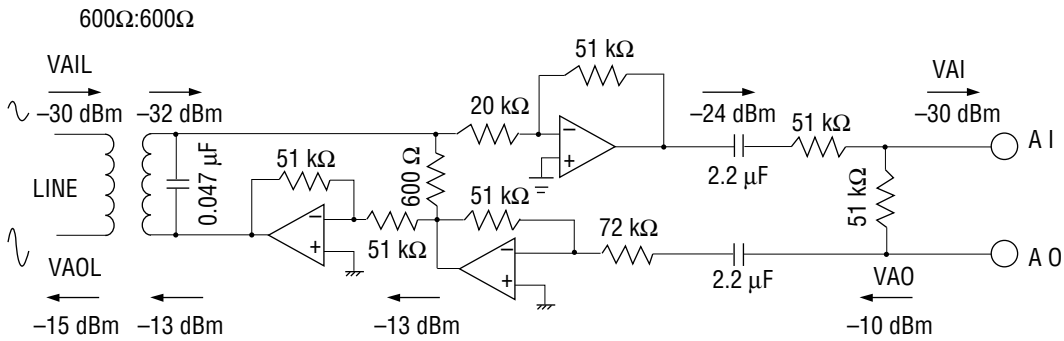


Figure 4-4 Actual Example

4.4 Internal Resistance Hybrid Circuit

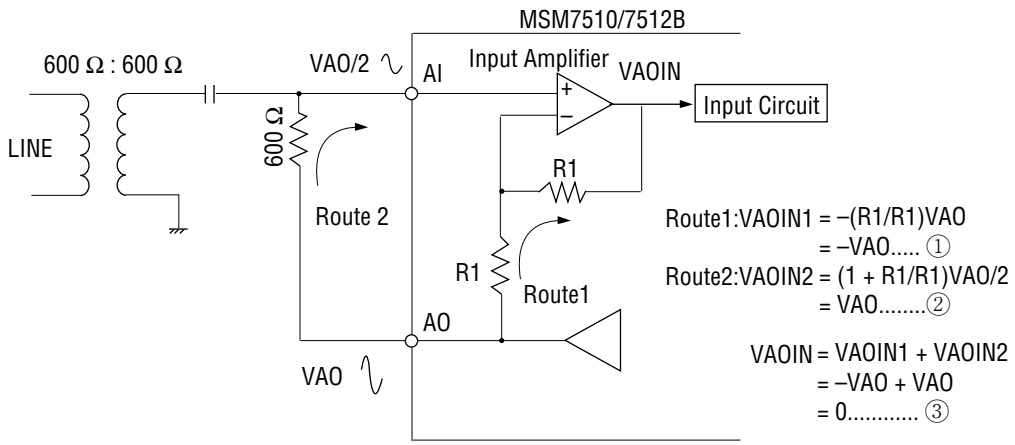


Figure 4-5 Functions of Resistance Hybrid Circuit

Figure 4-5 shows the functioning of the resistance hybrid circuit that prevents transmit signals from entering the input circuit. If the signal transmit level of the AO pin is VAO, and if the impedance around the line is optimal, the transmit signal becomes VAO/2 at the AI pin. The transmit signal also enters the input circuit via routes 1 and 2, and the level (VAOIN) at the input amplifier output component becomes -VAO and VAO respectively ①, ②. This means that the total level of these two routes become zero ③, and the transmit signal no longer enters the input circuit.

5. RECEIVE FILTER FREQUENCY CHARACTERISTICS

Figures 5-1 and 5-2 show the receive filter frequency characteristics of the MSM7510 and MSM7512B.

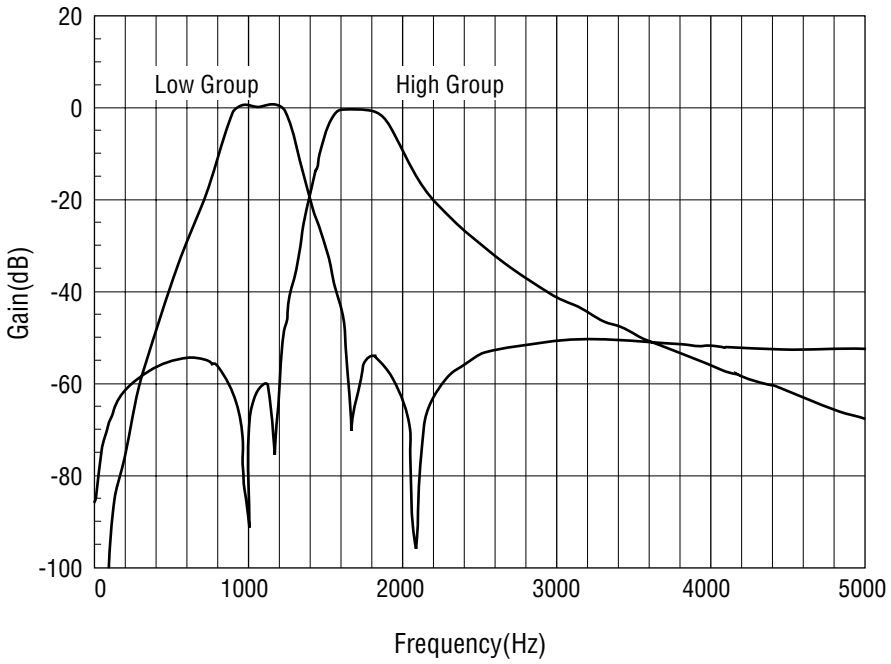


Figure 5-1 MSM7510 Receive Filter

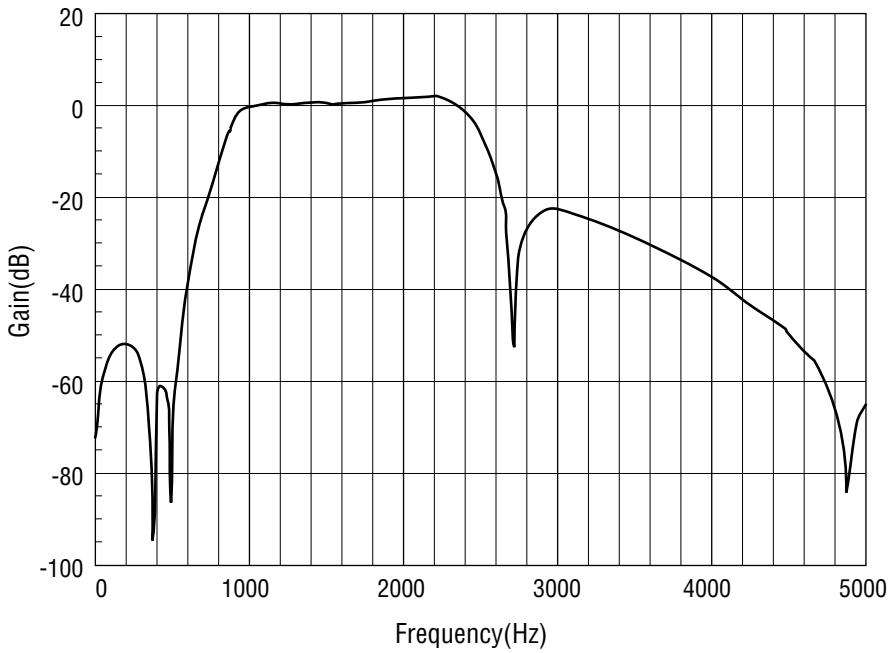
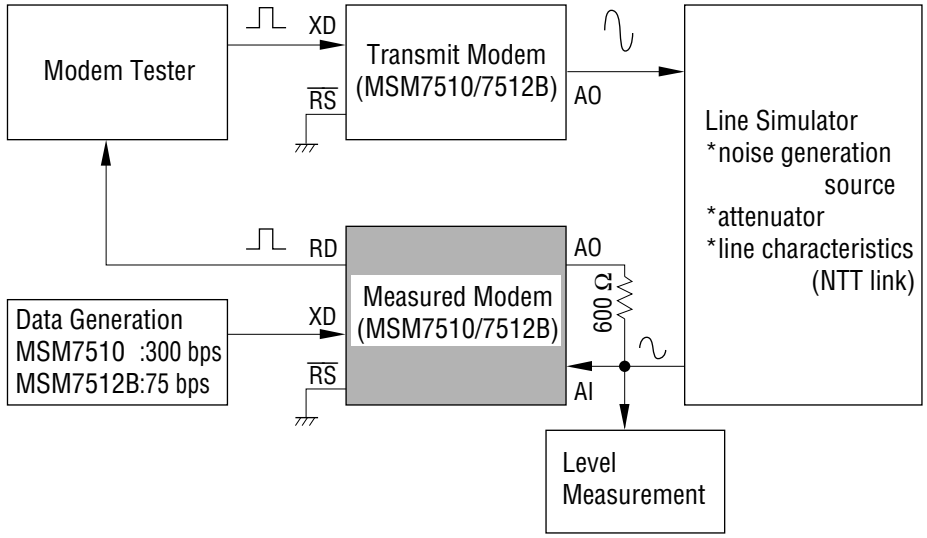


Figure 5-2 MSM7512B Receive Filter

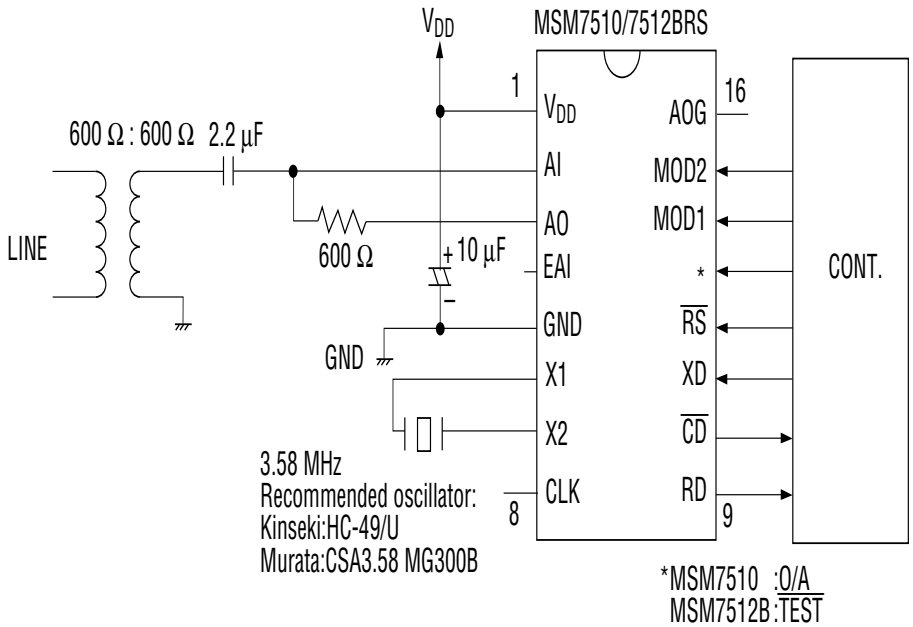
6. BER (BIT ERROR RATE)

Figures 6-1 to 6-4 show the measurement circuit and actual data on the BER of MSM7510 and MSM7512B.



Conditions: V_{DD} = 5 V, Room Temperature
S = –30 dBm, 511PN pattern
N = white noise

Figure 6-1 BER Measurement Circuit



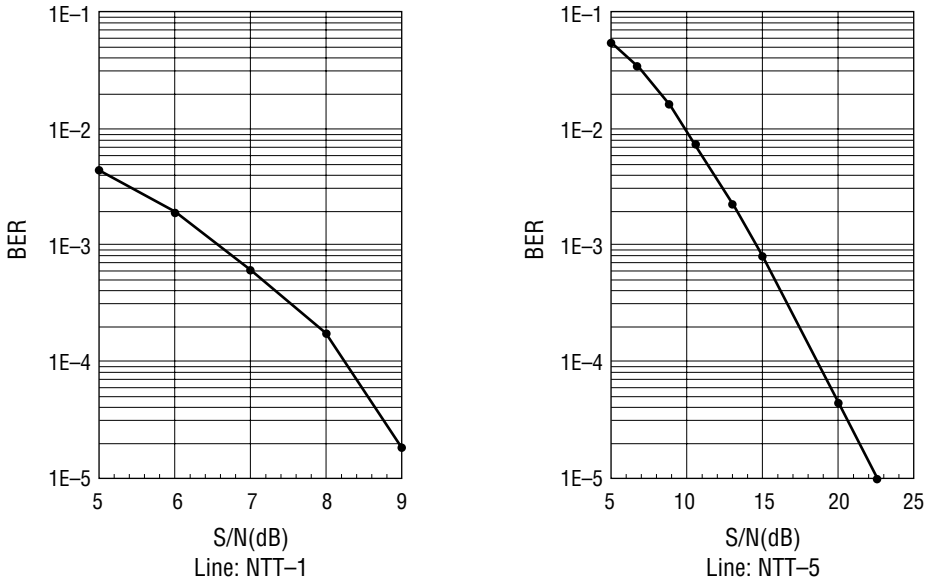


Figure 6-3 MSM7512B S/N vs. BER

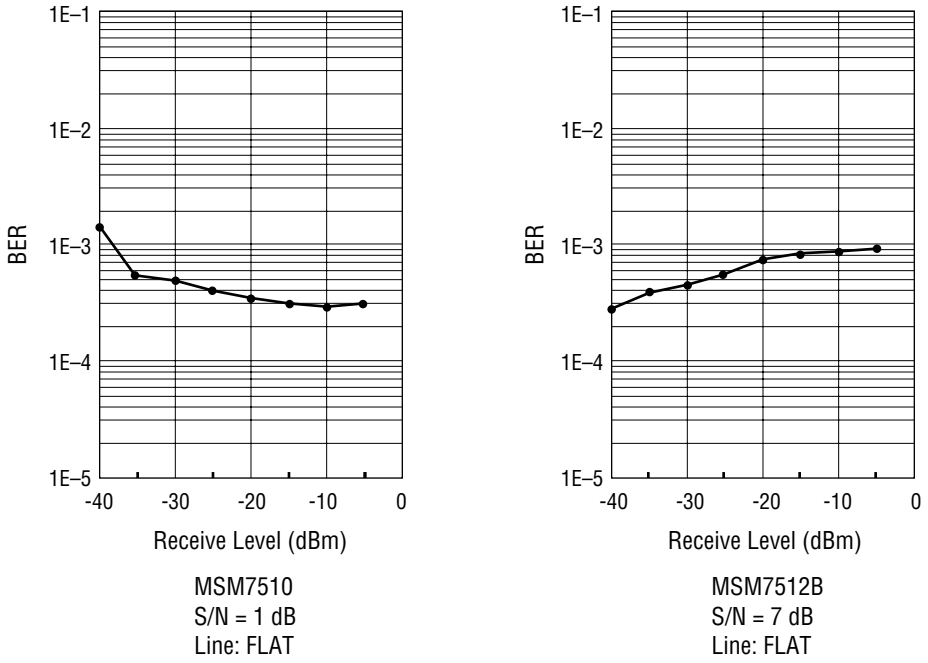


Figure 6-4 MSM7510/7512B Receive Level vs. BER

7. CHARACTERISTIC DETERIORATION BY POWER NOISE

Noise superimposed on the power supply (V_{DD}) affects such characteristics as the bit error rate. This is due to an internal filter that consists of a switched capacitor (SC) circuit that cannot eliminate very high frequency noise. Specifically, noise (integer multiple) passes through the internal filter as a sampling frequency of the 28 kHz ± (passband) of the SC circuit. That noise is received as a modem signal. In this event, "carrier" is detected during a "no signal time". CD does not turn off, even though a "carrier off" is observed. To prevent such characteristic deterioration, suppress as much of the power supply noise as possible using bypass capacitors, etc. Figures 7-1 to 7-3 show the result of this observed event.

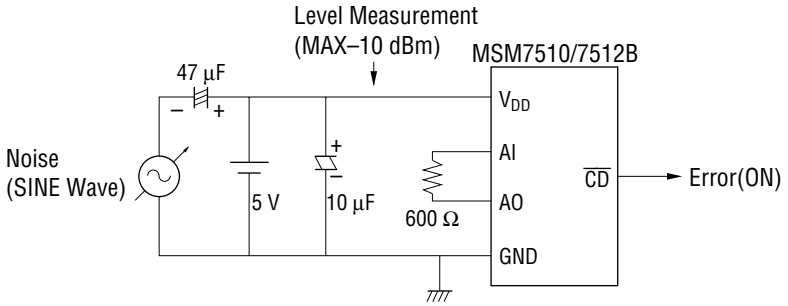


Figure 7-1 Power Noise Evaluation Circuit

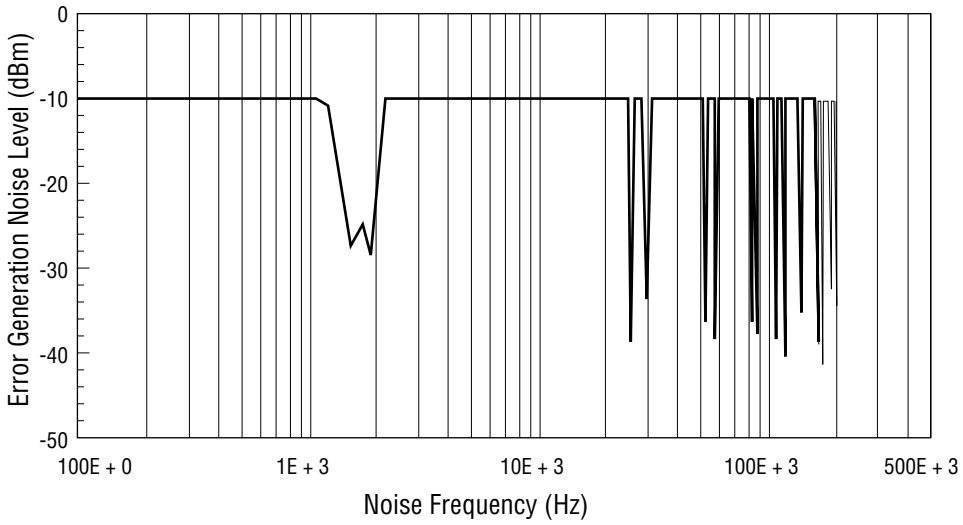


Figure 7-2 Characteristic Deterioration by MSM7510 Power Noise

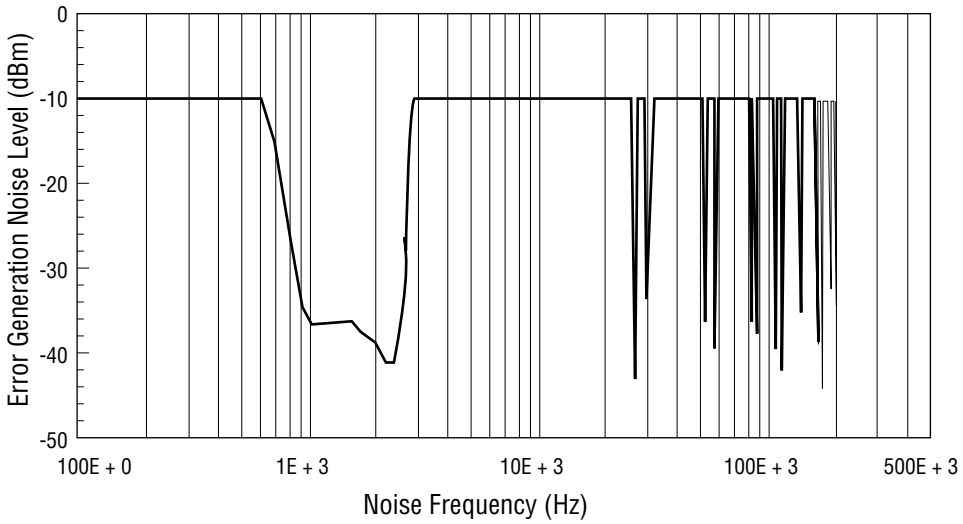


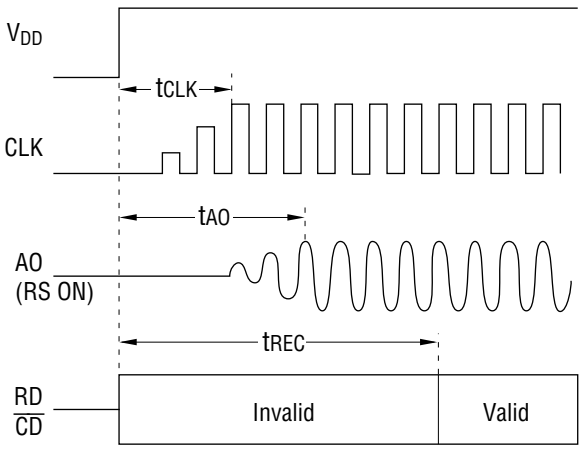
Figure 7-3 Characteristic Deterioration by MSM7512B Power Noise

8. RESPONSE TIME WHEN POWER IS TURNED ON

Shown below is the response time until the LSI operates normally when power is turned on, or when the mode is switched from power down mode to operation mode. LSI operation is not guaranteed during the response time.

Since the data below was measured under normal conditions, for actual use it may require a time frame that is twice as long.

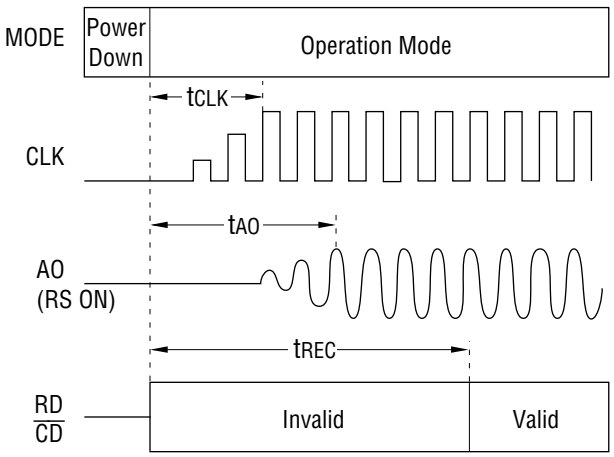
8.1 Actual Response Time Data when Power is Turned On



Item	M7510		M7512B		Unit
	V_{DD}		V_{DD}		
	3 V	5 V	3 V	5 V	
tCLK	5.8	3.9	5.7	3.6	ms
tAO	8.0	10.0	5.2	5.9	
tREC	37.0	47.0	38.0	42.0	

Figure 8-1 Response Time when Power is Turned On

8.2 Actual Response Time when Power Down Mode is Switched to Operator Mode



Item	M7510		M7512B		Unit
	V_{DD}		V_{DD}		
	3 V	5 V	3 V	5 V	
tCLK	7.0	3.2	4.4	2.9	ms
tAO	10.0	5.0	4.3	3.0	
tREC	40.0	44.0	37.0	41.0	

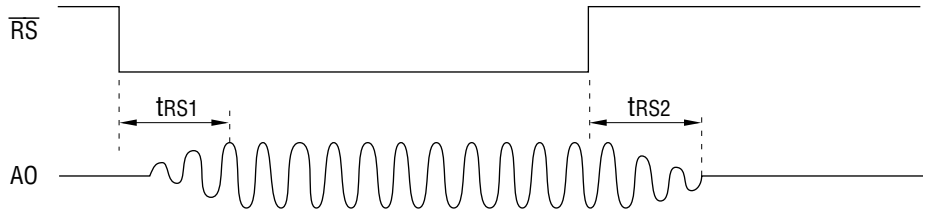
Figure 8-2 Response Time when Power Down Mode is Switched to Operation Mode

9. TRANSMIT/RECEIVE RESPONSE TIME

Shown below are the response times for transmit (RSON to carrier output) and the response times for receive (carrier input to CD ON).

Since the data below was measured under normal conditions, for actual use it may require a time frame of about twice as long.

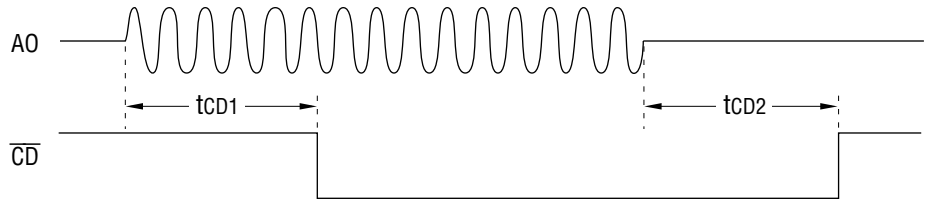
9.1 Actual Response Time for Transmit



Item	M7510		M7512B		Unit
	V_{DD}		V_{DD}		
	3 V	5 V	3 V	5 V	
tRS1	4.5	4.5	2.0	2.0	ms
tRS2	10.0	10.0	6.0	6.0	

Figure 9-1 Response Time for Transmit

9.2 Actual Response Time for Receive



Item	M7510		M7512B		Unit
	V_{DD}		V_{DD}		
	3 V	5 V	3 V	5 V	
tCD1	13.5	12.5	11.0	9.8	ms
tCD2	39.5	43.5	34.5	42.0	

Figure 9-2 Response Time for Receive

Note: In the tCD2 period shown in Figure 9-2, after receiving normal data, RD may output data other than the receive data. This is because the demodulator output is received when CD timer off is operating, to prevent any instant cutoffs. If this event causes difficulties, handle them externally.

10. POWER VOLTAGE DEPENDENCY CHARACTERISTICS

The power voltage dependency characteristics for operating current (I_{DD}), carrier transmit levels, and carrier detection (CD OFF → ON) levels are shown below. This data was measured under normal conditions.

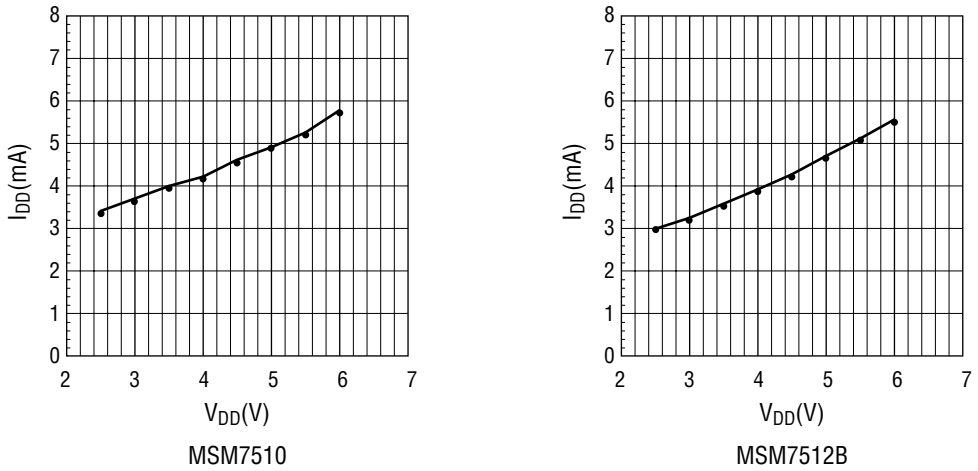


Figure 10-1 Power Voltage Dependency for Operating Current (I_{DD})

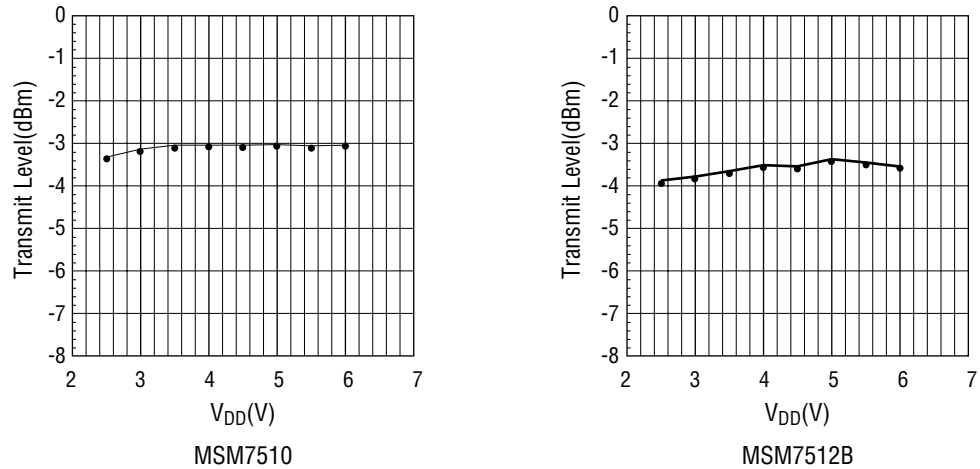


Figure 10-2 Power Voltage Dependency for Carrier Transmit Levels

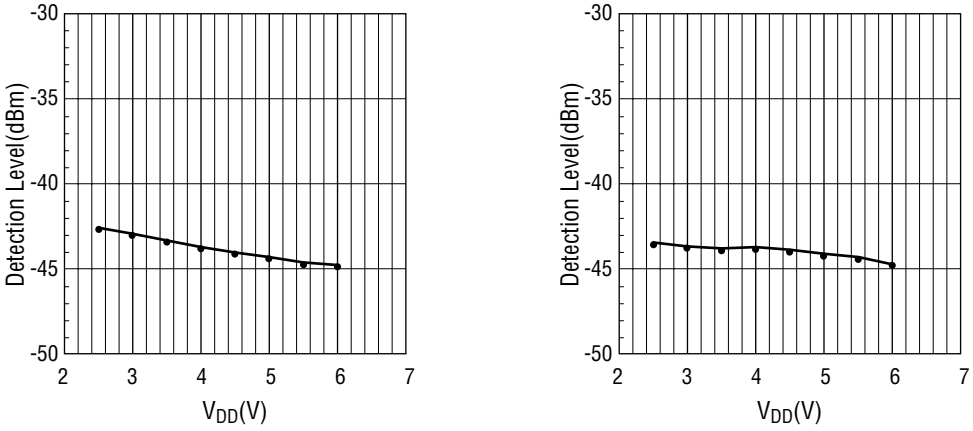
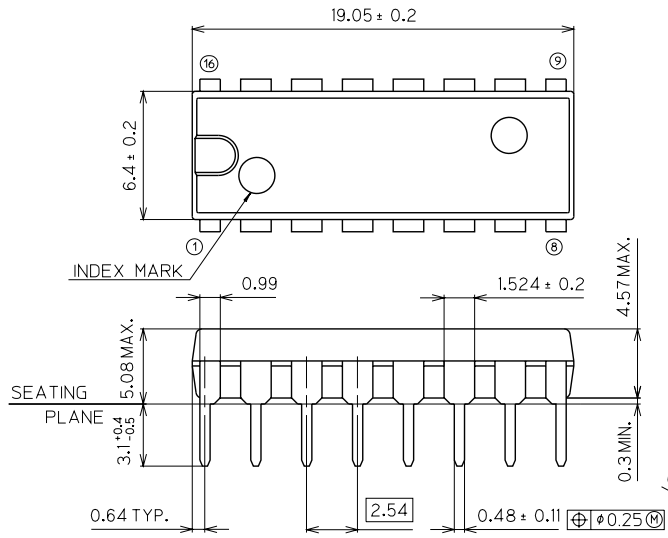


Figure 10-3 Power Voltage Dependency for Carrier Detection (CD ON) Levels

PACKAGE DIMENSIONS

(Unit : mm)

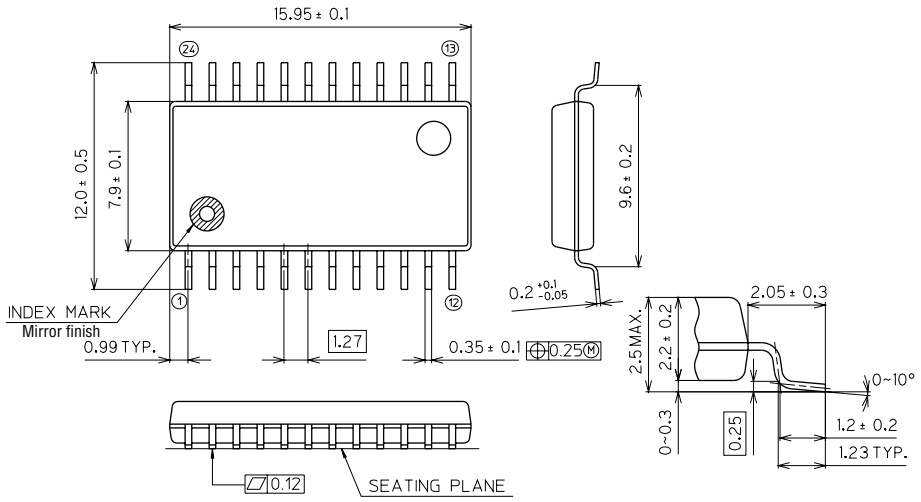
DIP16-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.99 TYP.

(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).