OKI Semiconductor

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MSM6568A

160-DOT COMMON DRIVER

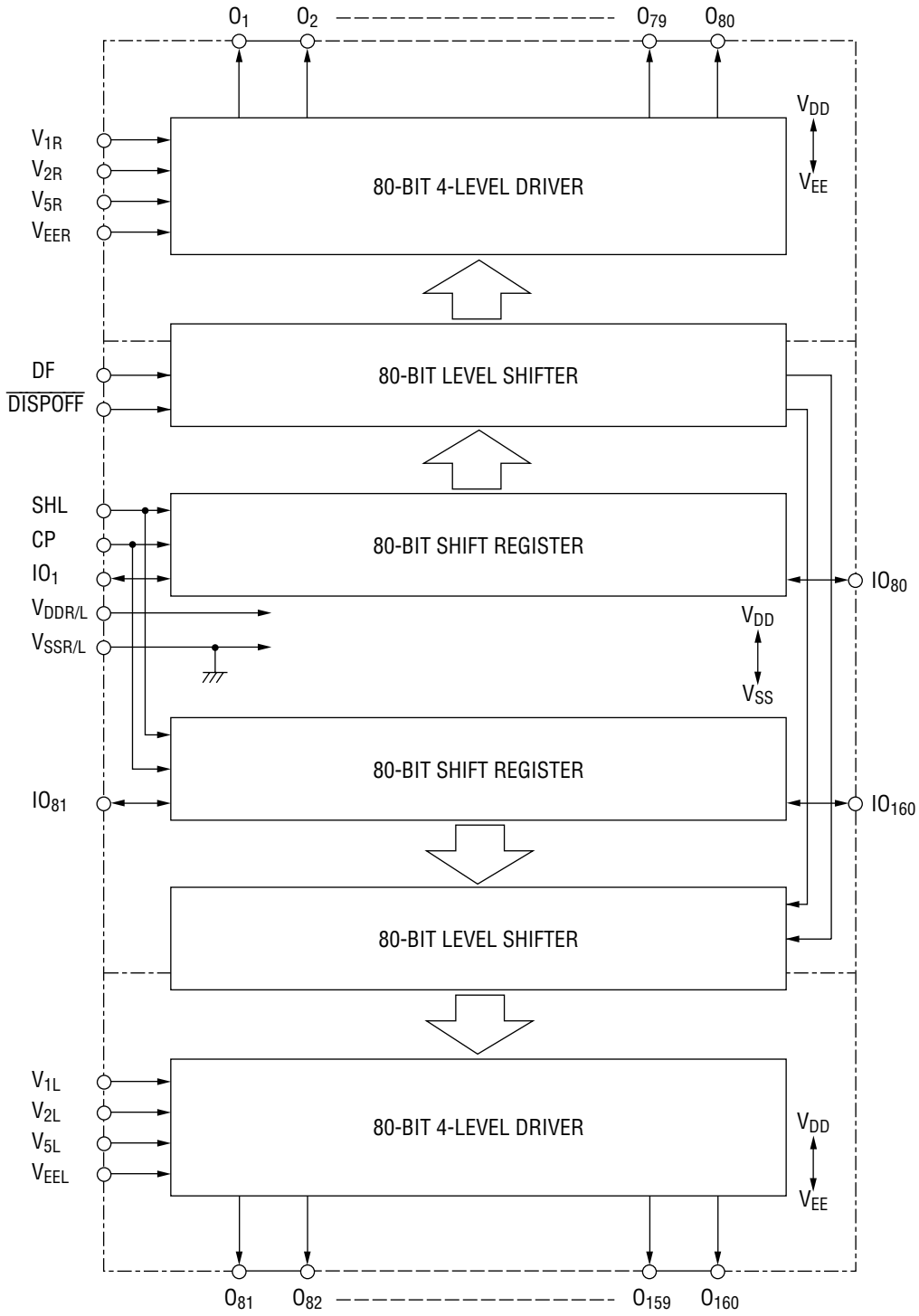
GENERAL DESCRIPTION

The MSM6568A is a dot matrix LCD common driver which is fabricated in CMOS technology. The MSM6568A consists of two 80-bit bidirectional shift registers, two 80-bit level shifters, and two 80-bit 4-level drivers.
The MSM6568A is equipped with 160 output pins. By connecting two or more MSM6568A devices in cascade, the number of LCD outputs can be increased.
The MSM6568A can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from an external source.

FEATURES

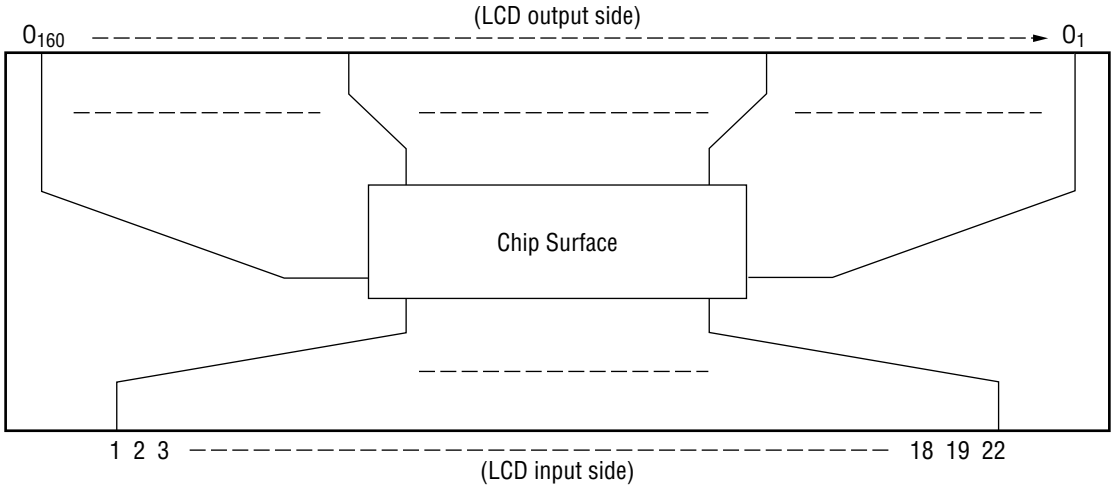
- Logic supply voltage : 2.7 to 5.5V
- LCD driving voltage : 14 to 28V
- Applicable LCD duty : 1/64 to 1/256
- External bias power supply available
- Package :
  TCP mounting with 70mm wide film (Product name : MSM6568AV-Z)
  Tin-plated

BLOCK DIAGRAM



($V_{DDR/L}$ stands for V_{DDR} and V_{DDL}, and $V_{SSR/L}$ for V_{SSR} and V_{SSL}.)

PIN CONFIGURATION (TOP VIEW)



Pin	Symbol	Pin	Symbol
1	V_{1L}	12	IO_{160}
2	V_{2L}	13	IO_{81}
3	V_{5L}	14	IO_{80}
4	V_{EEL}	15	IO_1
5	NC	16	V_{SSR}
6	V_{DDL}	17	V_{DDR}
7	SHL	18	NC
8	V_{SSL}	19	V_{EER}
9	$\overline{DISPOFF}$	20	V_{5R}
10	CP	21	V_{2R}
11	DF	22	V_{1R}

NC : No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +6.5	V
Bias Voltage	V_{LCD}	Ta=25°C, $V_{DD} - V_{EE}$	0 to 30	V
Input Voltage	V_I	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–30 to +85	°C

* $V_1 > V_2 > V_5 > V_{EE}$
$V_{EE} < V_5 \leq V_{EE}+10V$
$V_{DD} \geq V1 > V2 \geq V_{DD}-10V$
$V_{DD}=V_{DDR}=V_{DDL}$, $V_1=V_{1R}=V_{1L}$, $V_2=V_{2R}=V_{2L}$,
$V_5=V_{5R}=V_{5L}$, $V_{EE}=V_{EER}=V_{EEL}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Power Supply Voltage	V_{DD}	—		2.7 to 5.5	V
Bias Voltage	V_{LCD}	$V_{DD} - V_{EE}$	No load	14 to 28	V
			LCD being driven	18 to 28	V
Operating Temperature	T_{op}	—		–20 to +75	°C

* $V_1 > V_2 > V_5 > V_{EE}$
$V_{EE} < V_5 \leq V_{EE}+7V$
$V_{DD} \geq V1 > V2 \geq V_{DD}-7V$
$V_{DD}=V_{DDR}=V_{DDL}$, $V_1=V_{1R}=V_{1L}$, $V_2=V_{2R}=V_{2L}$,
$V_5=V_{5R}=V_{5L}$, $V_{EE}=V_{EER}=V_{EEL}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=2.7 to 5.5V, Ta=–20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	—	V
"L" Input Voltage	V_{IL} *1	—	—	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	V_I=V_{DD}, V_{DD}=5.5V	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I=0V, V_{DD}=5.5V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O=–0.2mA, V_{DD}=2.7V	V_{DD}–0.4	—	—	V
"L" Output Voltage	V_{OL} *2	I_O=0.2mA, V_{DD}=2.7V	—	—	0.4	V
ON Resistance	R_{ON} *4	V_{DD}–V_{EE}=25V *3	—	—	2.0	kΩ
		I V_N–V_O I=0.25V	—	—		
Supply Current	I_{SS}	CP=22kHz, V_{DD}=3.0V	—	—	50	µA
	I_{EE}	V_{DD}–V_{EE}=25V, no load*5	—	—	300	
Input Capacitance	C_I	f=1MHz	—	5	—	pF

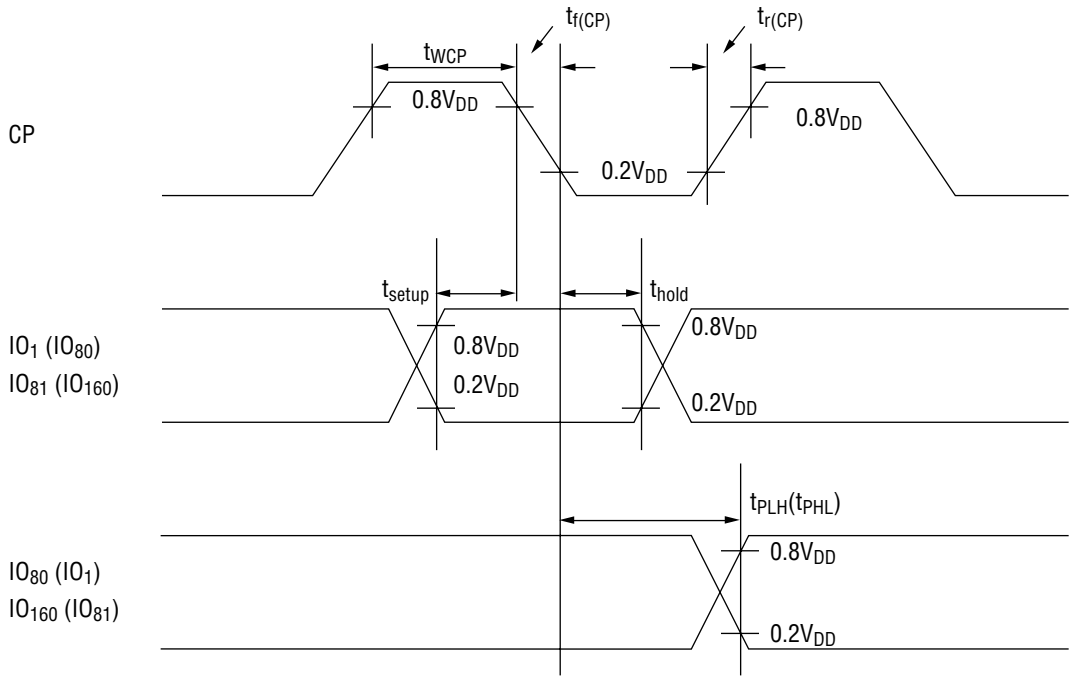
*1 Applied to CP, IO_1, IO_{80}, IO_{81}, IO_{160}, SHL, DF, $\overline{DISPOFF}$
*2 Applied to IO_1, IO_{80}, IO_{81}, IO_{160}
*3 V_N=V_{DD} to V_{EE}, V_2=1/16 (V_{DD} – V_{EE}), V_5=15/16 (V_{DD} – V_{EE})
V_{DD}=V_1, V_{DD}=4.5V, V_1=V_{1L}=V_{1R}, V_2=V_{2L}=V_{2R}, V_5=V_{5L}=V_{5R}, V_{EE}=V_{EEL}=V_{EER},
V_{DD}=V_{DDL}=V_{DDR}
*4 Applied to O_1 to O_{160}
*5 Input a "H" level signal through the IO pins every 240 clock pulses when a supply current is measured.
The DF frequency is 45Hz.

Switching Characteristics

(V_{DD}=2.7 to 5.5V, Ta=–20 to +75°C, C_L=15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PHL} t_{PLH}	—	—	—	3	µs
Maximum Clock Frequency	f_{CP}	—	1	—	—	MHz
Clock Pulse Width	t_{WCP}	—	63	—	—	ns
Data Setup Time IO_n→CP *1	t_{setup}	—	100	—	—	ns
Data Hold Time CP→IO_n *1	t_{hold}	—	100	—	—	ns
Rise Time / Fall Time of CP	$t_{r(CP)}$ $t_{f(CP)}$	—	—	—	20	ns

*1 IO_n=IO_1-IO_{160}


$t_{f(CP)}$
$t_{r(CP)}$
t_{WCP}
CP
$0.8V_{DD}$
$0.2V_{DD}$
$0.8V_{DD}$
t_{setup}
t_{hold}
IO_1 (IO_{80})
IO_{81} (IO_{160})
$0.8V_{DD}$
$0.2V_{DD}$
$0.8V_{DD}$
$0.2V_{DD}$
$t_{PLH}(t_{PHL})$
IO_{80} (IO_1)
IO_{160} (IO_{81})
$0.8V_{DD}$
$0.2V_{DD}$

FUNCTIONAL DESCRIPTION

Pin Functional Description

- IO_1, IO_{80}, IO_{81}, IO_{160}
  Data input/output pins for the two 80-bit bidirectional shift registers.
- SHL
  Input pin to select the shift direction of the two 80-bit bidirectional registers.
  Table 1 shows the relations between the SHL pin and the IO_1, IO_{80}, IO_{81}, IO_{160} pins.
- CP
  Clock pulse input pin for the two 80-bit bidirectional shift registers.
  Scan data shifts at the falling edge of a clock pulse.
- DF
  Signal input pin to synchronize with AC current for LCD driving waveforms.
  Normally an inverted frame signal is input to this pin.
- V_{DDL}, V_{DDR}, V_{SSL}, V_{SSR}
  Power supply pins.
  Normal operating conditions are $V_{DDR}=V_{DDL}=2.7$ to 5.5V, $V_{SSR}=V_{SSL}=0$V.
- $\overline{DISPOFF}$
  Input pin to control the O_1 to O_{160} outputs. During input of "L" level, V_1 levels are output from O_1 to O_{160}.
- V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{5L}, V_{5R}, V_{EEL}, V_{EER}
  Bias voltage input pins for LCD driving. Voltages must be input to all these pins.
- O_1 to O_{160}
  4-level driver output pins corresponding to each bit of the shift registers.
  The V_1, V_2, V_5, or V_{EE} level is selected and output based on the combination of shift register data and a DF signal.
  Table 2 shows the relations between the scan data and the LCD driving outputs.

Table 1

SHL	Shift direction	IO_1, IO_{81} / IO_{80}, IO_{160}	I/O	Input
L	$O_1 \rightarrow O_{80}$ $O_{81} \rightarrow O_{160}$	IO_1, IO_{81}	Input	IO_1 and IO_{81} are data input pins for the shift register. Data is input to these pins in synchronization with clocks and is output from IO_{80} and IO_{160} with delay by the number (80) of shift register bits in synchronization with clocks.
		IO_{80}, IO_{160}	Output	
H	$O_{80} \rightarrow O_1$ $O_{160} \rightarrow O_{81}$	IO_{80}, IO_{160}	Input	IO_{80} and IO_{160} are data input pins for the shift register. Data is input to these pins in synchronization with clocks and is output from IO_1 and IO_{81} with delay by the number (80) of shift register bits in synchronization with clocks.
		IO_1, IO_{81}	Output	

Table 2

Scan data	LCD driving output
H	Select levels (V_1, V_{EE})
L	Non-select levels (V_2, V_5)

Truth Table

DF	Shift register data	$\overline{\text{DISPOFF}}$	Driver output level (O_1-O_{160})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

X : Don't Care