

# OKI Semiconductor

## MSM63184B

**4-Bit Microcontroller with Built-in 640-Dot Matrix LCD Drivers, Operating at 0.9 V (Min.)**

### GENERAL DESCRIPTION

The MSM63184B is a CMOS 4-bit microcontroller with built-in 640-dot matrix LCD drivers and operates at 0.9 V (min.). The MSM63184B is suitable for applications such as games, toys, watches, etc. which are provided with an LCD display.

The MSM63184B is an M6318x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

The MSM63P180 is the one-time-programmable ROM version of MSM63188, having one-time PROM (OTP) as internal program memory.

The MSM63P180 is used to evaluate the software development.

### FEATURES



- Rich instruction set
  - 439 instructions
  - Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, branch, conditional branch, call/return, control.
- Rich selection of addressing modes
  - Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  - Data memory bank internal direct addressing mode.
- Processing speed
  - Two clocks per machine cycle, with most instructions executed in one machine cycle.
  - Minimum instruction execution time : 61  $\mu$ s (@ 32.768 kHz system clock)
  - 1  $\mu$ s (@ 2 MHz system clock)
- Clock generation circuit
  - Low-speed clock : 32.768 kHz crystal oscillator
  - High-speed clock : 2 MHz (Max.) RC or ceramic oscillator select
- Program memory space
  - 8K words
  - Basic instruction length is 16 bits/1 word
- Data memory space
  - 640 nibbles
- External data memory space
  - 64 Kbytes (expandable by using an I/O port)

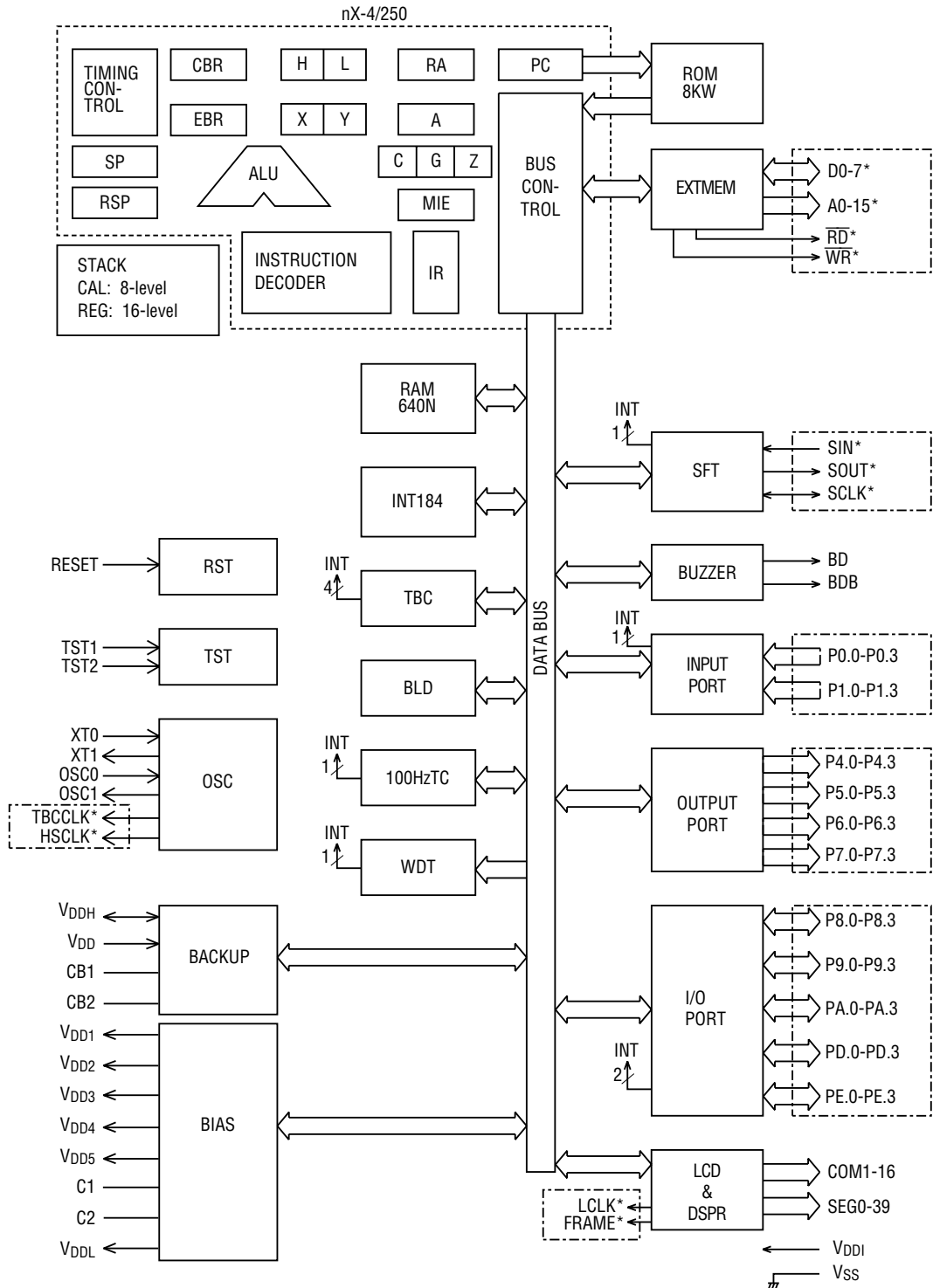
- Stack level
  - Call stack level : 8 levels
  - Register stack level : 16 levels
- I/O ports
  - Input ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
  - Output ports: Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Input-output ports: Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input  
Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
  - Can be interfaced with external peripherals that use a different power supply than this device uses.
  - Number of ports:
    - Input port : 2 ports × 4 bits
    - Output port : 4 ports × 4 bits
    - Input-output port : 5 ports × 4 bits
- Buzzer function
  - Buzzer output : 0.946 to 5.461 kHz (adjustable in 15 steps)
  - Buzzer output modes : Intermittent sound 1, 2; simple sound; continuous sound
- LCD driver
  - Number of segments : 640 Max. (40 SEG × 16 COM)
  - 1/1 to 1/16 duty
  - 1/4 or 1/5 bias (regulator built-in)
  - Selectable as all-on mode/all-off mode/power down mode/normal display mode
  - Adjustable contrast
- Reset function
  - Reset through RESET pin
  - Power-on reset
  - Reset by low-speed oscillation halt
- Battery check
  - Low-voltage supply check
  - Criterion voltage : Can be selected as 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V or 2.80 ±0.30 V
- Power supply backup
  - Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
  - Watchdog timer × 1
    - Overflows in 2 sec.
  - 100 Hz timer × 1
    - Measurable in steps of 1/100 sec.
  - 15-bit time base counter × 1
    - 1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read
  
- Shift register
  - Shift clock : 1x or 1/2x system clock; external clock
  - Data length : 8 bits
  
- Interrupt sources
  - External interrupt : 3
  - Internal interrupt : 7 (watchdog timer interrupt is a nonmaskable interrupt)
  
- Operating voltage
  - When backup used : 0.9 to 2.7 V
    - (Low-speed clock operating)
    - 1.2 to 2.7 V
      - (Operating frequency: 300 to 500 kHz)
    - 1.5 to 2.7 V
      - (Operating frequency: 200 kHz to 1 MHz)
  - When backup not used : 1.8 to 5.5 V
    - (Operating frequency: 300 to 500 kHz)
    - 2.2 to 5.5 V
      - (Operating frequency: 300 kHz to 1 MHz)
    - 2.7 to 5.5 V
      - (Operating frequency: 200 kHz to 2 MHz)
  
- Package:
  - 128-pin plastic QFP (QFP128-P-1420-0.50-K) : (Product name: MSM63184B-xxxGS-K)
  - Chip : (Product name: MSM63184B-xxx)

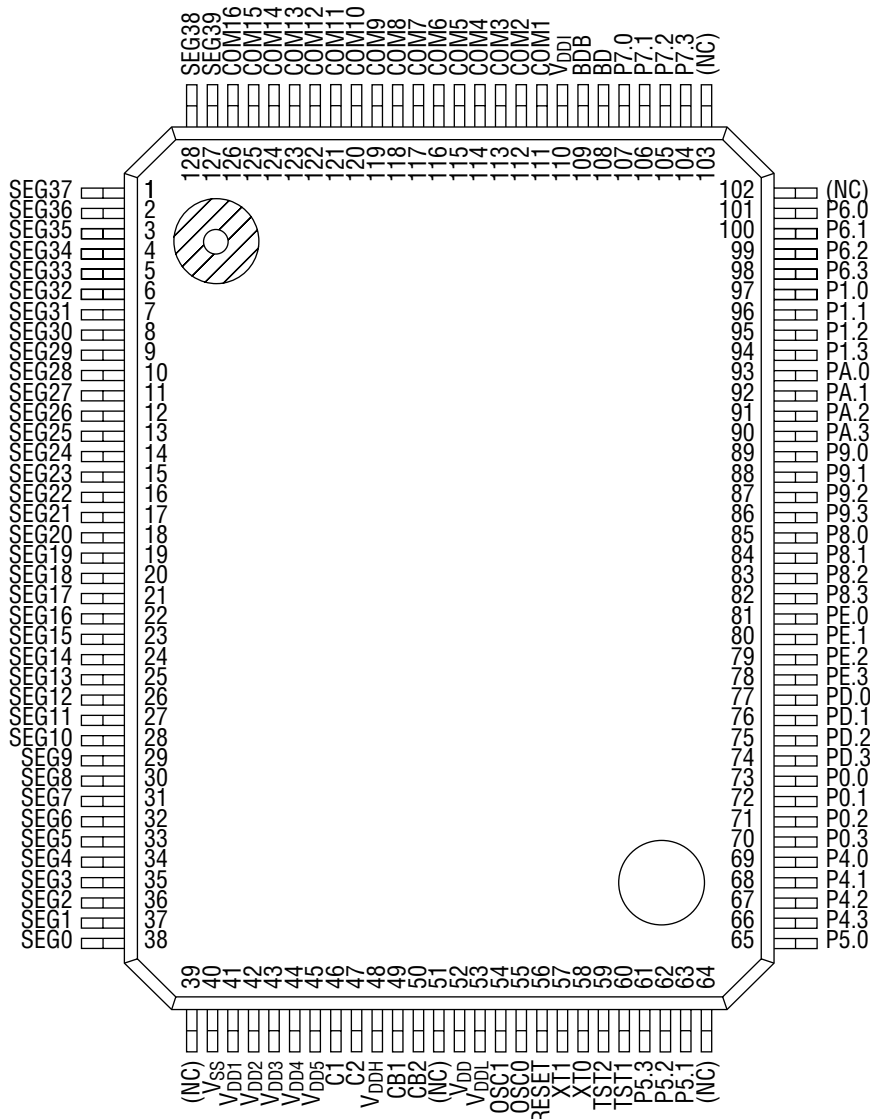
xxx indicates a code number.

### BLOCK DIAGRAM

An asterisk (\*) indicates the port secondary function.  indicates that the power is supplied to the circuits corresponding to the signal names inside  from V<sub>DDI</sub> (power supply for interface).



**PIN CONFIGURATION (TOP VIEW)**

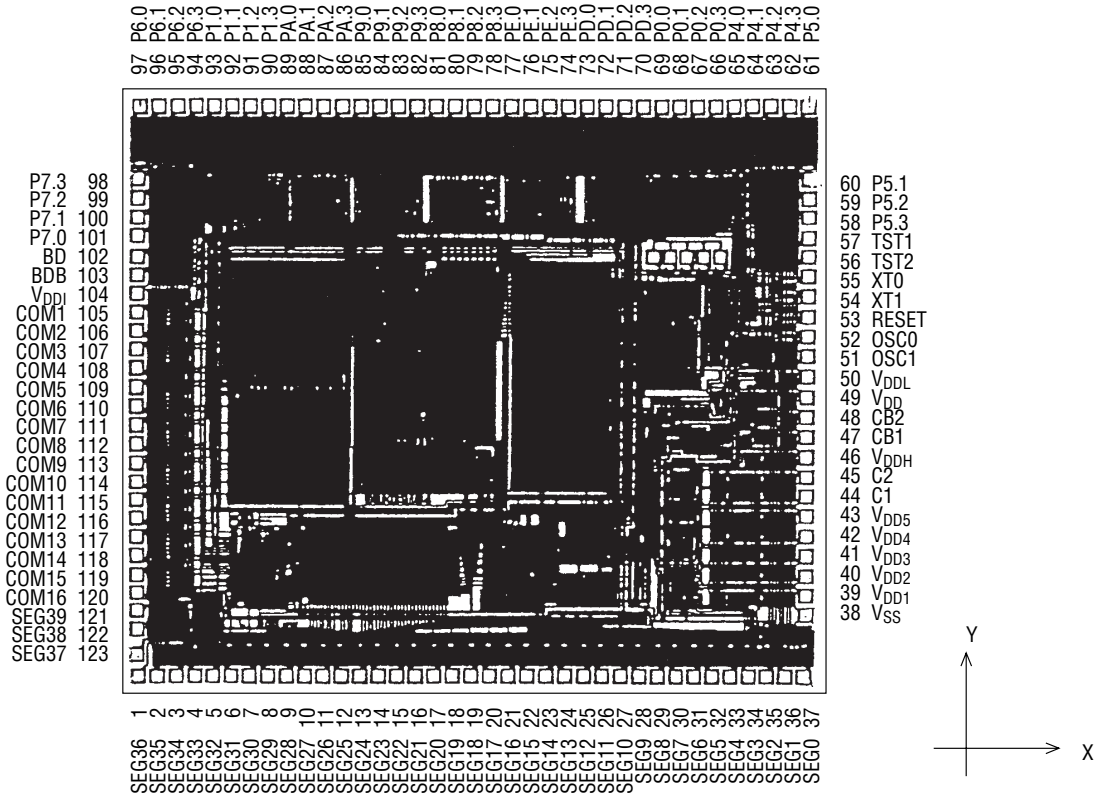


**128-Pin Plastic QFP**

Note: Pins marked as (NC) are no-connection pins which are left open.

### PAD CONFIGURATION

#### Pad Layout



- Chip Size : 5.35 mm × 4.66 mm
- Chip Thickness : 350 μm (typ.)
- Coordinate Origin : Chip center
- Pad Hole Size : 100 μm × 100 μm
- Pad Size : 110 μm × 110 μm
- Minimum Pad Pitch : 140 μm

Note: The chip substrate voltage is V<sub>SS</sub>.

## Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG36	-2520	-2135	42	V <sub>DD4</sub>	2530	-1065	83	P9.2	-560	2135
2	SEG35	-2380	-2135	43	V <sub>DD5</sub>	2530	-915	84	P9.1	-700	2135
3	SEG34	-2240	-2135	44	C1	2530	-765	85	P9.0	-840	2135
4	SEG33	-2100	-2135	45	C2	2530	-615	86	PA.3	-980	2135
5	SEG32	-1960	-2135	46	V <sub>DDH</sub>	2530	-465	87	PA.2	-1120	2135
6	SEG31	-1820	-2135	47	CB1	2530	-315	88	PA.1	-1260	2135
7	SEG30	-1680	-2135	48	CB2	2530	-165	89	PA.0	-1400	2135
8	SEG29	-1540	-2135	49	V <sub>DD</sub>	2530	-15	90	P1.3	-1540	2135
9	SEG28	-1400	-2135	50	V <sub>DDL</sub>	2530	135	91	P1.2	-1680	2135
10	SEG27	-1260	-2135	51	OSC1	2530	285	92	P1.1	-1820	2135
11	SEG26	-1120	-2135	52	OSC0	2530	435	93	P1.0	-1960	2135
12	SEG25	-980	-2135	53	RESET	2530	585	94	P6.3	-2100	2135
13	SEG24	-840	-2135	54	XT1	2530	735	95	P6.2	-2240	2135
14	SEG23	-700	-2135	55	XT0	2530	885	96	P6.1	-2380	2135
15	SEG22	-560	-2135	56	TST2	2530	1030	97	P6.0	-2520	2135
16	SEG21	-420	-2135	57	TST1	2530	1170	98	P7.3	-2530	1607
17	SEG20	-280	-2135	58	P5.3	2530	1328	99	P7.2	-2530	1467
18	SEG19	-140	-2135	59	P5.2	2530	1468	100	P7.1	-2530	1327
19	SEG18	0	-2135	60	P5.1	2530	1608	101	P7.0	-2530	1187
20	SEG17	140	-2135	61	P5.0	2520	2135	102	BD	-2530	1029
21	SEG16	280	-2135	62	P4.3	2380	2135	103	BDB	-2530	889
22	SEG15	420	-2135	63	P4.2	2240	2135	104	V <sub>DDI</sub>	-2530	749
23	SEG14	560	-2135	64	P4.1	2100	2135	105	COM1	-2530	609
24	SEG13	700	-2135	65	P4.0	1960	2135	106	COM2	-2530	469
25	SEG12	840	-2135	66	P0.3	1820	2135	107	COM3	-2530	329
26	SEG11	980	-2135	67	P0.2	1680	2135	108	COM4	-2530	189
27	SEG10	1120	-2135	68	P0.1	1540	2135	109	COM5	-2530	49
28	SEG9	1260	-2135	69	P0.0	1400	2135	110	COM6	-2530	-91
29	SEG8	1400	-2135	70	PD.3	1260	2135	111	COM7	-2530	-231
30	SEG7	1540	-2135	71	PD.2	1120	2135	112	COM8	-2530	-371
31	SEG6	1680	-2135	72	PD.1	980	2135	113	COM9	-2530	-511
32	SEG5	1820	-2135	73	PD.0	840	2135	114	COM10	-2530	-651
33	SEG4	1960	-2135	74	PE.3	700	2135	115	COM11	-2530	-791
34	SEG3	2100	-2135	75	PE.2	560	2135	116	COM12	-2530	-931
35	SEG2	2240	-2135	76	PE.1	420	2135	117	COM13	-2530	-1071
36	SEG1	2380	-2135	77	PE.0	280	2135	118	COM14	-2530	-1211
37	SEG0	2520	-2135	78	P8.3	140	2135	119	COM15	-2530	-1351
38	V <sub>SS</sub>	2530	-1665	79	P8.2	0	2135	120	COM16	-2530	-1491
39	V <sub>DD1</sub>	2530	-1515	80	P8.1	-140	2135	121	SEG39	-2530	-1631
40	V <sub>DD2</sub>	2530	-1365	81	P8.0	-280	2135	122	SEG38	-2530	-1771
41	V <sub>DD3</sub>	2530	-1215	82	P9.3	-420	2135	123	SEG37	-2530	-1970

### PIN DESCRIPTIONS

The basic functions of each pin of the MSM63184B are described in Table 1.

A symbol with a slash (/) denotes a pin that has a secondary function.

Refer to Table 2 for secondary functions.

For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

**Table 1 Pin Descriptions (Basic Functions)**

Function	Symbol	Pin	Type	Description
Power Supply	V <sub>DD</sub>	52	—	Positive power supply
	V <sub>SS</sub>	40	—	Negative power supply
	V <sub>DD1</sub>	41	—	Power supply pins for LCD bias (internally generated). Capacitors (0.1 μF) should be connected between these pins and V <sub>SS</sub> .
	V <sub>DD2</sub>	42		
	V <sub>DD3</sub>	43		
	V <sub>DD4</sub>	44		
	V <sub>DD5</sub>	45		
	C1	46		
	C2	47	—	A capacitor (0.1 μF) should be connected between C1 and C2.
	V <sub>DDI</sub>	110	—	Positive power supply pin for external interface (power supply for input, output, and input-output ports)
	V <sub>DDL</sub>	53	—	Positive power supply pin for internal logic (internally generated). A capacitor (0.1 μF) should be connected between this pin and V <sub>SS</sub> .
	V <sub>DDH</sub>	48	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor (1.0 μF) should be connected between this pin and V <sub>SS</sub> .
	CB1	49	—	Pins to connect a capacitor for voltage multiplier.
	CB2	50	—	A capacitor (1.0 μF) should be connected between CB1 and CB2.
Oscillation	XT0	58	I	Low-speed clock oscillation pins. A 32.768 kHz crystal should be connected between XT0 and XT1, and C <sub>G</sub> (5 to 25 pF) should be connected between XT0 and V <sub>SS</sub> .
	XT1	57	O	
	OSC0	55	I	High-speed clock oscillation pins. A ceramic resonator and capacitors (C <sub>LO</sub> , C <sub>L1</sub> ) or external oscillation resistor (R <sub>OS</sub> ) should be connected to these pins.
	OSC1	54	O	
Test	TST1	60	I	Input pins for testing. A pull-down resistor is internally connected to these pins.
	TST2	59	I	The user cannot use these pins.
Reset	RESET	56	I	Reset input pin. Setting this pin to "H" level puts this device into a reset state. Then, setting this pin to "L" level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Buzzer	BD	108	O	Buzzer output pin (non-inverted output)
	BDB	109	O	Buzzer output pin (inverted output)



**Table 1 Pin Descriptions (Basic Functions) (continued)**

Function	Symbol	Pin	Type	Description
Port	P0.0/INT5	73	I	4-bit input ports. Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P0.1/INT5	72		
	P0.2/INT5	71		
	P0.3/INT5	70		
	P1.0/INT5	97	I	
	P1.1/INT5	96		
	P1.2/INT5	95		
	P1.3/INT5	94		
	P4.0/A0	69	O	4-bit output ports. P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P4.1/A1	68		
	P4.2/A2	67		
	P4.3/A3	66		
	P5.0/A4	65	O	
	P5.1/A5	63		
	P5.2/A6	62		
	P5.3/A7	61	O	
	P6.0/A8	101		
	P6.1/A9	100		
	P6.2/A10	99		
	P6.3/A11	98	O	
P7.0/A12	107			
P7.1/A13	106			
P7.2/A14	105			
P7.3/A15	104			

**Table 1 Pin Descriptions (Basic Functions) (continued)**

Function	Symbol	Pin	Type	Description
Port	P8.0/ $\overline{RD}$	85	I/O	4-bit input-output ports. In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P8.1/ $\overline{WR}$	84		
	P8.2	83		
	P8.3/INT4	82		
	P9.0/D0	89	I/O	In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P9.1/D1	88		
	P9.2/D2	87		
	P9.3/D3	86		
	PA.0/D4	93	I/O	
	PA.1/D5	92		
	PA.2/D6	91		
	PA.3/D7	90		
	PD.0/FRAME	77	I/O	
	PD.1/LCLK	76		
	PD.2/TBCCLK	75		
	PD.3/HSCLK	74		
	PE.0/SIN	81	I/O	
	PE.1/SOUT	80		
PE.2/SCLK	79			
PE.3/INT2	78			

**Table 1 Pin Descriptions (Basic Functions) (continued)**

Function	Symbol	Pin	Type	Description
LCD	COM1	111	0	LCD common signal output pins
	COM2	112		
	COM3	113		
	COM4	114		
	COM5	115		
	COM6	116		
	COM7	117		
	COM8	118		
	COM9	119		
	COM10	120		
	COM11	121		
	COM12	122		
	COM13	123		
	COM14	124		
	COM15	125		
	COM16	126		
	SEG0	38	0	LCD segment signal output pins
	SEG1	37		
	SEG2	36		
	SEG3	35		
	SEG4	34		
	SEG5	33		
	SEG6	32		
	SEG7	31		
	SEG8	30		
	SEG9	29		
	SEG10	28		
	SEG11	27		
	SEG12	26		
	SEG13	25		
	SEG14	24		
	SEG15	23		
SEG16	22			
SEG17	21			
SEG18	20			
SEG19	19			
SEG20	18			
SEG21	17			
SEG22	16			
SEG23	15			
SEG24	14			

**Table 1 Pin Descriptions (Basic Functions) (continued)**

Function	Symbol	Pin	Type	Description
LCD	SEG25	13	0	LCD segment signal output pins
	SEG26	12		
	SEG27	11		
	SEG28	10		
	SEG29	9		
	SEG30	8		
	SEG31	7		
	SEG32	6		
	SEG33	5		
	SEG34	4		
	SEG35	3		
	SEG36	2		
	SEG37	1		
	SEG38	128		
	SEG39	127		

Table 2 shows the secondary functions of each pin of the MSM63184B.

**Table 2 Pin Descriptions (Secondary Functions)**

Function	Symbol	Pin	Type	Description
External Interrupt	PE.3/INT2	78	I	External 2 interrupt input pins. The change of input signal level causes an interrupt to occur.
	P8.3/INT4	82	I	External 4 interrupt input pins. The change of input signal level causes an interrupt to occur.
	P0.0/INT5	73	I	External 5 interrupt input pins. The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit.
	P0.1/INT5	72		
	P0.2/INT5	71		
	P0.3/INT5	70		
	P1.0/INT5	97		
	P1.1/INT5	96		
	P1.2/INT5	95		
	P1.3/INT5	94		
LCD External Expansion	PD.0/FRAME	77	0	Frame output pin for LCD driver expansion
	PD.1/LCLK	76	0	Clock output pin for LCD driver expansion
Oscillation Output	PD.2/TBCCLK	75	0	Low-speed oscillation clock output pin
	PD.3/HSCCLK	74	0	High-speed oscillation clock output pin
Shift Register	PE.0/SIN	81	I	Shift register receive data input pin
	PE.1/SOUT	80	0	Shift register transmit data output pin
	PE.2/SCLK	79	0	Shift register clock input-output pin. Clock output when this device is used as a master processor. Clock input when this device is used as a slave processor.

**Table 2 Pin Descriptions (Secondary Functions) (continued)**

Function	Symbol	Pin	Type	Description
External Memory	P4.0/A0	69	0	Address output bus for external memory
	P4.1/A1	68		
	P4.2/A2	67		
	P4.3/A3	66		
	P5.0/A4	65		
	P5.1/A5	63		
	P5.2/A6	62		
	P5.3/A7	61		
	P6.0/A8	101		
	P6.1/A9	100		
	P6.2/A10	99		
	P6.3/A11	98		
	P7.0/A12	107		
	P7.1/A13	106		
	P7.2/A14	105		
P7.3/A15	104			
	P9.0/D0	89	I/O	Data bus for external memory
	P9.1/D1	88		
	P9.2/D2	87		
	P9.3/D3	86		
	PA.0/D4	93		
	PA.1/D5	92		
	PA.2/D6	91		
	PA.3/D7	90		
	P8.0/ $\overline{RD}$	85	0	Read signal output pin for external memory (negative logic)
	P8.1/ $\overline{WR}$	84	0	Write signal output pin for external memory (negative logic)

**ABSOLUTE MAXIMUM RATINGS**(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V <sub>DD1</sub>	T <sub>a</sub> = 25°C	-0.3 to +1.6	V
Power Supply Voltage 2	V <sub>DD2</sub>	T <sub>a</sub> = 25°C	-0.3 to +2.9	V
Power Supply Voltage 3	V <sub>DD3</sub>	T <sub>a</sub> = 25°C	-0.3 to +4.2	V
Power Supply Voltage 4	V <sub>DD4</sub>	T <sub>a</sub> = 25°C	-0.3 to +5.5	V
Power Supply Voltage 5	V <sub>DD5</sub>	T <sub>a</sub> = 25°C	-0.3 to +6.8	V
Power Supply Voltage 6	V <sub>DD</sub>	T <sub>a</sub> = 25°C	-0.3 to +6.0	V
Power Supply Voltage 7	V <sub>DDI</sub>	T <sub>a</sub> = 25°C	-0.3 to +6.0	V
Power Supply Voltage 8	V <sub>DDH</sub>	T <sub>a</sub> = 25°C	-0.3 to +6.0	V
Power Supply Voltage 9	V <sub>DDL</sub>	T <sub>a</sub> = 25°C	-0.3 to +6.0	V
Input Voltage 1	V <sub>IN1</sub>	V <sub>DD</sub> Input, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD</sub> + 0.3	V
Input Voltage 2	V <sub>IN2</sub>	V <sub>DDI</sub> Input, T <sub>a</sub> = 25°C	-0.3 to V <sub>DDI</sub> + 0.3	V
Output Voltage 1	V <sub>OUT1</sub>	V <sub>DD1</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD1</sub> + 0.3	V
Output Voltage 2	V <sub>OUT2</sub>	V <sub>DD2</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD2</sub> + 0.3	V
Output Voltage 3	V <sub>OUT3</sub>	V <sub>DD3</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD3</sub> + 0.3	V
Output Voltage 4	V <sub>OUT4</sub>	V <sub>DD4</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD4</sub> + 0.3	V
Output Voltage 5	V <sub>OUT5</sub>	V <sub>DD5</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD5</sub> + 0.3	V
Output Voltage 6	V <sub>OUT6</sub>	V <sub>DD</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage 7	V <sub>OUT7</sub>	V <sub>DDI</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DDI</sub> + 0.3	V
Output Voltage 8	V <sub>OUT8</sub>	V <sub>DDH</sub> Output, T <sub>a</sub> = 25°C	-0.3 to V <sub>DDH</sub> + 0.3	V
Storage Temperature	T <sub>STG</sub>	—	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

- When backup is used

(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T <sub>op</sub>	—	-20 to +70	°C
Operating Voltage	V <sub>DD</sub>	—	0.9 to 2.7	V
	V <sub>DDI</sub>	—	0.9 to 5.5	V
Crystal Oscillation Frequency	f <sub>XT</sub>	—	30 to 35	kHz
Ceramic Oscillation Frequency	f <sub>CM</sub>	V <sub>DD</sub> = 1.2 to 2.7 V	300k to 500k	Hz
		V <sub>DD</sub> = 1.5 to 2.7 V	200k to 1M	
External RC Oscillator Resistance	R <sub>OS</sub>	V <sub>DD</sub> = 1.2 to 2.7 V	100 to 300	kΩ
		V <sub>DD</sub> = 1.5 to 2.7 V	50 to 300	

- When backup is not used

(V<sub>SS</sub> = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T <sub>op</sub>	—	-20 to +70	°C
Operating Voltage	V <sub>DD</sub>	—	1.8 to 5.5	V
	V <sub>DDI</sub>	—	1.8 to 5.5	V
Crystal Oscillation Frequency	f <sub>XT</sub>	—	30 to 35	kHz
Ceramic Oscillation Frequency	f <sub>CM</sub>	V <sub>DD</sub> = 1.8 to 5.5 V	300k to 500k	Hz
		V <sub>DD</sub> = 2.2 to 5.5 V	300k to 1M	
		V <sub>DD</sub> = 2.7 to 5.5 V	200k to 2M	
External RC Oscillator Resistance	R <sub>OS</sub>	V <sub>DD</sub> = 1.8 to 5.5 V	100 to 300	kΩ
		V <sub>DD</sub> = 2.2 to 5.5 V	50 to 300	
		V <sub>DD</sub> = 2.7 to 5.5 V	30 to 300	



**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

( $V_{DD} = V_{DD1} = 0.9$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
$V_{DD2}$ Voltage	$V_{DD2}$	1/5 bias, 1/4 bias ( $T_a = 25^\circ\text{C}$ )	1.7	1.8	1.9	V	1
$V_{DD2}$ Voltage Temperature Deviation	$\Delta V_{DD2}$	—	—	-4	—	mV/ $^\circ\text{C}$	
$V_{DD1}$ Voltage	$V_{DD1}$	1/5 bias, 1/4 bias	Typ.-0.2	$1/2 \times V_{DD2}$	Typ.+0.2	V	
$V_{DD3}$ Voltage	$V_{DD3}$	1/5 bias	Typ.-0.3	$3/2 \times V_{DD2}$	Typ.+0.3	V	
		1/4 bias (connect $V_{DD3}$ and $V_{DD2}$ )	Typ.-0.2	$V_{DD2}$	Typ.+0.2		
$V_{DD4}$ Voltage	$V_{DD4}$	1/5 bias	Typ.-0.4	$2 \times V_{DD2}$	Typ.+0.4	V	
		1/4 bias	Typ.-0.3	$3/2 \times V_{DD2}$	Typ.+0.3		
$V_{DD5}$ Voltage	$V_{DD5}$	1/5 bias	Typ.-0.5	$5/2 \times V_{DD2}$	Typ.+0.5	V	
		1/4 bias	Typ.-0.4	$2 \times V_{DD2}$	Typ.+0.4		
$V_{DDH}$ Voltage (Backup used)	$V_{DDH}$	High-speed clock oscillation stopped $V_{DD} = 1.5$ V	2.8	—	3.0	V	
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) $V_{DD} = 1.5$ V	2.0	—	2.7	V	
$V_{DDL}$ Voltage	$V_{DDL}$	High-speed clock oscillation stopped	1.0	1.5	2.0	V	
		High-speed clock oscillation ( $V_{DD} = 1.2$ to $5.5$ V)	1.2	—	5.5	V	
Crystal Oscillation Start Voltage	$V_{STA}$	Oscillation start time: within 5 seconds	1.0	—	—	V	
Crystal Oscillation Hold Voltage	$V_{HOLD}$	Backup	0.9	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	$T_{STOP}$	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	$C_G$	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	$C_D$	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	$C_{L0, 1}$	CSA2.00MG (Murata MFG.-make) used $V_{DD} = 3.0$ V	—	30	—	pF	
Internal RC Oscillator Capacitance	$C_{OS}$	—	8	12	16	pF	
POR Voltage	$V_{POR1}$	$V_{DD} = 1.5$ V	0.0	—	0.4	V	
		$V_{DD} = 3.0$ V	0.0	—	0.7	V	
Non-POR Voltage	$V_{POR2}$	$V_{DD} = 1.5$ V	1.2	—	1.5	V	
		$V_{DD} = 3.0$ V	2.0	—	3.0	V	

Notes: 1. " $T_{STOP}$ " indicates that if the crystal oscillator stops over the value of  $T_{STOP}$ , the system reset occurs.

2. "POR" denotes Power On Reset.

3. " $V_{POR1}$ " indicates that POR occurs when  $V_{DD}$  falls from  $V_{DD}$  to  $V_{POR1}$  and again rises up to  $V_{DD}$ .

4. " $V_{POR2}$ " indicates that POR does not occur when  $V_{DD}$  falls from  $V_{DD}$  to  $V_{POR2}$  and again rises up to  $V_{DD}$ .

**DC Characteristics (continued)**

- When backup is used

( $V_{DD} = V_{DD1} = 1.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU is in HALT state. (High-speed clock oscillation stopped)	—	7.0	35	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	—	5.5	30	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU is in operating state. (High-speed clock oscillation stopped)	—	24	40	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU is in operation at high-speed oscillation (RC oscillation, $R_{OS} = 51\text{ k}\Omega$ )	—	600	800	$\mu\text{A}$	
Supply Current 5	$I_{DD5}$	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)	—	700	900	$\mu\text{A}$	

- When backup is not used

( $V_{DD} = V_{DD1} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	$I_{DD1}$	CPU is in HALT state. (High-speed clock oscillation stopped)	—	3.0	20	$\mu\text{A}$	1
Supply Current 2	$I_{DD2}$	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	—	2.0	18	$\mu\text{A}$	
Supply Current 3	$I_{DD3}$	CPU is in operating state. (High-speed clock oscillation stopped)	—	11	20	$\mu\text{A}$	
Supply Current 4	$I_{DD4}$	CPU is in operation at high-speed oscillation (RC oscillation, $R_{OS} = 51\text{ k}\Omega$ )	—	450	600	$\mu\text{A}$	
Supply Current 5	$I_{DD5}$	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)	—	850	1000	$\mu\text{A}$	

DC Characteristics (continued)

( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Output Current 1 (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (PD.0 to PD.3) (PE.0 to PE.3)	$I_{OH1}$	$V_{OH1} = V_{DD1} - 0.5\text{ V}$	$V_{DD1} = 1.5\text{ V}$	-2.0	-1.2	-0.2	mA	2
			$V_{DD1} = 3.0\text{ V}$	-5.0	-3.0	-1.0	mA	
			$V_{DD1} = 5.0\text{ V}$	-8.0	-4.0	-1.5	mA	
	$I_{OL1}$	$V_{OL1} = 0.5\text{ V}$	$V_{DD1} = 1.5\text{ V}$	0.2	1.2	2.0	mA	
			$V_{DD1} = 3.0\text{ V}$	1.0	3.0	5.0	mA	
			$V_{DD1} = 5.0\text{ V}$	1.5	4.0	8.0	mA	
Output Current 2 (BD, BDB)	$I_{OH2}$	$V_{OH2} = V_{DD} - 0.7\text{ V}$	$V_{DD} = 1.5\text{ V}$	-2.5	-1.3	-0.4	mA	
			$V_{DD} = 3.0\text{ V}$	-6.0	-4.0	-2.0	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-9.0	-5.5	-3.0	mA	
	$I_{OL2}$	$V_{OL2} = 0.7\text{ V}$	$V_{DD} = 1.5\text{ V}$	0.4	1.3	2.5	mA	
			$V_{DD} = 3.0\text{ V}$	2.0	4.0	6.0	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	3.0	5.5	9.0	mA	
Output Current 3 (SEG0 to SEG39) (COM1 to COM16)	$I_{OH3}$	$V_{OH3} = V_{DD5} - 0.2\text{ V}$ ( $V_{DD5}$ level)	—	—	-4	$\mu\text{A}$		
	$I_{OHM3}$	$V_{OHM3} = V_{DD4} + 0.2\text{ V}$ ( $V_{DD4}$ level)	4	—	—	$\mu\text{A}$		
	$I_{OHM3S}$	$V_{OHM3S} = V_{DD4} - 0.2\text{ V}$ ( $V_{DD4}$ level)	—	—	-4	$\mu\text{A}$		
	$I_{OMH3}$	$V_{OMH3} = V_{DD3} + 0.2\text{ V}$ ( $V_{DD3}$ level)	4	—	—	$\mu\text{A}$		
	$I_{OMH3S}$	$V_{OMH3S} = V_{DD3} - 0.2\text{ V}$ ( $V_{DD3}$ level)	—	—	-4	$\mu\text{A}$		
	$I_{OML3}$	$V_{OML3} = V_{DD2} + 0.2\text{ V}$ ( $V_{DD2}$ level)	4	—	—	$\mu\text{A}$		
	$I_{OML3S}$	$V_{OML3S} = V_{DD2} - 0.2\text{ V}$ ( $V_{DD2}$ level)	—	—	-4	$\mu\text{A}$		
	$I_{OLM3}$	$V_{OLM3} = V_{DD1} + 0.2\text{ V}$ ( $V_{DD1}$ level)	4	—	—	$\mu\text{A}$		
	$I_{OLM3S}$	$V_{OLM3S} = V_{DD1} - 0.2\text{ V}$ ( $V_{DD1}$ level)	—	—	-4	$\mu\text{A}$		
	$I_{OL3}$	$V_{OL3} = V_{SS} + 0.2\text{ V}$ ( $V_{SS}$ level)	4	—	—	$\mu\text{A}$		
Output Current 4 (OSC1)	$I_{OH4R}$	$V_{OH4R} = V_{DDH} - 0.5\text{ V}$ (RC oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-2.5	-1.5	-0.75	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-3.5	-2.0	-1.0	mA	
	$I_{OL4R}$	$V_{OL4R} = 0.5\text{ V}$ (RC oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.75	1.5	2.5	mA	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	1.0	2.0	3.5	mA	
	$I_{OH4C}$	$V_{OH4C} = V_{DDH} - 0.5\text{ V}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-300	-180	-60	$\mu\text{A}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-450	-280	-100	$\mu\text{A}$	
	$I_{OL4C}$	$V_{OL4C} = 0.5\text{ V}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	60	120	300	$\mu\text{A}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	100	200	450	$\mu\text{A}$	
Output Leakage (P4.0 to P4.3) (P5.0 to P5.3) (P6.0 to P6.3) ⋮ (PE.0 to PE.3)	$I_{OOH}$	$V_{OH} = V_{DD1}$	—	—	0.3	$\mu\text{A}$		
	$I_{OOL}$	$V_{OL} = V_{SS}$	-0.3	—	—	$\mu\text{A}$		

**DC Characteristics (continued)**

( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

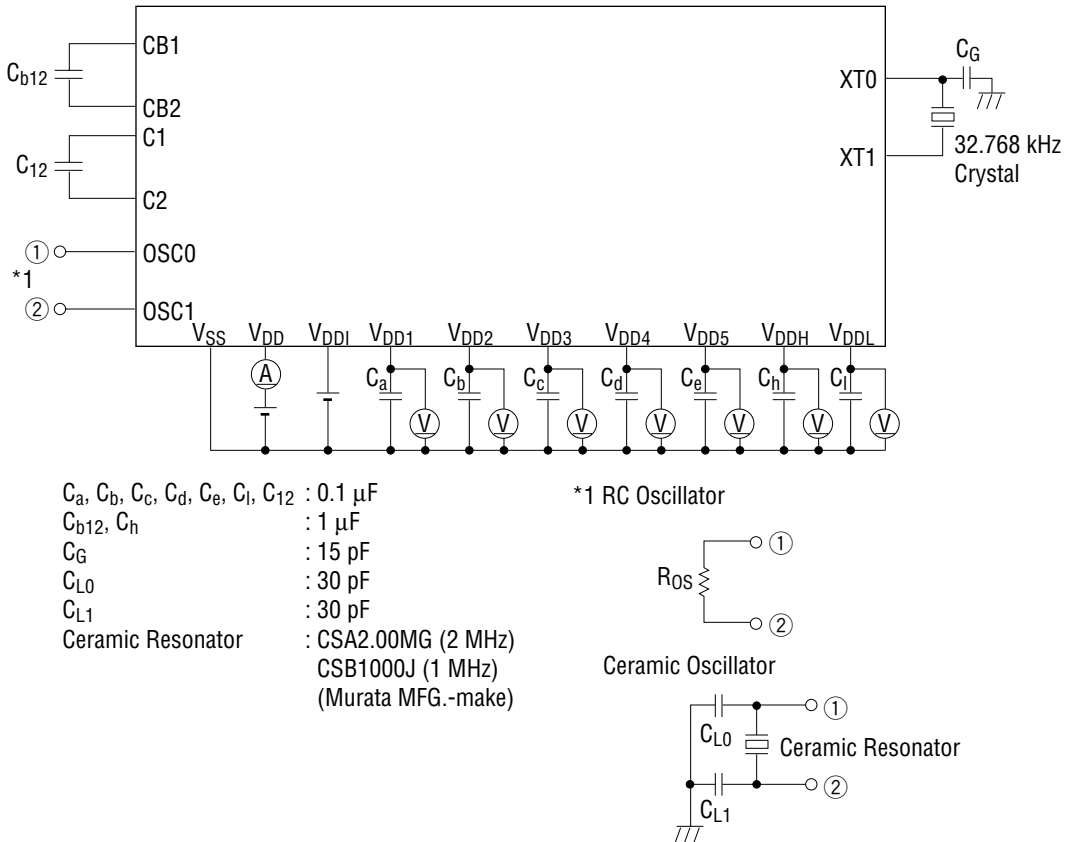
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PE.0 to PE.3)	$I_{IH1}$	$V_{IH1} = V_{DD1}$ (when pulled down)	$V_{DD1} = 1.5\text{ V}$	2	10	30	$\mu\text{A}$	3
			$V_{DD1} = 3.0\text{ V}$	30	90	180	$\mu\text{A}$	
			$V_{DD1} = 5.0\text{ V}$	70	250	600	$\mu\text{A}$	
	$I_{IL1}$	$V_{IL1} = V_{SS}$ (when pulled up)	$V_{DD1} = 1.5\text{ V}$	-30	-10	-2	$\mu\text{A}$	
			$V_{DD1} = 3.0\text{ V}$	-180	-90	-30	$\mu\text{A}$	
			$V_{DD1} = 5.0\text{ V}$	-600	-250	-70	$\mu\text{A}$	
	$I_{IH1Z}$	$V_{IH1} = V_{DD1}$ (in a high impedance state)	0.0	—	1.0	$\mu\text{A}$		
$I_{IL1Z}$	$V_{IL1} = V_{SS}$ (in a high impedance state)	-1.0	—	0.0	$\mu\text{A}$			
Input Current 2 (OSCO)	$I_{IL2}$	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-200	-110	-30	$\mu\text{A}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	-600	-350	-150	$\mu\text{A}$	
	$I_{IH2R}$	$V_{IH2R} = V_{DDH}$ (RC oscillation)	0.0	—	1.0	$\mu\text{A}$		
	$I_{IL2R}$	$V_{IL2R} = V_{SS}$ (RC oscillation)	-1.0	—	0.0	$\mu\text{A}$		
	$I_{IH2C}$	$V_{IH2C} = V_{DDH}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.1	0.5	1.0	$\mu\text{A}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.75	1.5	3.0	$\mu\text{A}$	
	$I_{IL2C}$	$V_{IL2C} = V_{SS}$ (ceramic oscillation)	$V_{DD} = V_{DDH} = 3.0\text{ V}$	-1.0	-0.5	-0.1	$\mu\text{A}$	
$V_{DD} = V_{DDH} = 5.0\text{ V}$			-3.0	-1.5	-0.75	$\mu\text{A}$		
Input Current 3 (RESET)	$I_{IH3}$	$V_{IH3} = V_{DD}$	$V_{DD} = 1.5\text{ V}$	10	50	80	$\mu\text{A}$	
			$V_{DD} = 3.0\text{ V}$	150	350	600	$\mu\text{A}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.5	1.0	2.0	$\text{mA}$	
	$I_{IL3}$	$V_{IL3} = V_{SS}$	-1.0	—	0.0	$\mu\text{A}$		
Input Current 4 (TST1, TST2)	$I_{IH4}$	$V_{IH4} = V_{DD}$	$V_{DD} = 1.5\text{ V}$	50	150	300	$\mu\text{A}$	
			$V_{DD} = 3.0\text{ V}$	0.5	1.0	1.5	$\text{mA}$	
			$V_{DD} = V_{DDH} = 5.0\text{ V}$	1.25	2.5	4.0	$\text{mA}$	
	$I_{IL4}$	$V_{IL4} = V_{SS}$	-1.0	—	0.0	$\mu\text{A}$		

DC Characteristics (continued)

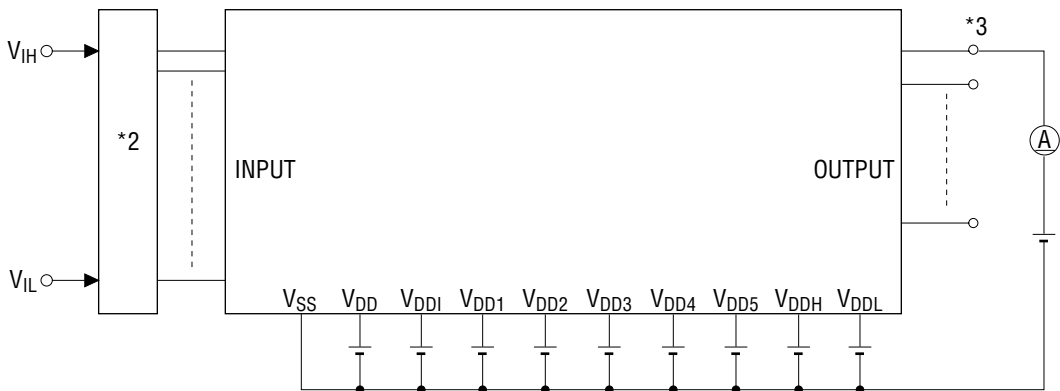
( $V_{DD} = V_{DD1} = V_{DDH} = 3.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{DD1} = 1.1\text{ V}$ ,  $V_{DD2} = 2.2\text{ V}$ ,  $V_{DD3} = 3.3\text{ V}$ ,  $V_{DD4} = 4.4\text{ V}$ ,  $V_{DD5} = 5.5\text{ V}$ ,  $T_a = -20\text{ to }+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PE.0 to PE.3)	$V_{IH1}$	$V_{DD1} = 1.5\text{ V}$	1.2	—	1.5	V	4
		$V_{DD1} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD1} = 5.0\text{ V}$	4.0	—	5.0	V	
	$V_{IL1}$	$V_{DD1} = 1.5\text{ V}$	0.0	—	0.3	V	
		$V_{DD1} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD1} = 5.0\text{ V}$	0.0	—	1.0	V	
Input Voltage 2 (OSCO)	$V_{IH2}$	$V_{DD} = V_{DDH} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	4.0	—	5.0	V	
	$V_{IL2}$	$V_{DD} = V_{DDH} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2)	$V_{IH3}$	$V_{DD} = 1.5\text{ V}$	1.35	—	1.5	V	
		$V_{DD} = 3.0\text{ V}$	2.4	—	3.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	4.0	—	5.0	V	
	$V_{IL3}$	$V_{DD} = 1.5\text{ V}$	0.0	—	0.15	V	
		$V_{DD} = 3.0\text{ V}$	0.0	—	0.6	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.0	—	1.0	V	
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PE.0 to PE.3)	$\Delta V_{T1}$	$V_{DD1} = 1.5\text{ V}$	0.05	0.1	0.3	V	
		$V_{DD1} = 3.0\text{ V}$	0.2	0.5	1.0	V	
		$V_{DD1} = 5.0\text{ V}$	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	$\Delta V_{T2}$	$V_{DD} = 1.5\text{ V}$	0.05	0.1	0.3	V	
		$V_{DD} = 3.0\text{ V}$	0.2	0.5	1.0	V	
		$V_{DD} = V_{DDH} = 5.0\text{ V}$	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) (P9.0 to P9.3) ⋮ (PD.0 to PD.3) (PE.0 to PE.3)	$C_{IN}$	—	—	—	5	pF	1

Measuring circuit 1



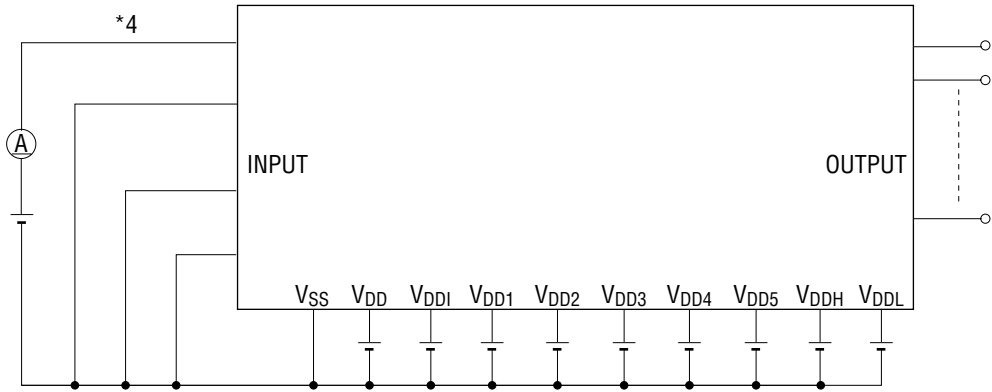
Measuring circuit 2



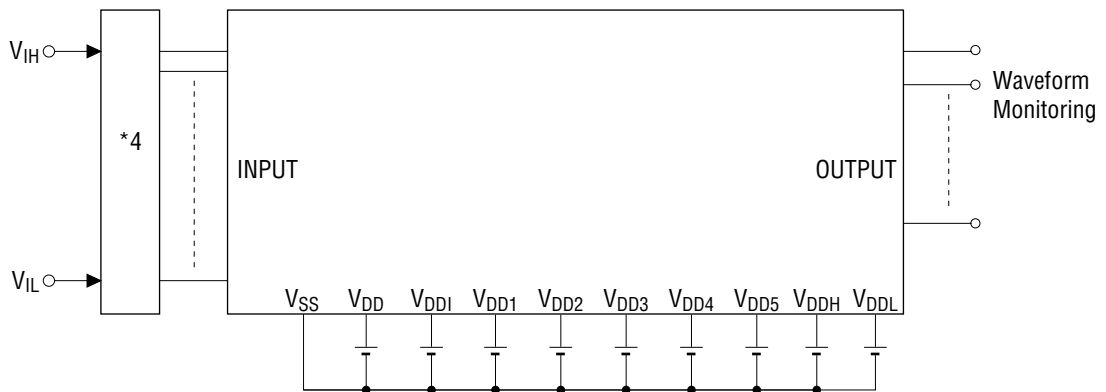
\*2 Input logic circuit to determine the specified measuring conditions.

\*3 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



\*4 Measured at the specified input pins.

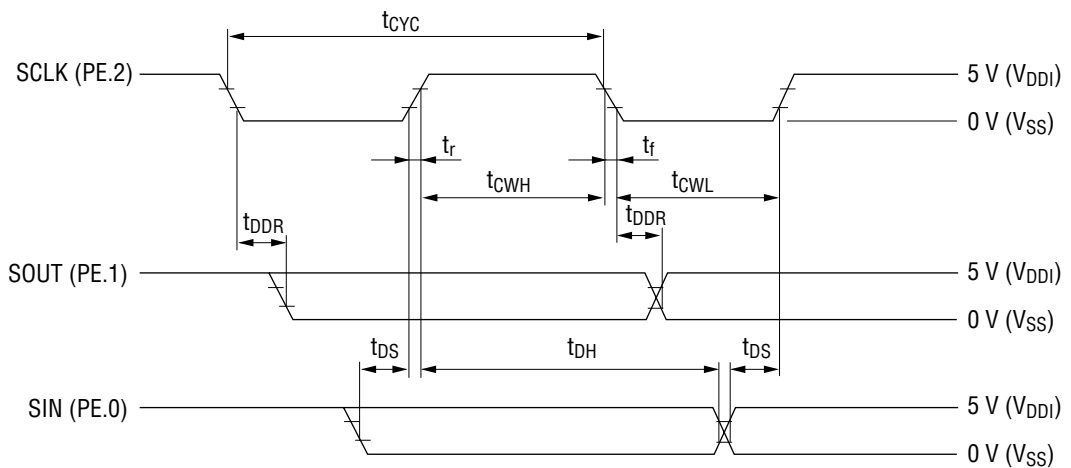
**AC Characteristics (Serial Interface, Shift Register)**

( $V_{DD} = 0.9$  to  $5.5$  V,  $V_{DDH} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{DDI} = 5.0$  V,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	$t_f$	—	—	—	1.0	$\mu\text{s}$
SCLK Input Rise Time	$t_r$	—	—	—	1.0	$\mu\text{s}$
SCLK Input "L" Level Pulse Width	$t_{CWL}$	—	0.8	—	—	$\mu\text{s}$
SCLK Input "H" Level Pulse Width	$t_{CWH}$	—	0.8	—	—	$\mu\text{s}$
SCLK Input Cycle Time	$t_{CYC}$	$V_{DDI} = 5$ V to $V_{DD}$	1.8	—	—	$\mu\text{s}$
SCLK Output Cycle Time	$t_{CYC1(0)}$	CPU in operation state at 32 kHz	—	30.5	—	$\mu\text{s}$
	$t_{CYC2(0)}$	CPU in operation at 2 MHz $V_{DD} = V_{DDH} = 2.7$ V to $5.5$ V	—	0.5	—	$\mu\text{s}$
SOUT Output Delay Time	$t_{DDR}$	$C_l = 10$ pF	—	—	0.4	$\mu\text{s}$
SIN Input Setup Time	$t_{DS}$	—	0.5	—	—	$\mu\text{s}$
SIN Input Hold Time	$t_{DH}$	—	0.8	—	—	$\mu\text{s}$

AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)





**AC Characteristics (External Memory Interface)**

( $V_{DD} = 0.9$  to  $5.5$  V,  $V_{DDH} = 1.8$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{DDI} = 5.0$  V,  $T_a = -20$  to  $+70^\circ\text{C}$  unless otherwise specified)

(1) Reading from External Memory

(a) When CPU operates at 32.768 kHz

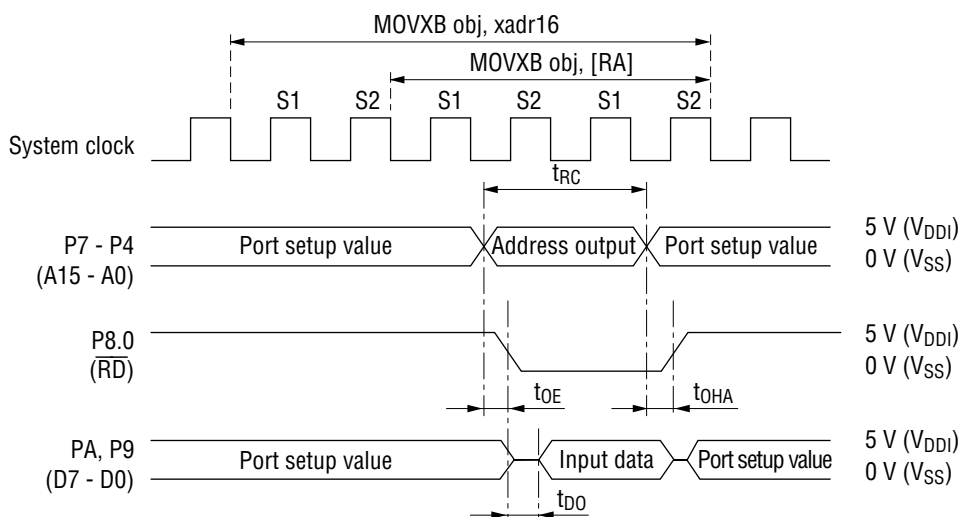
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	$t_{RC}$	—	—	61.0	—	$\mu\text{s}$
$\overline{\text{RD}}$ Output Delay Time	$t_{OE}$	—	—	—	5.0	$\mu\text{s}$
Output Valid Time	$t_{OHA}$	—	—	—	5.0	$\mu\text{s}$
External Memory Output Delay Time	$t_{DO}$	—	—	—	5.0	$\mu\text{s}$

(b) When CPU operates at 2 MHz ( $V_{DDH} = 2.7$  to  $5.5$  V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	$t_{RC}$	—	1.0	—	—	$\mu\text{s}$
$\overline{\text{RD}}$ Output Delay Time	$t_{OE}$	—	—	—	100	ns
Output Valid Time	$t_{OHA}$	—	—	—	100	ns
External Memory Output Delay Time	$t_{DO}$	—	—	—	150	ns

AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



(2) Writing to External Memory

(a) When CPU operates at 32.768 kHz

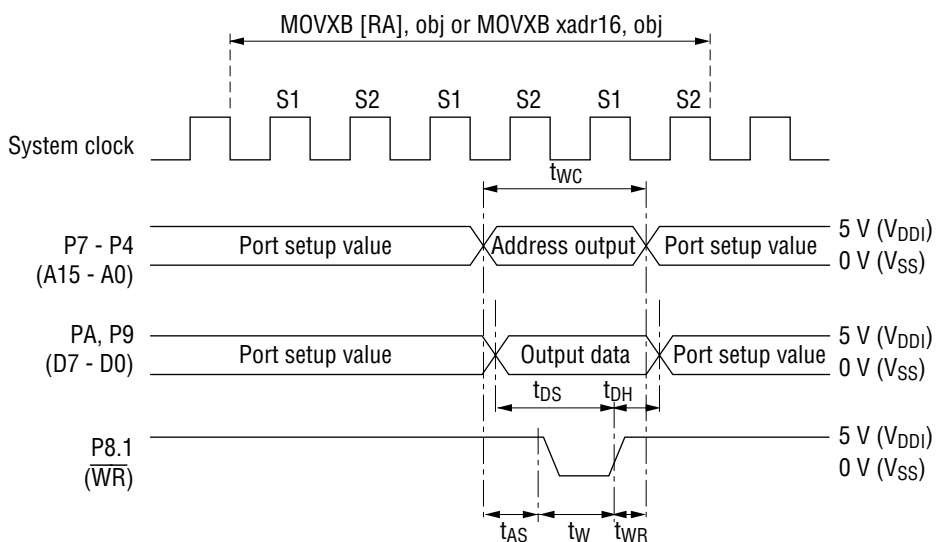
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	$t_{WC}$	—	—	61.0	—	$\mu\text{s}$
Address Setup Time	$t_{AS}$	—	—	30.5	—	$\mu\text{s}$
Write Time	$t_W$	—	—	15.3	—	$\mu\text{s}$
Write Recovery Time	$t_{WR}$	—	—	15.3	—	$\mu\text{s}$
Data Setup Time	$t_{DS}$	—	—	45.8	—	$\mu\text{s}$
Data Hold Time	$t_{DH}$	—	—	15.3	—	$\mu\text{s}$

(b) When CPU operates at 2 MHz ( $V_{DDH} = 2.7$  to  $5.5$  V)

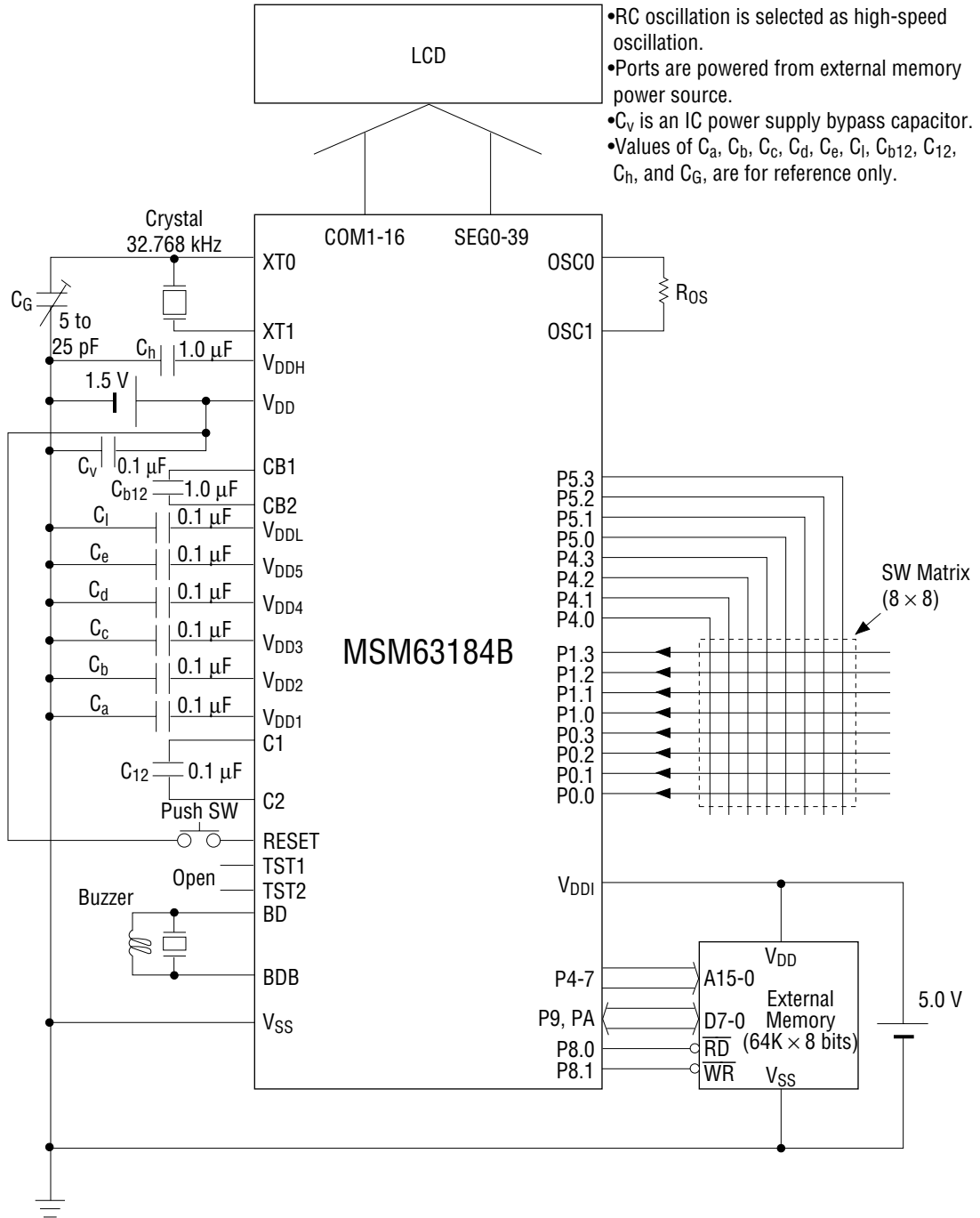
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	$t_{WC}$	—	1.0	—	—	$\mu\text{s}$
Address Setup Time	$t_{AS}$	—	0.4	—	—	$\mu\text{s}$
Write Time	$t_W$	—	0.2	—	—	$\mu\text{s}$
Write Recovery Time	$t_{WR}$	—	0.2	—	—	$\mu\text{s}$
Data Setup Time	$t_{DS}$	—	0.7	—	—	$\mu\text{s}$
Data Hold Time	$t_{DH}$	—	0.2	—	—	$\mu\text{s}$

AC characteristics timing

("H" level = 4.0 V, "L" level = 1.0 V)



APPLICATION CIRCUITS

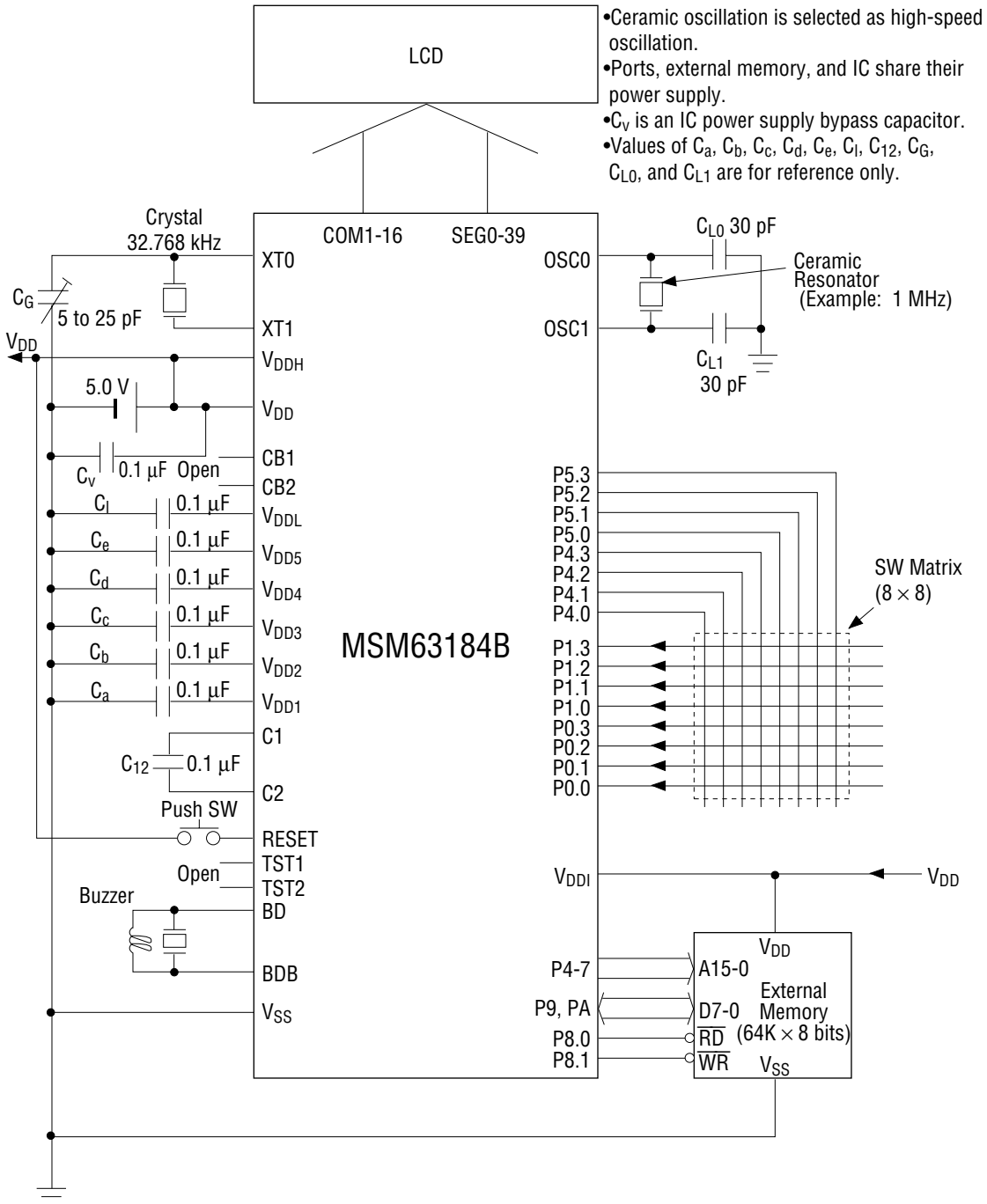


- RC oscillation is selected as high-speed oscillation.
- Ports are powered from external memory power source.
- C<sub>v</sub> is an IC power supply bypass capacitor.
- Values of C<sub>a</sub>, C<sub>b</sub>, C<sub>c</sub>, C<sub>d</sub>, C<sub>e</sub>, C<sub>1</sub>, C<sub>b12</sub>, C<sub>12</sub>, C<sub>h</sub>, and C<sub>G</sub>, are for reference only.

Note: V<sub>DDI</sub> is the power supply pin for the input, output, and input-output ports. Be sure to connect the V<sub>DDI</sub> pin either to the positive power supply pin (V<sub>DD</sub>) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with Power Supply Backup

APPLICATION CIRCUITS (continued)

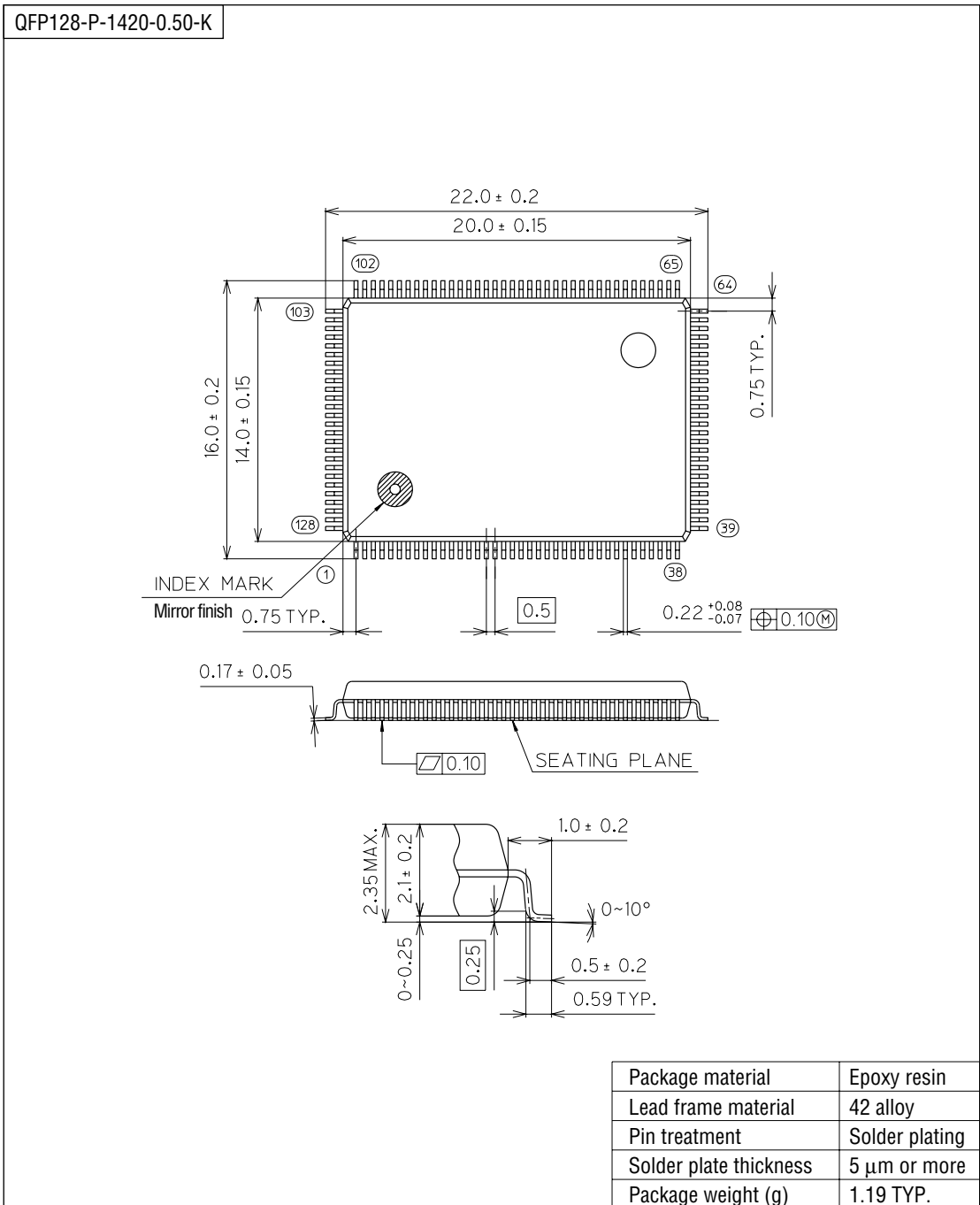


Note:  $V_{DDI}$  is the power supply pin for the input, output, and input-output ports. Be sure to connect the  $V_{DDI}$  pin either to the positive power supply pin ( $V_{DD}$ ) of this device or to the positive power supply pin of the external memory.

Application Circuit Example with No Power Supply Backup

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).