This version : Dec. 2000

# OKI Semiconductor

# MSM514800D/DSL

**524,288-Word x 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE**

## DESCRIPTION

The MSM514800D/DSL is a 524,288-word × 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM514800D/DSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM514800D/DSL is available in a 28-pin plastic SOJ. The MSM514800DSL (the self-refresh and lower-power version) is specially designed for lower-power applications.

## FEATURES

- 524,288-word × 8-bit configuration
- Single 5V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 1,024 cycles/16 ms, 1,024 cycles/128 ms (SL Version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
- Package options:

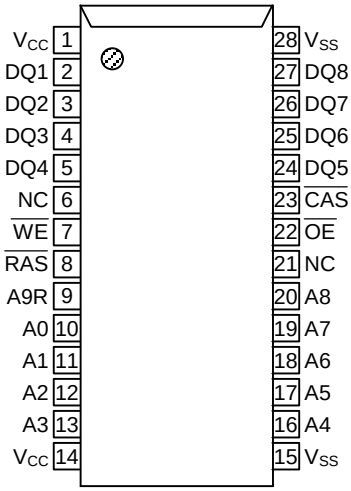
  28-pin 400mil plastic SOJ (SOJ28-P-400-1.27) (Product : MSM514800D/DSL-xxJS)

  xx : indicates speed rank.

## PRODUCT FAMILY

| Family | Access Time (Max.) | | | | Cycle Time (Min.) | Power Dissipation | |
|---|---|---|---|---|---|---|---|
| | $t_{RAC}$ | $t_{AA}$ | $t_{CAC}$ | $t_{OEA}$ | | Operating (Max.) | Standby (Max.) |
| MSM514800D/DSL | 60ns | 30ns | 20ns | 20ns | 110ns | 660mW | 5.5mW/ 1.1mW (SL Version) |
| | 70ns | 35ns | 20ns | 20ns | 130ns | 605mW | |

## PIN CONFIGRATION (TOP VIEW)

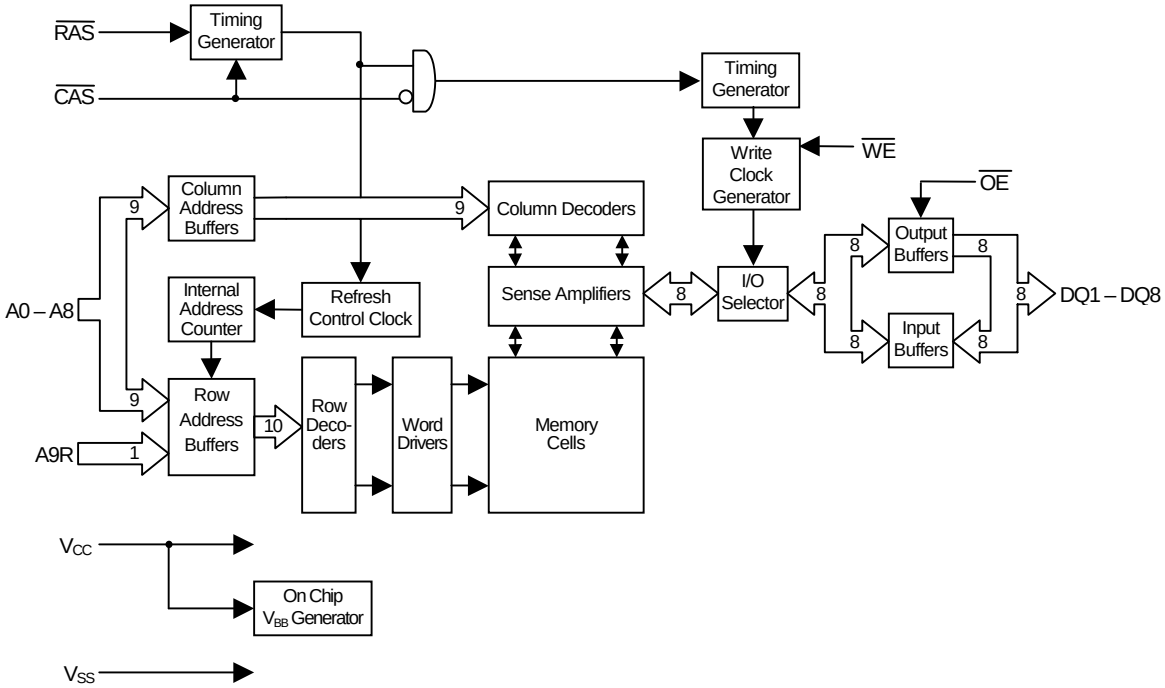



28-Pin Plastic SOJ

| Pin Name | Function |
|---|---|
| A0 - A8, A9R | Address Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| DQ1 – DQ8 | Data Input/Data Output |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{CC}$ | Power Supply (5V) |
| $V_{SS}$ | Ground (0V) |
| NC | No Connection |

Note : The same power supply voltage must be provided to every $V_{CC}$ pin, and the same GND voltage level must be provided to every $V_{SS}$ pin.

## BLOCK DIAGRAM



# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$ | –1.0 to 7.0 | V |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_{D*}$ | 1 | W |
| Operating Temperature | $T_{opr}$ | 0 to 70 | °C |
| Storage Temperature | $T_{stg}$ | –55 to 150 | °C |

*: Ta = 25°C

## Recommended Operating Conditions

(Ta = 0°C to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | — | 6.5 *1 | V |
| Input Low Voltage | $V_{IL}$ | –1.0 *2 | — | 0.8 | V |

Notes: *1. The input voltage is $V_{CC}$ + 2.0V when the pulse width is less than 20ns (the pulse width is with respect to the point at which $V_{CC}$ is applied).

*2. The input voltage is $V_{SS}$ − 2.0V when the pulse width is less than 20ns (the pulse width is with respect to the point at which $V_{SS}$ is applied).

## Capacitance

($V_{CC}$ = 5V ± 10%, Ta = 25°C, f=1MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance (A0 – A8, A9R) | $C_{IN1}$ | — | 7 | pF |
| Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) | $C_{IN2}$ | — | 7 | pF |
| Output Capacitance (DQ1 – DQ8) | $C_{I/O}$ | — | 8 | pF |

## DC Characteristics

($V_{CC}$ = 5V ± 10%, Ta = 0°C to 70°C)

| Parameter | Symbol | Condition | MSM514800 D/DSL-60 | | MSM514800 D/DSL-70 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = –5.0mA | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.2mA | 0 | 0.4 | 0 | 0.4 | V | |
| Input Leakage Current | $I_{LI}$ | 0V ≤ $V_I$ ≤ 6.5V ; All other pins not under test = 0V | –10 | 10 | –10 | 10 | µA | |
| Output Leakage Current | $I_{LO}$ | DQ disable 0V ≤ $V_O$ ≤ 5.5V | –10 | 10 | –10 | 10 | µA | |
| Average Power Supply Current (Operating) | $I_{CC1}$ | $\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC}$ = Min. | — | 120 | — | 110 | mA | 1,2 |
| Power Supply Current (Standby) | $I_{CC2}$ | $\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$ | — | 2 | — | 2 | mA | 1 |
| | | $\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2V | — | 1 | — | 1 | | |
| | | | — | 200 | — | 200 | µA | 1,5 |
| Average Power Supply Current ($\overline{RAS}$-only Refresh) | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CAS}$ = $V_{IH}$, $t_{RC}$ = Min. | — | 120 | — | 110 | mA | 1,2 |
| Power Supply Current (Standby) | $I_{CC5}$ | $\overline{RAS}$ = $V_{IH}$, $\overline{CAS}$ = $V_{IL}$, DQ = enable | — | 5 | — | 5 | mA | 1 |
| Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $I_{CC6}$ | $\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$ | — | 120 | — | 110 | mA | 1,2 |
| Average Power Supply Current (Fast Page Mode) | $I_{CC7}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ cycling, $t_{PC}$ = Min. | — | 110 | — | 100 | mA | 1,3 |
| Average Power Supply Current (Battery Backup) | $I_{CC10}$ | $t_{RC}$ = 125µs, $\overline{CAS}$ before $\overline{RAS}$, $t_{RAS}$ ≤ 1µs | — | 300 | — | 300 | µA | 1,4,5 |
| Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $I_{CCS}$ | $\overline{RAS}$ ≤ 0.2V, $\overline{CAS}$ ≤ 0.2V | — | 300 | — | 300 | µA | 1,5 |

Notes: 1. $I_{CC}$ Max. is specified as $I_{CC}$ for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. The address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.
4. $V_{CC}$ – 0.2V ≤ $V_{IH}$ ≤ 6.5V, – 1.0V ≤ $V_{IL}$ ≤ 0.2V.
5. SL version.

## AC Characteristic (1/2)

($V_{CC}$ = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

| Parameter | Symbol | MSM514800 D/DSL-60 | | MSM514800 D/DSL-70 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 110 | — | 130 | — | ns | |
| Read Modify Write Cycle Time | $t_{RWC}$ | 155 | — | 185 | — | ns | |
| Fast Page Mode Cycle Time | $t_{PC}$ | 40 | — | 45 | — | ns | |
| Fast Page Mode Read Modify Write Cycle Time | $t_{PRWC}$ | 85 | — | 100 | — | ns | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 60 | — | 70 | ns | 4,5,6 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 20 | — | 20 | ns | 4,5 |
| Access Time from Column Address | $t_{AA}$ | — | 30 | — | 35 | ns | 4,6 |
| Access Time from $\overline{CAS}$ Precharge | $t_{CPA}$ | — | 35 | — | 40 | ns | 4 |
| Access Time from $\overline{OE}$ | $t_{OEA}$ | — | 20 | — | 20 | ns | 4 |
| Output Low Impedance Time from $\overline{CAS}$ | $t_{CLZ}$ | 0 | — | 0 | — | ns | 4 |
| $\overline{CAS}$ to Data Output Buffer Turn-off Delay Time | $t_{OFF}$ | 0 | 15 | 0 | 20 | ns | 7 |
| $\overline{OE}$ to Data Output Buffer Turn-off Delay Time | $t_{OEZ}$ | 0 | 15 | 0 | 20 | ns | 7 |
| Transition Time | $t_T$ | 3 | 50 | 3 | 50 | ns | 3 |
| Refresh Period | $t_{REF}$ | — | 16 | — | 16 | ms | |
| Refresh Period | $t_{REF}$ | — | 128 | — | 128 | ms | 11 |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 40 | — | 50 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{RAS}$ Pulse Width (Fast Page Mode) | $t_{RASP}$ | 60 | 100,000 | 70 | 100,000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 15 | — | 20 | — | ns | |
| $\overline{RAS}$ Hold Time referenced to $\overline{OE}$ | $t_{ROH}$ | 15 | — | 20 | — | ns | |
| $\overline{CAS}$ Precharge Time (Fast Page Mode) | $t_{CP}$ | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 20 | 10,000 | 20 | 10,000 | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 60 | — | 70 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | $t_{RHCP}$ | 35 | — | 40 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 40 | 20 | 50 | ns | 5 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns | 6 |
| Row Address Set-up Time | $t_{ASR}$ | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | ns | |

## AC Characteristic (2/2)

($V_{CC}$ = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

| Parameter | Symbol | MSM514800 D/DSL-60 | | MSM514800 D/DSL-70 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Column Address Set-up Time | $t_{ASC}$ | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CAH}$ | 10 | — | 15 | — | ns | |
| Column Address Hold Time from $\overline{RAS}$ | $t_{AR}$ | 50 | — | 55 | — | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 30 | — | 35 | — | ns | |
| Read Command Set-up Time | $t_{RCS}$ | 0 | — | 0 | — | ns | |
| Read Command Hold Time | $t_{RCH}$ | 0 | — | 0 | — | ns | 8 |
| Read Command Hold Time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | ns | 8 |
| Write Command Set-up Time | $t_{WCS}$ | 0 | — | 0 | — | ns | 9 |
| Write Command Hold Time | $t_{WCH}$ | 15 | — | 15 | — | ns | |
| Write Command Hold Time from $\overline{RAS}$ | $t_{WCR}$ | 50 | — | 55 | — | | |
| Write Command Pulse Width | $t_{WP}$ | 15 | — | 15 | — | ns | |
| $\overline{OE}$ Command Hold Time | $t_{OEH}$ | 15 | — | 20 | — | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 15 | — | 20 | — | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 15 | — | 20 | — | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | — | 0 | — | ns | 10 |
| Data-in Hold Time | $t_{DH}$ | 15 | — | 15 | — | ns | 10 |
| Data-in Hold Time from $\overline{RAS}$ | $t_{DHR}$ | 50 | — | 55 | — | | |
| $\overline{OE}$ to Data-in Delay Time | $t_{OED}$ | 15 | — | 20 | — | ns | |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 40 | — | 50 | — | ns | 9 |
| Column Address to WE Delay Time | $t_{AWD}$ | 60 | — | 65 | — | ns | 9 |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 90 | — | 100 | — | ns | 9 |
| $\overline{CAS}$ Precharge $\overline{WE}$ Delay Time | $t_{CPWD}$ | 65 | — | 70 | — | ns | 9 |
| $\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge | $t_{RPC}$ | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CSR}$ | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$) | $t_{CHR}$ | 15 | — | 15 | — | ns | |
| $\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{RASS}$ | 100 | — | 100 | — | µs | 11 |
| $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{RPS}$ | 110 | — | 130 | — | ns | 11 |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh) | $t_{CHS}$ | –40 | — | –50 | — | ns | 11 |

Notes:

1. A start-up delay of 200μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume $t_T$ = 5ns.

3. $V_{IH}$ (Min.) and $V_{IL}$ (Max.) are reference levels for measuring input timing signals. Transition times ($t_T$) are measured between $V_{IH}$ and $V_{IL}$.

4. This parameter is measured with a load circuit equivalent to 2 TTL load and 100pF.

5. Operation within the $t_{RCD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RCD}$ (Max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (Max.) limit, then the access time is controlled by $t_{CAC}$.

6. Operation within the $t_{RAD}$ (Max.) limit ensures that $t_{RAC}$ (Max.) can be met. $t_{RAD}$ (Max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (Max.) limit, then the access time is controlled by $t_{AA}$.

7. $t_{OFF}$ (Max.) and $t_{OEZ}$ (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.

8. $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

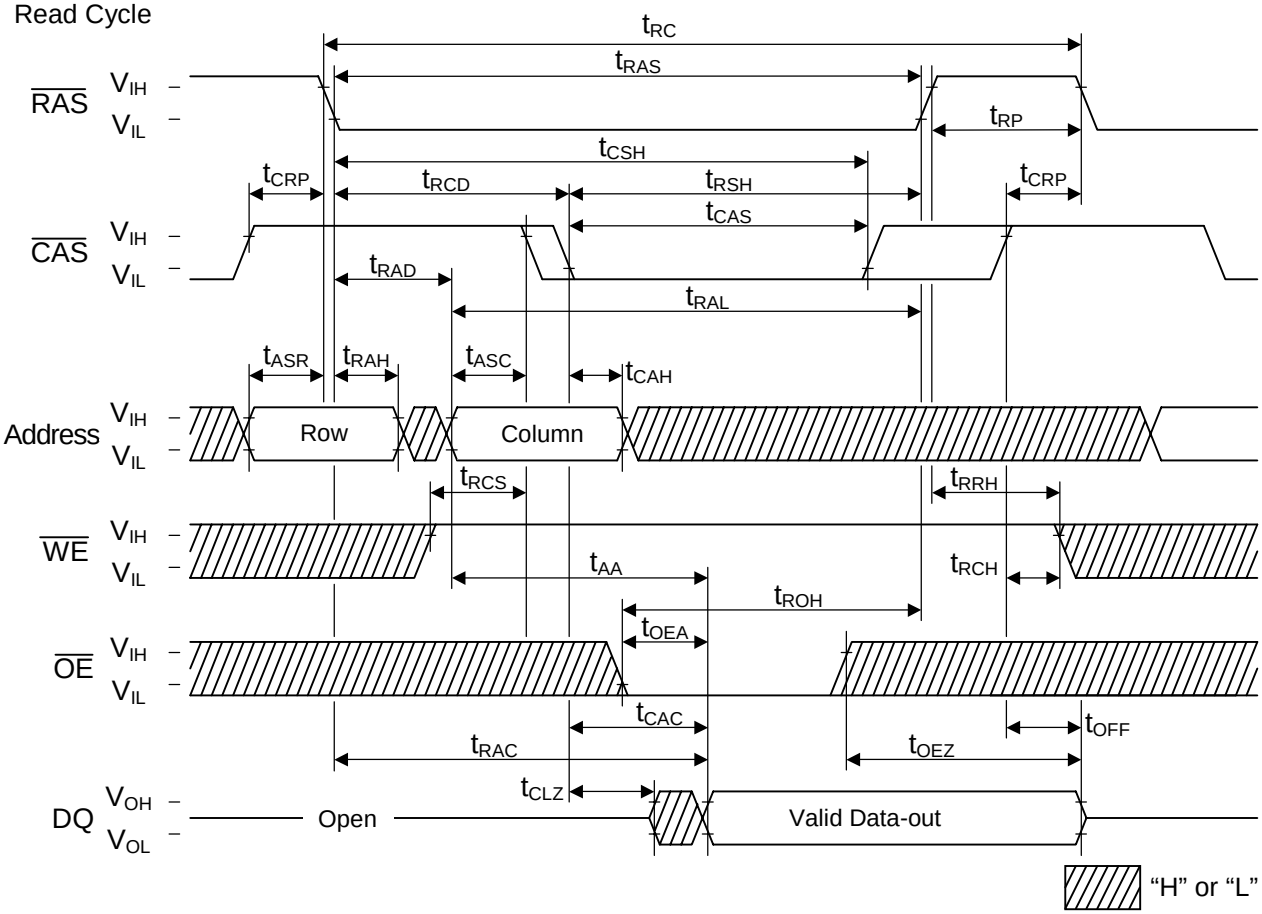
9. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to the $\overline{CAS}$, leading edges in an early write cycle, and to the $\overline{WE}$ leading edge in an $\overline{OE}$ control write cycle, or a read modify write cycle.

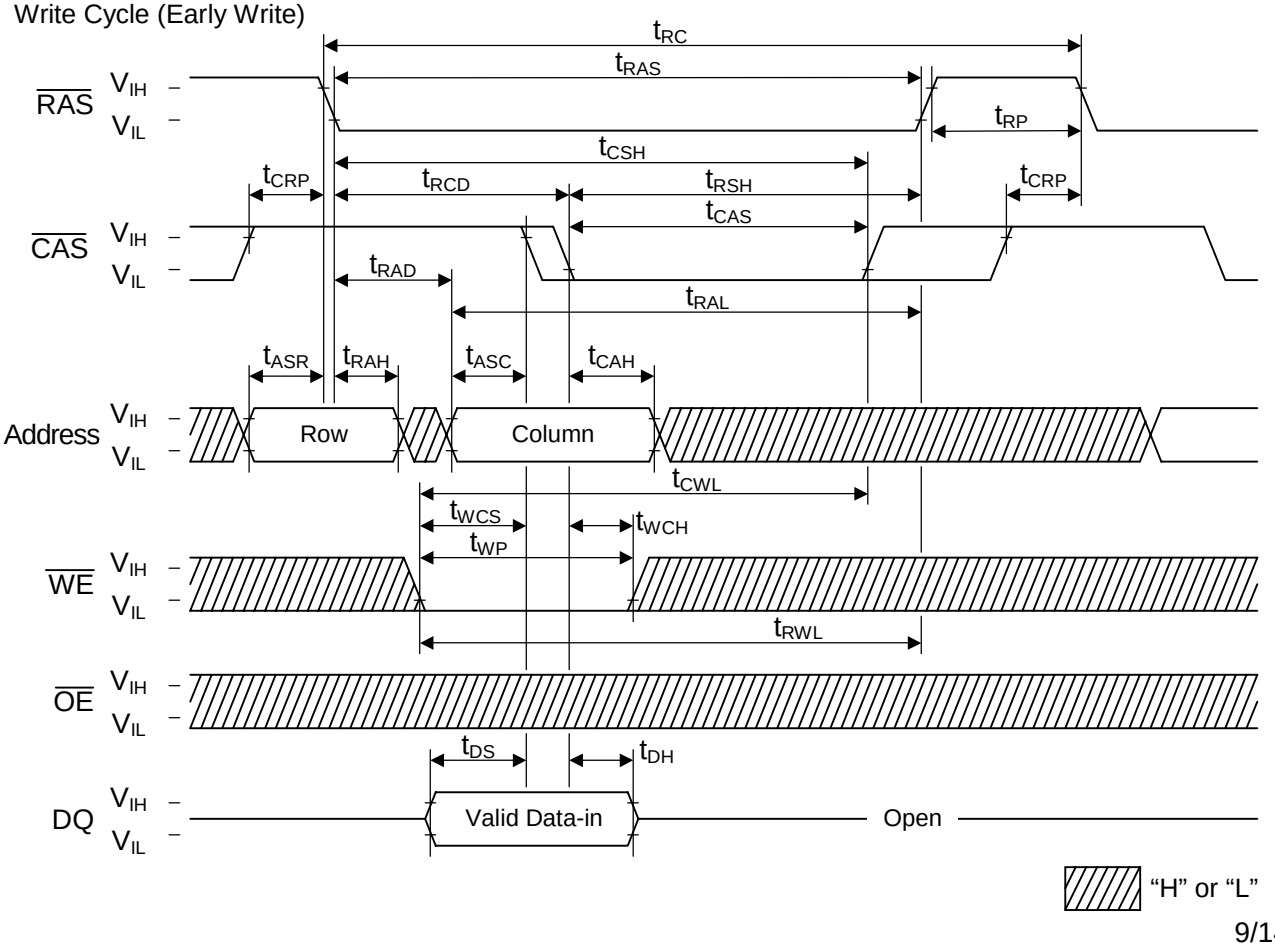
11. SL version only.

## Timing Chart

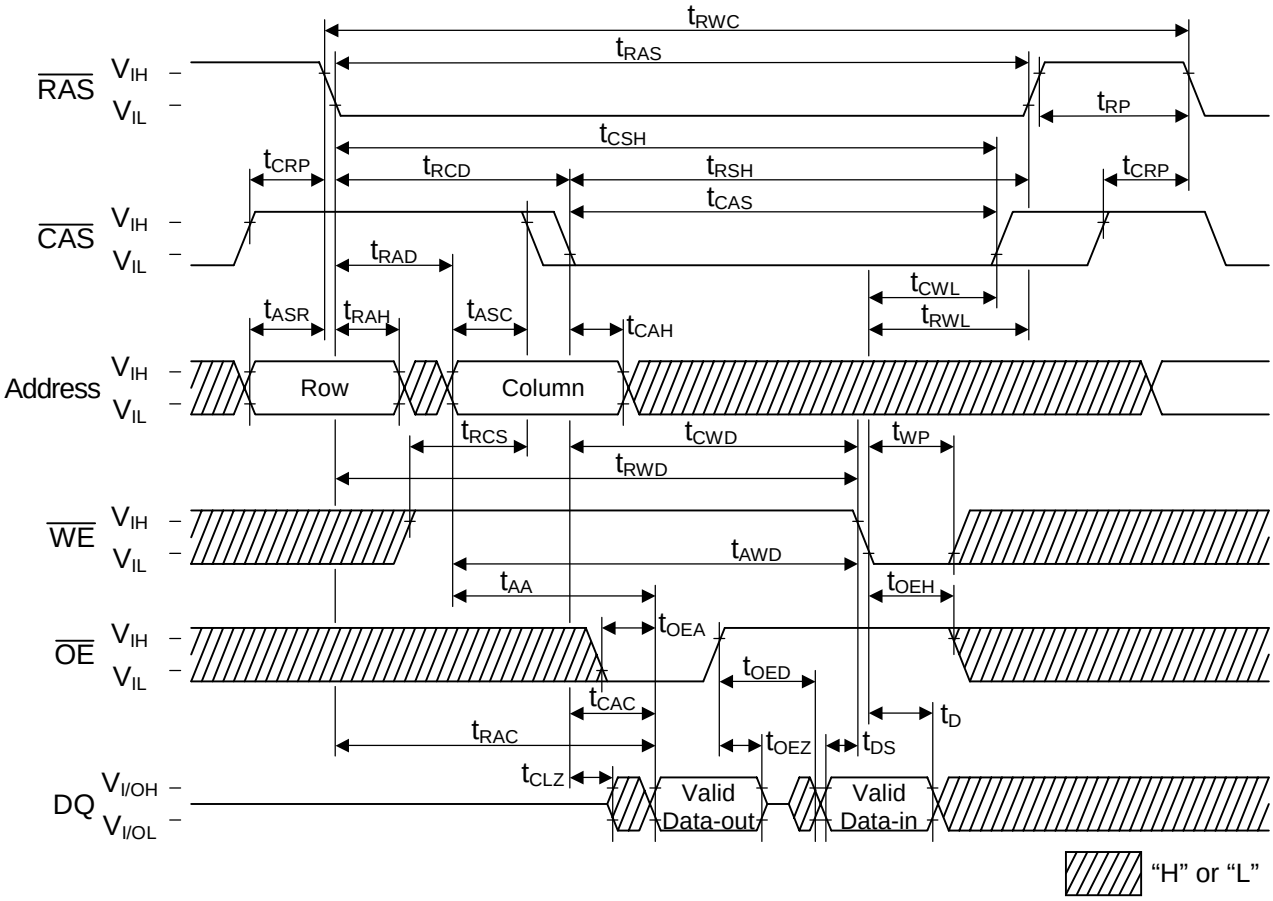
- Read Cycle



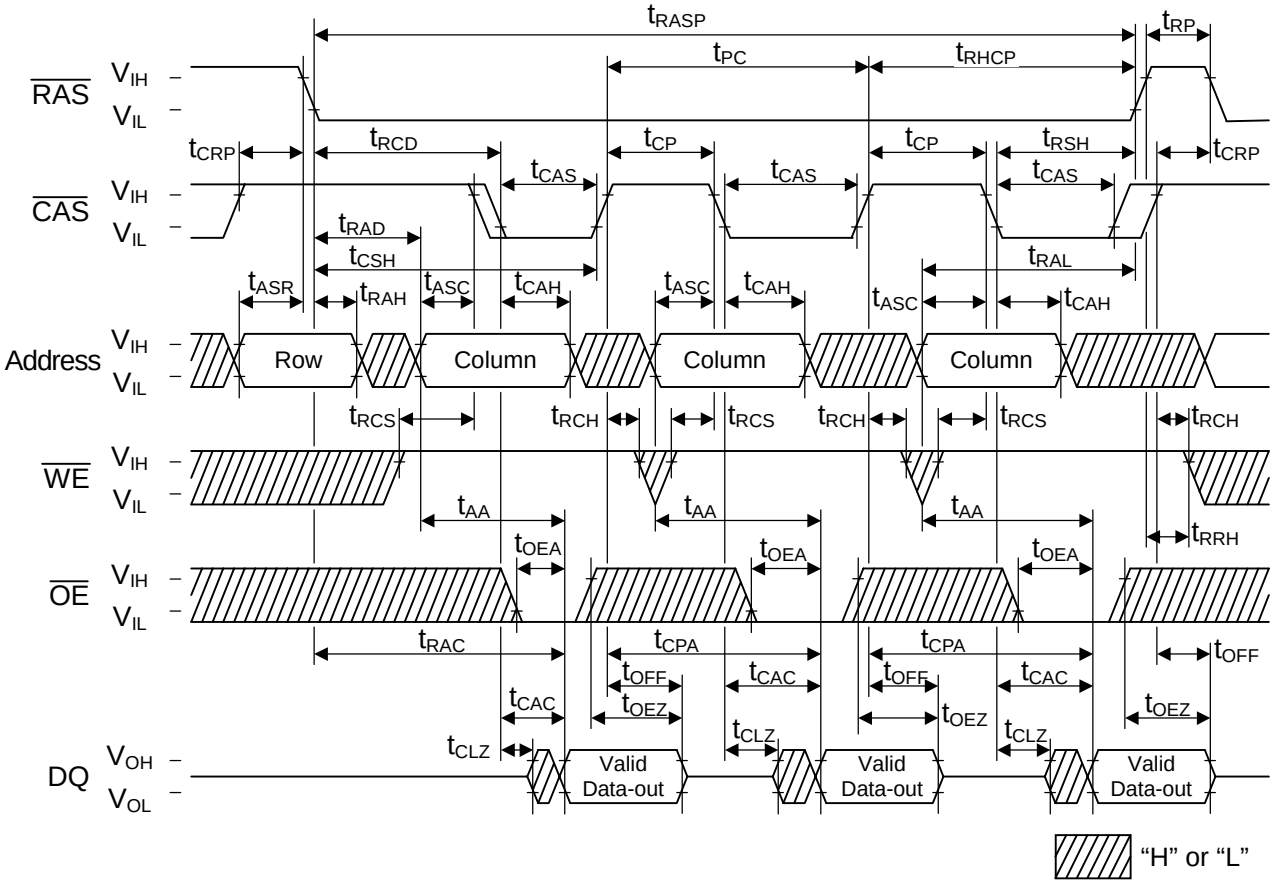

- Write Cycle (Early Write)



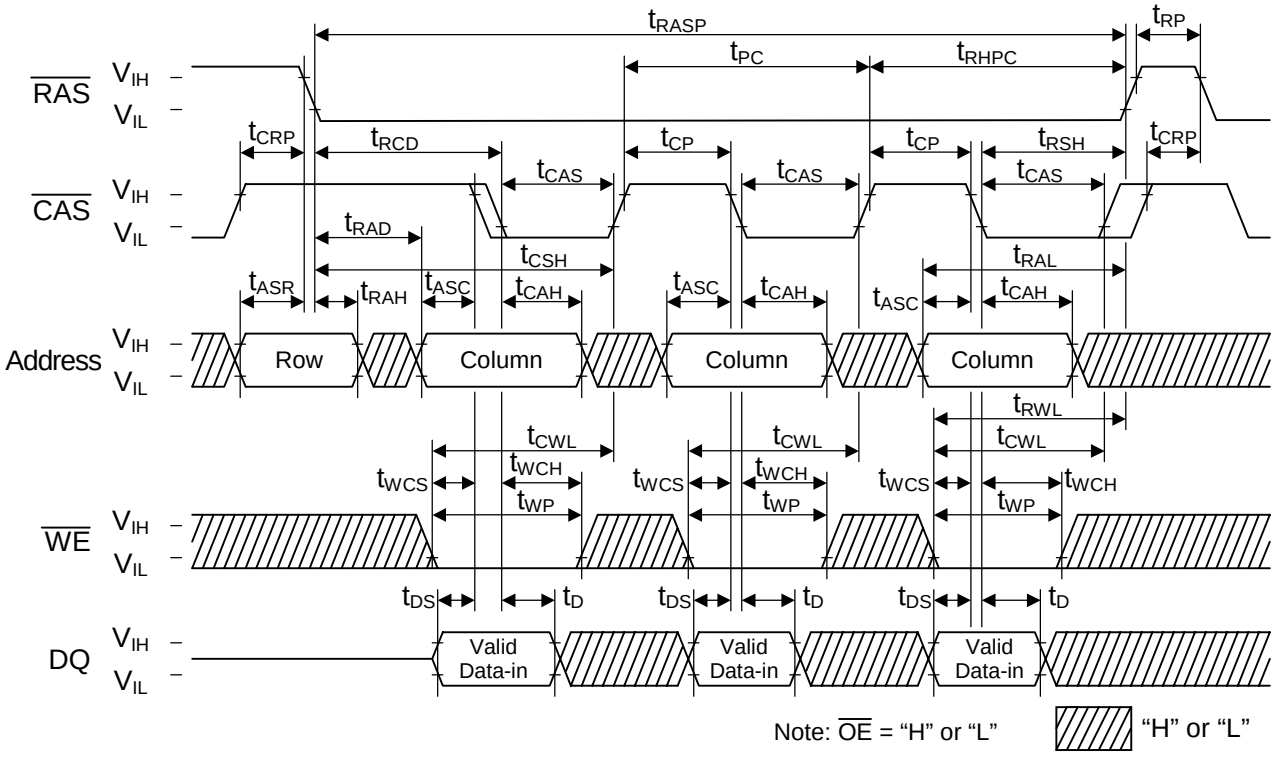
- Read Modify Write Cycle



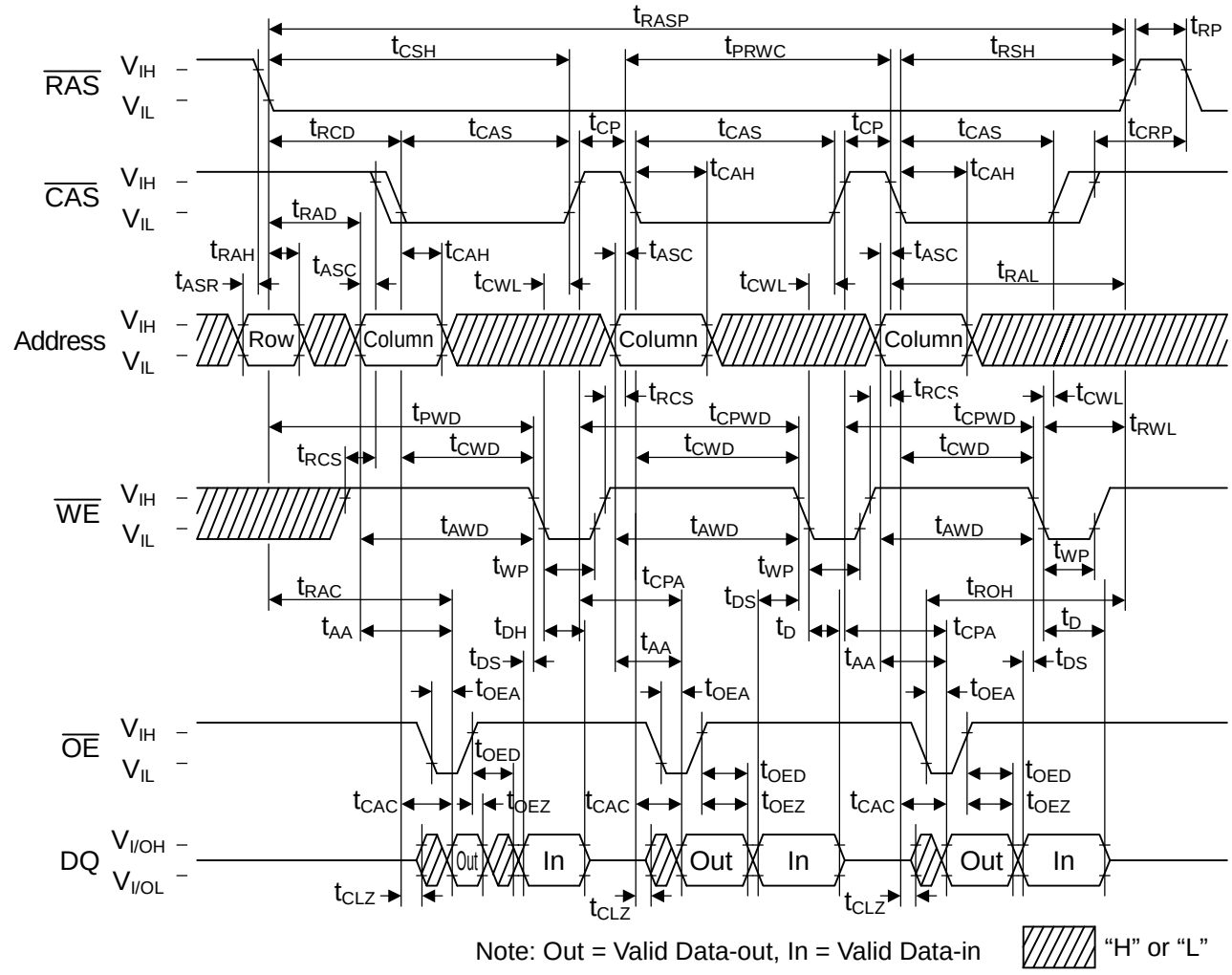
- Fast Page Mode Read Cycle



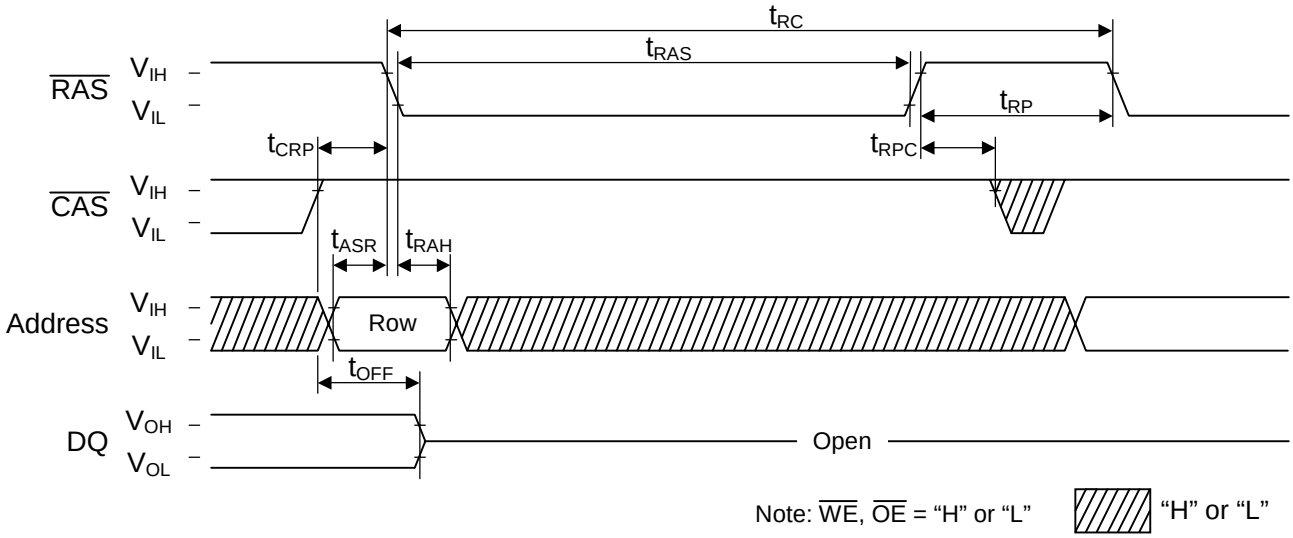

- Fast Page Mode Write Cycle (Early Write)



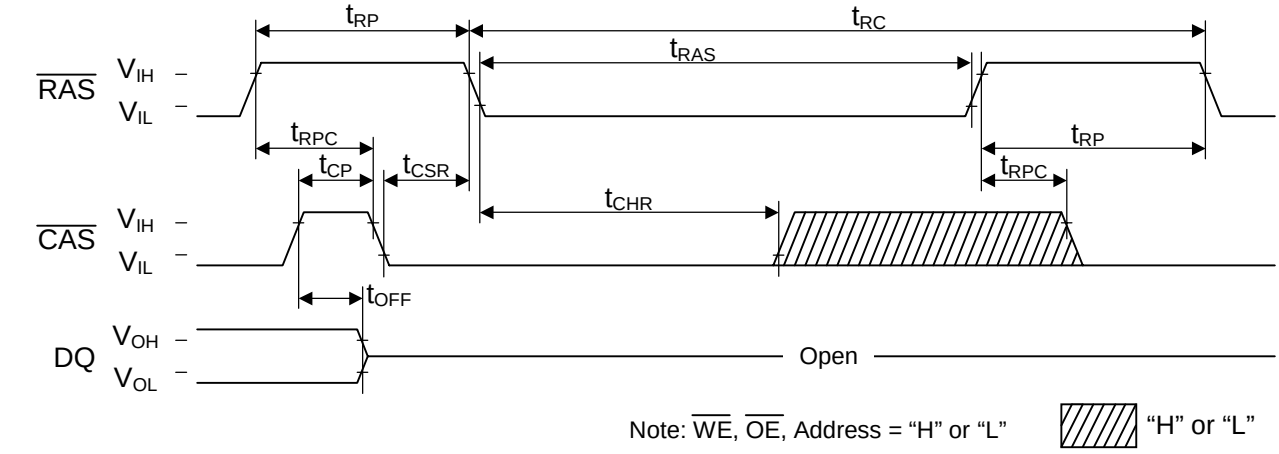
- Fast Page Mode Read Modify Write Cycle



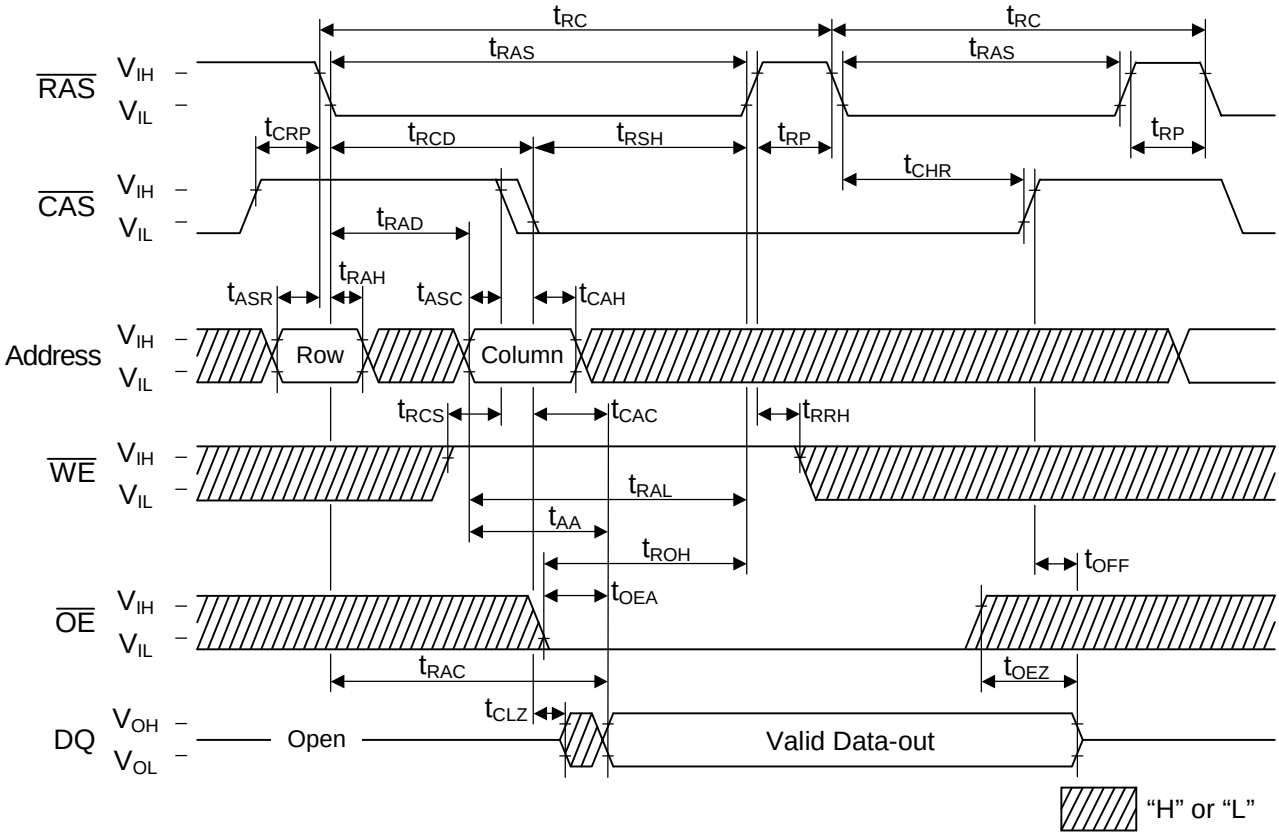

- $\overline{\text{RAS}}$-only Refresh Cycle



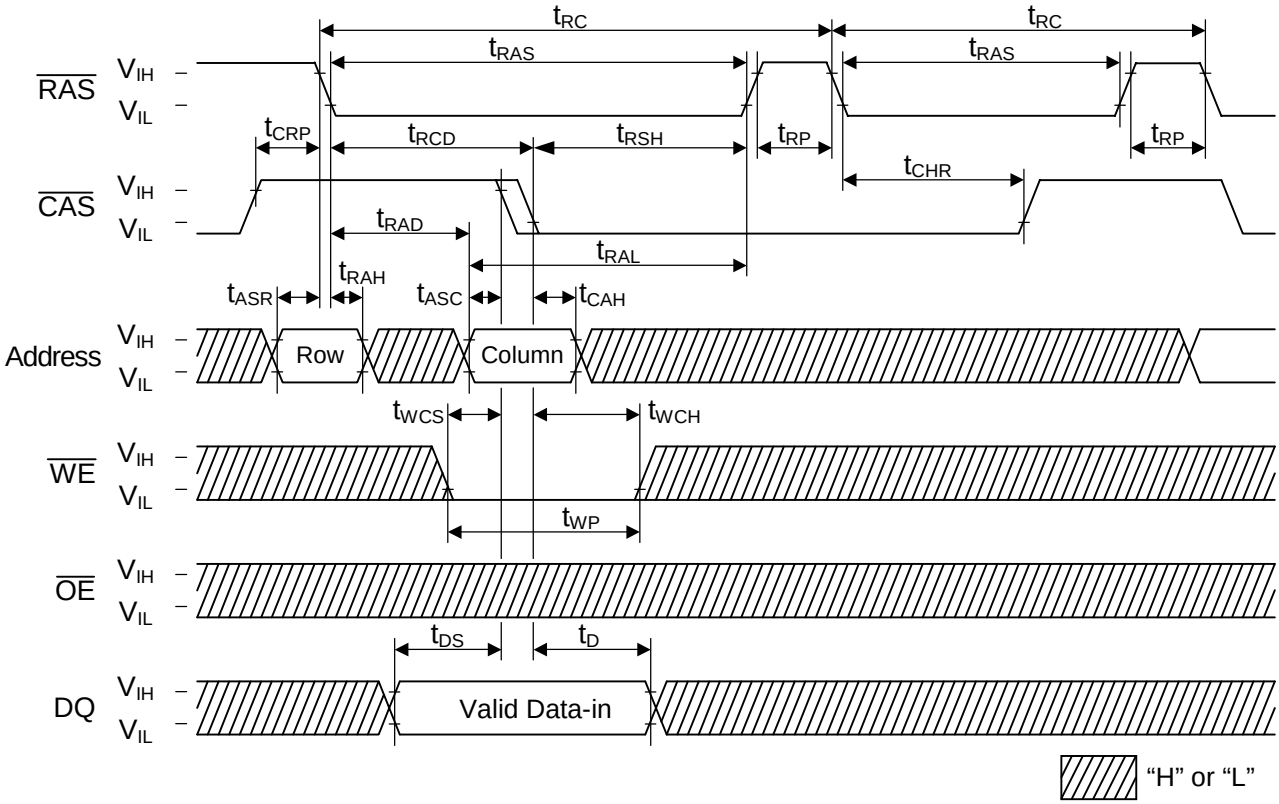
- $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle




- Hidden Refresh Read Cycle



Hidden Refresh Write Cycle




$\overline{CAS}$ before $\overline{RAS}$ Self-Refresh Cycle