Preliminary

OKI Semiconductor

This version: Jan. 2000
Previous version: Nov. 1998

ML9090-01,-02

LCD Driver with Key Scanner and RAM

GENERAL DESCRIPTION

The ML9090-01 and ML9090-02 are LCD drivers that contain internal RAM and a key scan function. They are best suited for car audio displays.
Since 1-bit data of the display RAM corresponds to the light-on or light-off of 1-dot of the LCD panel (a bit map system), a flexible display is possible.
A single chip can implement a graphic display system of a maximum of 80 × 16 dots (80 × 8 dots for the ML9090-01, 80 × 16 dots for the ML9090-02) and an arbitrator display system of 80 × 2 dots.
Since containing voltage multipliers, the ML9090-01 and ML9090-02 require no power supply circuit to drive the LCD.
Since the internal 5 × 5 scan circuit has eliminated the needs of key scanning by the CPU, the ports of the CPU can be efficiently used.

FEATURES

- Logic voltage: V_{DD} 2.7 to 5.5 V
- LCD drive voltage: V_{BI} 6 to 16 V (positive voltage)
- 80 segment outputs,10 common outputs for ML9090-01 and 18 common outputs for ML9090-02
- Built-in bit-mapped RAM (ML9090-01: 80 × 10 = 800 bits, ML9090-02: 80 × 18 = 1440 bits)
- 4-pin serial interface with CPU: $\overline{CS}$, $\overline{CP}$, DI/O, KREQ
- Built-in LCD drive bias resistors
- Built-in voltage doubler and tripler circuits
- Built-in 5 × 5 key scanner
- Port A output : 1 pin, output current: -15mA: (may be used for LED driving)
- Port B output : 8 pins
  Output current (available for the ML9090-01 only)
  –2mA : 5 pins
  –15mA : 3 pins
- Temperature range: –40 to +85°C
- Package: 128-pin plastic QFP (QFP128-P-1420-0.50-K) (Product name: ML9090-01GA)
  (Product name: ML9090-02GA)

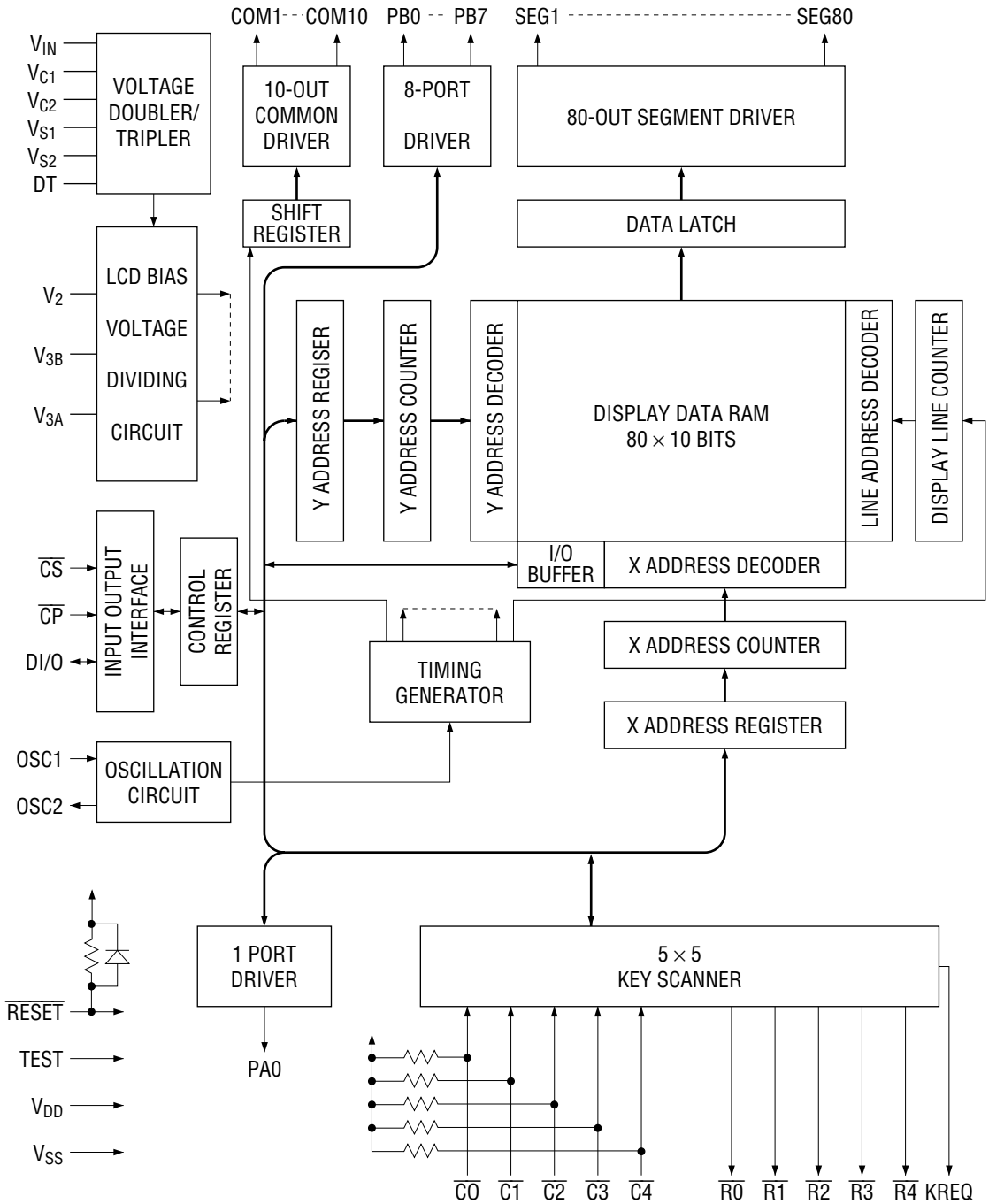
Model	ML9090-01			ML9090-02		
Display duty	1/8	1/9	1/10	1/16	1/17	1/18
No. of display lines	8	9	10	16	17	18
No. of port B outputs	8	8	8	—	—	—

APPLICATION

- Car audio

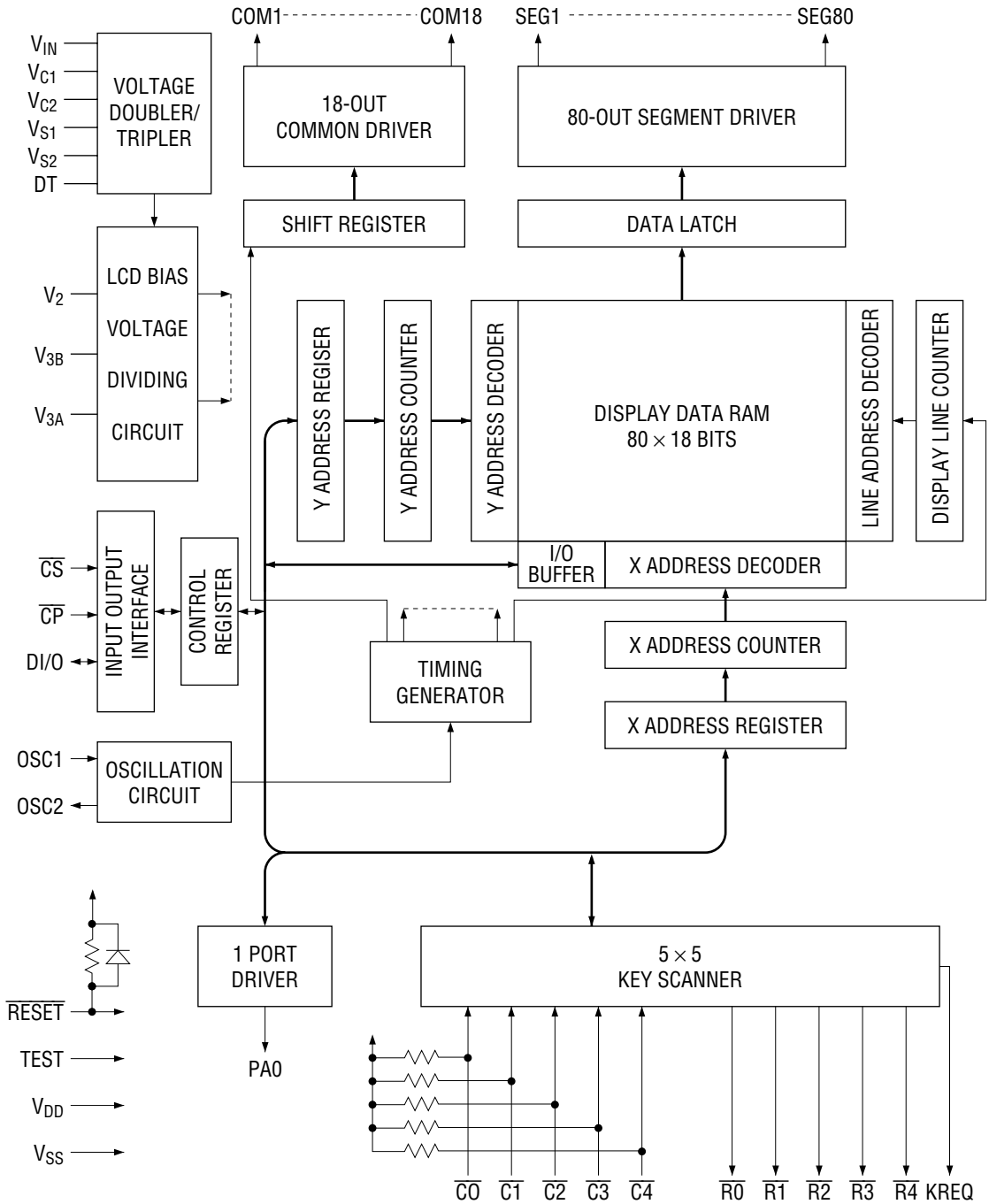
BLOCK DIAGRAM

ML9090-01



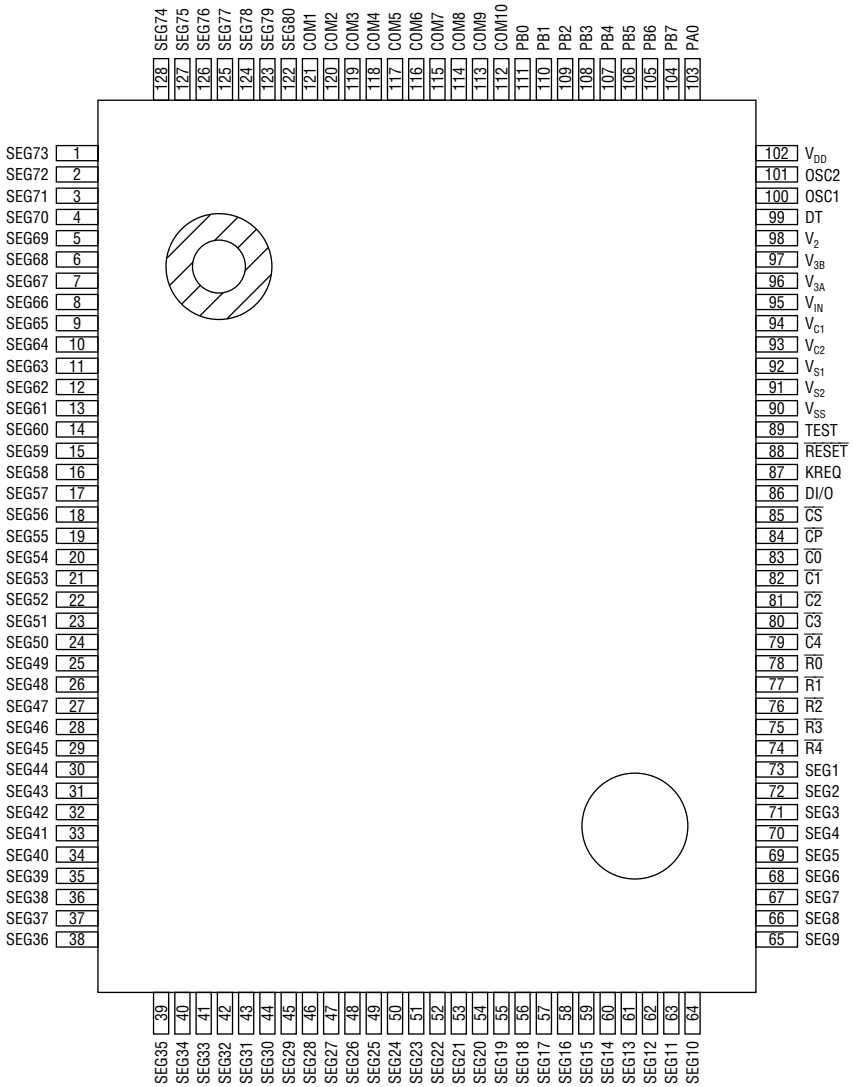
BLOCK DIAGRAM

ML9090-02



PIN CONFIGURATION (TOP VIEW)

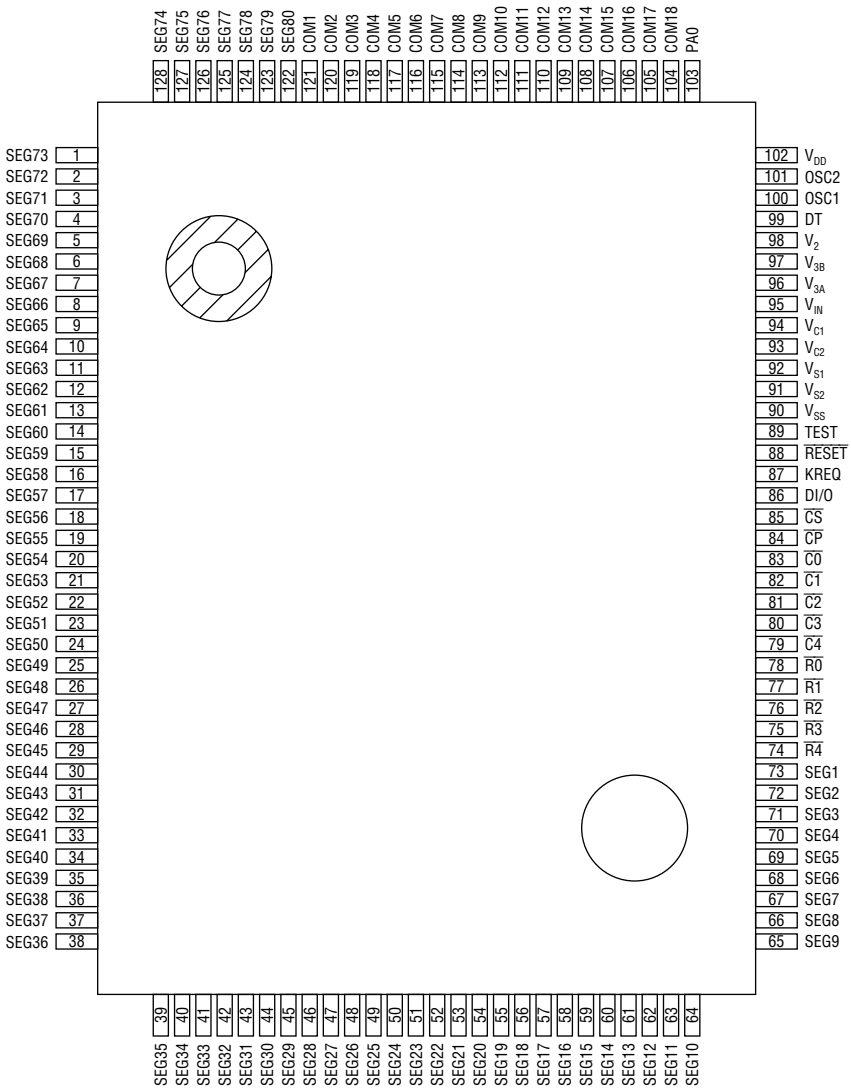
ML9090-01



128-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW)

ML9090-02



128-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V	V_{DD}
Bias Voltage	V_{BI}	Ta = 25°C	–0.3 to +18.0	V	V_{C1}, V_{C2}, V_{S1}, V_{S2}, V_2, V_{3A}, V_{3B}
Voltage Multiplier Reference Voltage	V_{IN}	Ta = 25°C *1	–0.3 to +9.84	V	V_{IN}
		Ta = 25°C *2	–0.3 to +7.36		
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V	$\overline{CS}$, $\overline{CP}$, DI/O, OSC1, $\overline{RESET}$, DT, TEST, $\overline{C0}$ to $\overline{C4}$
Output Current	I_O	Ta = 25°C	–20	mA	PA0, PB5 to PB7
		Ta = 25°C	–3	mA	PB0 to PB4
Power Dissipation	P_D	Ta = 85°C	190	mW	—
Storage Temperature	T_{stg}	—	–55 to +150	°C	—

*1: When Ta = 25°C and the voltage doubler is used, use voltage multiplier reference voltage V_{IN} values within a range that does not exceed the maximum bias voltage.

*2: When Ta = 25°C and the voltage tripler is used, use voltage multiplier reference voltage V_{IN} values within a range that does not exceed the maximum bias voltage.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable Pins
Power Supply Voltage	V_{DD}	—	2.7 to 5.5	V	V_{DD}
Bias Voltage	V_{BI}	*1	6.0 to 16.0	V	V_{S2}
Voltage Multiplier Reference Voltage	V_{IN}	*2	3.0 to 8.8	V	V_{IN}
		*3	2.0 to 6.6		
Operating Frequency	F_{op}	R = 56kΩ ±2%	480 to 1200	kHz	OSC1
Operating Temperature	T_{op}	—	–40 to +85	°C	—

*1: For the bias voltage, V_{S2} is the maximum voltage potential and V_{SS} is the minimum voltage potential. $V_{S2} > V_2 \geq V_{3A}$, $V_{3B} > V_{SS}$.

*2: When the voltage doubler is used, use voltage multiplier reference voltage V_{IN} values within a range that does not exceed the maximum bias voltage.

*3: When the voltage tripler is used, use voltage multiplier reference voltage V_{IN} values within a range that does not exceed the maximum bias voltage.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{BI} = 6 to 16 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
"H" Input Voltage 1	V_{IH1}	—	$0.85V_{DD}$	—	V_{DD}	V	OSC1
"H" Input Voltage 2	V_{IH2}	—	$0.85V_{DD}$	—	V_{DD}	V	$\overline{RESET}$
"H" Input Voltage 3	V_{IH3}	—	$0.85V_{DD}$	—	V_{DD}	V	$\overline{CP}$
"H" Input Voltage 4	V_{IH4}	—	$0.8V_{DD}$	—	V_{DD}	V	$\overline{CS}$, DI/O, $\overline{C0}$ to $\overline{C4}$
"L" Input Voltage 1	V_{IL1}	—	0	—	$0.15V_{DD}$	V	OSC1
"L" Input Voltage 2	V_{IL2}	—	0	—	$0.15V_{DD}$	V	$\overline{RESET}$
"L" Input Voltage 3	V_{IL3}	—	0	—	$0.15V_{DD}$	V	$\overline{CP}$
"L" Input Voltage 4	V_{IL4}	—	0	—	$0.2V_{DD}$	V	$\overline{CS}$, DI/O, $\overline{C0}$ to $\overline{C4}$
Hysteresis Voltage 1	V_{HIS1}	V_{DD} = 5 V	—	0.3	—	V	OSC1
Hysteresis Voltage 2	V_{HIS2}	V_{DD} = 5 V	—	0.4	—	V	$\overline{CP}$
Hysteresis Voltage 3	V_{HIS3}	V_{DD} = 5 V	—	0.4	—	V	$\overline{RESET}$
"H" Input Current 1	I_{IH1}	$V_I = V_{DD}$	—	—	10	µA	$\overline{RESET}$
"H" Input Current 2	I_{IH2}	$V_I = V_{DD}$	—	—	10	µA	$\overline{C0}$ to $\overline{C4}$
"H" Input Current 3	I_{IH3}	$V_I = V_{DD}$	—	—	10	µA	DI/O
"H" Input Current 4	I_{IH4}	$V_I = V_{DD}$	—	—	1	µA	OSC1, $\overline{CS}$, $\overline{CP}$, DT, TEST
"L" Input Current 1	I_{IL1}	V_{DD} = 5 V, V_I = 0 V	–0.02	–0.05	–0.1	mA	$\overline{RESET}$
"L" Input Current 2	I_{IL2}	V_{DD} = 5 V, V_I = 0 V	–0.18	–0.45	–0.9	mA	$\overline{C0}$ to $\overline{C4}$
"L" Input Current 3	I_{IL3}	V_I = 0 V	—	—	–10	µA	DI/O
"L" Input Current 4	I_{IL4}	V_I = 0 V	—	—	–1	µA	OSC1, $\overline{CS}$, $\overline{CP}$, DT, TEST
"H" Output Voltage 1	V_{OH1}	I_O = –0.4mA	V_{DD}–0.4	—	—	V	DI/O, KREQ
"H" Output Voltage 2	V_{OH2}	I_O = –40µA	$0.9V_{DD}$	—	—	V	OSC2
"H" Output Voltage 3	V_{OH3}	I_O = –15mA	V_{DD}–1.7	—	—	V	PA0, PB5 to PB7
"H" Output Voltage 4	V_{OH4}	I_O = –2mA	V_{DD}–1.2	—	—	V	PB0 to PB4
"H" Output Voltage 5	V_{OH5}	I_O = –50µA	V_{DD}–2.0	—	—	V	$\overline{R0}$ to $\overline{R4}$
"L" Output Voltage 1	V_{OL1}	I_O = 0.4mA	—	—	0.4	V	DI/O, KREQ
"L" Output Voltage 2	V_{OL2}	I_O = 40µA	—	—	$0.1V_{DD}$	V	OSC2
"L" Output Voltage 3	V_{OL3}	I_O = 1mA	—	—	0.4	V	PA0, PB0 to PB7
"L" Output Voltage 4	V_{OL4}	I_O = 1.8mA	—	—	0.7	V	$\overline{R0}$ to $\overline{R4}$
LCD Driving Bias Resistance	L_{BR}	—	6.3	9	13	kΩ	V_2 to V_{3A}
Segment Output Voltage 1 (1/4 bias)	V_{OS0}	I_O = –10µA	V_{S2}–0.6	—	—	V	SEG1 to SEG80
	V_{OS1}	I_O = ±10µA	$2/4V_{S2}$–0.6	—	$2/4V_{S2}$+0.6	V	
	V_{OS2}	I_O = ±10µA	$2/4V_{S2}$–0.6	—	$2/4V_{S2}$+0.6	V	
	V_{OS3}	I_O = +10µA	—	—	V_{SS}+0.6	V	

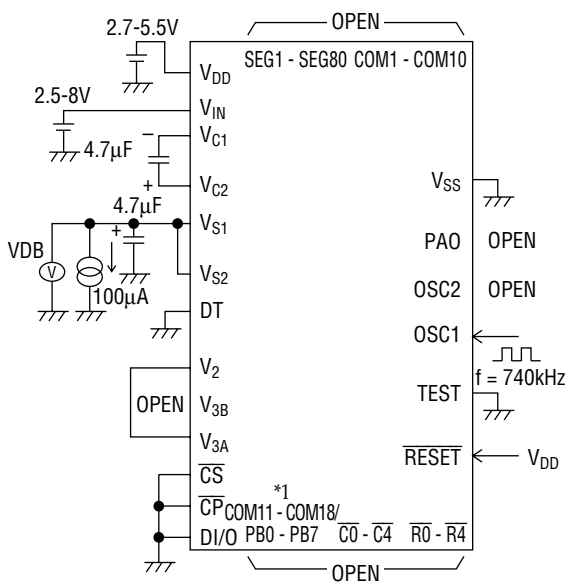
(V_{DD} = 2.7 to 5.5 V, V_{BI} = 6 to 16 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
Common Output Voltage 1 (1/4 bias)	V_{OC0}	I_O = –10µA	V_{S2}–0.3	—	—	V	COM1 to COM18
	V_{OC1}	I_O = ±10µA	3/4V_{S2}–0.3	—	3/4V_{S2}+0.3	V	
	V_{OC2}	I_O = ±10µA	1/4V_{S2}–0.3	—	1/4V_{S2}+0.3	V	
	V_{OC3}	I_O = +10µA	—	—	V_{SS}+0.3	V	
Segment Output Voltage 2 (1/5 bias)	V_{OS0}	I_O = –10µA	V_{S2}–0.6	—	—	V	SEG1 to SEG80
	V_{OS1}	I_O = ±10µA	3/5V_{S2}–0.6	—	3/5V_{S2}+0.6	V	
	V_{OS2}	I_O = ±10µA	2/5V_{S2}–0.6	—	2/5V_{S2}+0.6	V	
	V_{OS3}	I_O = +10µA	—	—	V_{SS}+0.6	V	
Common Output Voltage 2 (1/5 bias)	V_{OC0}	I_O = –10µA	V_{S2}–0.3	—	—	V	COM1 to COM18
	V_{OC1}	I_O = ±10µA	4/5V_{S2}–0.3	—	4/5V_{S2}+0.3	V	
	V_{OC2}	I_O = ±10µA	1/5V_{S2}–0.3	—	1/5V_{S2}+0.3	V	
	V_{OC3}	I_O = +10µA	—	—	V_{SS}+0.3	V	
Voltage Multiplier Voltage 1	V_{DB}	External clock = 740KHz *1	V_{IN}×1.83 –0.5	—	—	V	V_{S1}
Voltage Multiplier Voltage 2	V_{TR}	External clock = 740KHz *1	V_{IN}×2.46 –1.0	—	—	V	V_{S2}
Supply Current 1	I_{DD1}	R = 56KΩ±2% *1	—	—	0.95	mA	V_{DD}
Supply Current 2	I_{DD2}	External clock = 740KHz *1	—	—	0.7	mA	V_{DD}

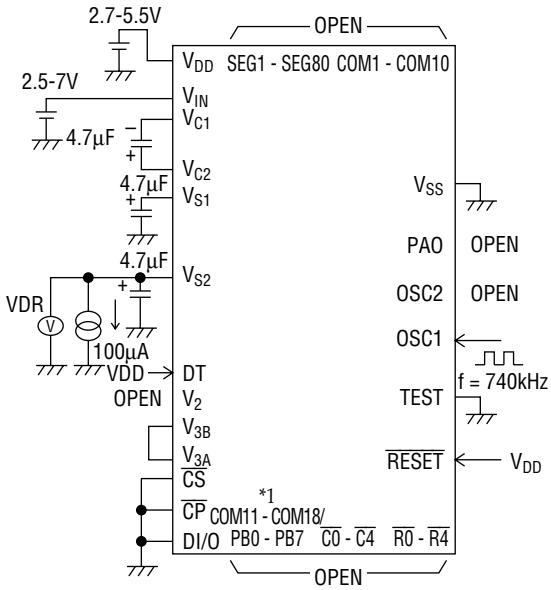
*1: Refer to Measuring Circuits

Measuring Circuits

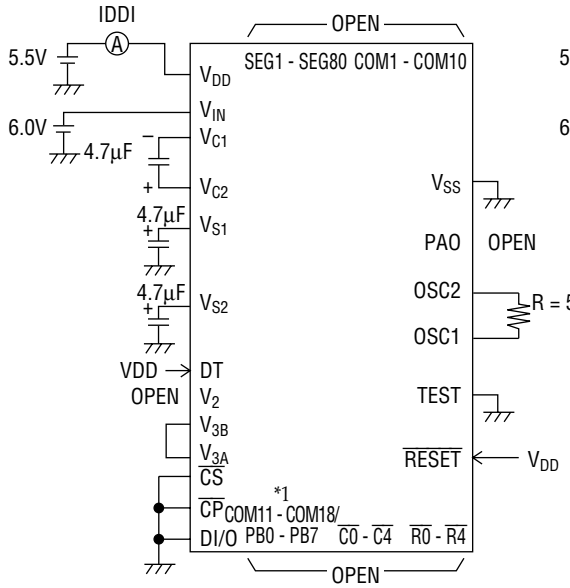
Voltage multiplier voltage 1
When voltage doubler is used.



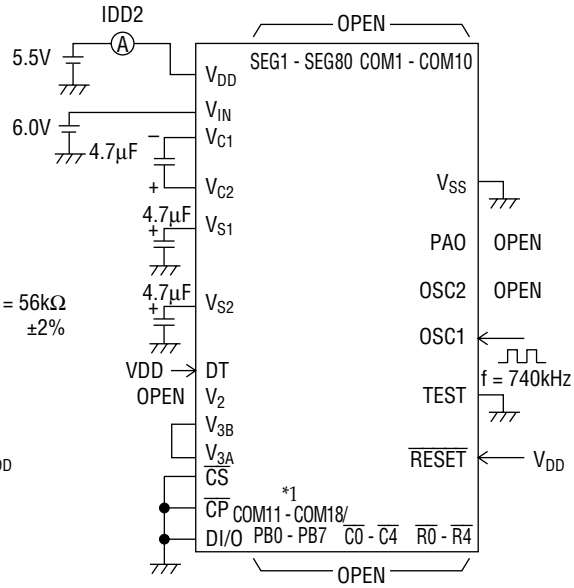
Voltage multiplier voltage 2
When voltage tripler is used.



Supply current 1



Supply current 2



*1: PB0 - PB7 for ML9090-01, and COM11 - COM18 for ML9090-02

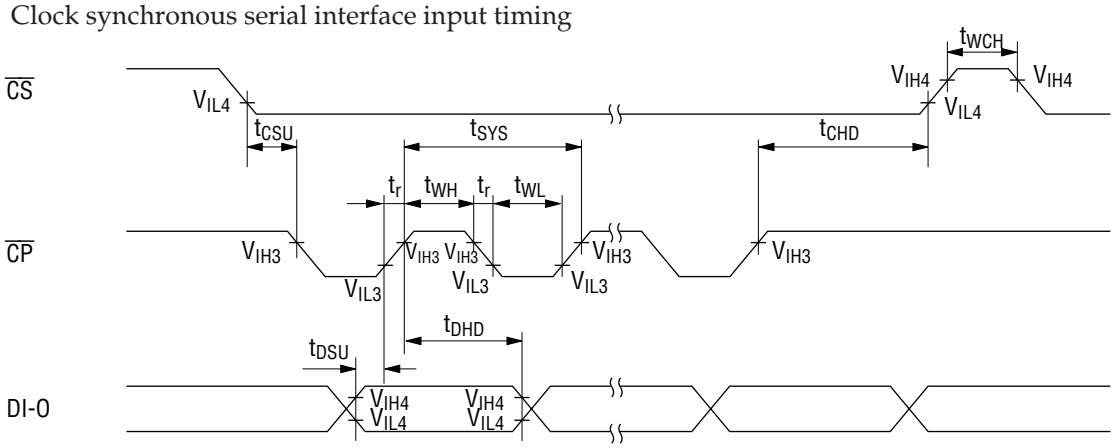
Switching Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{BI} = 6 to 16 V, Ta = –40 to +85°C)

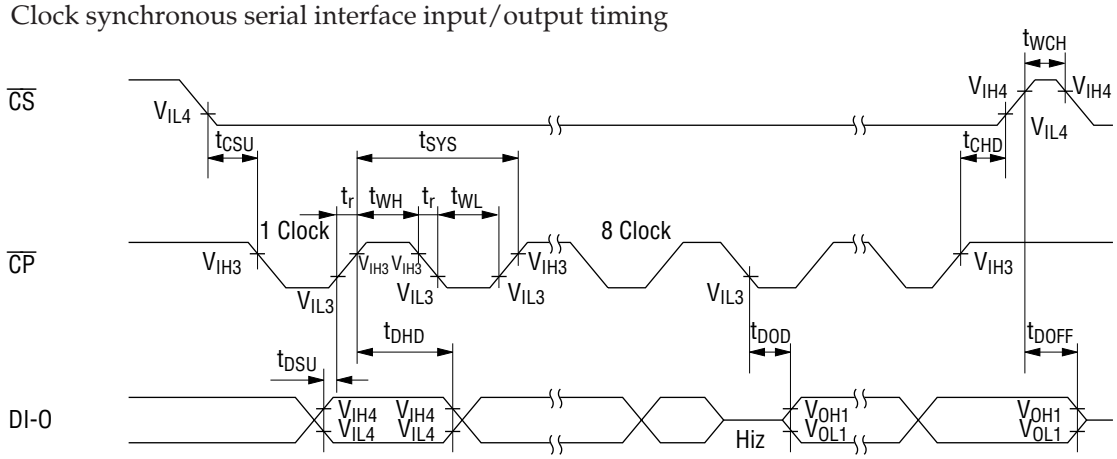
Parameter	Symbol	Condition	Min	Max	Unit
$\overline{CP}$ Clock Cycle Time	t_{SYS}	—	1000	—	ns
$\overline{CP}$ "H" Pulse Width	t_{WH}	—	400	—	ns
$\overline{CP}$ "L" Pulse Width	t_{WL}	—	400	—	ns
$\overline{CS}$ "H" Pulse Width	t_{WCH}	—	200	—	ns
$\overline{CP}$ Clock Rise/fall Time	t_r, t_f	—	—	100	ns
$\overline{CS}$ Setup Time	t_{CSU}	—	60	—	ns
$\overline{CS}$ Hold Time	t_{CHD}	—	290	—	ns
DI/O Setup Time	t_{DSU}	—	100	—	ns
DI/O Hold Time	t_{DHD}	—	15	—	ns
DI/O Output Delay Time	t_{DOD}	CL = 50pF	—	200	ns
DI/O Output OFF Delay Time	t_{DOFF}	CL = 50pF	—	200	ns
$\overline{RESET}$ Pulse Width	t_{WRE}	—	2		µs
External Clock Cycle Time	t_{SES}	—	833	—	ns
External Clock "H" Pulse Width	t_{WEH}	—	316	—	ns
External Clock "L" Pulse Width	t_{WEL}	—	316	—	ns
External Clock Rise/fall Time	t_{rE}, t_{fE}	—	—	100	ns

Clock synchronous serial interface timing diagrams

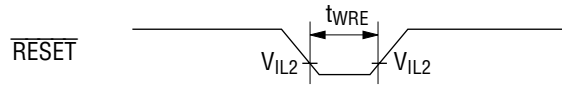
Clock synchronous serial interface input timing



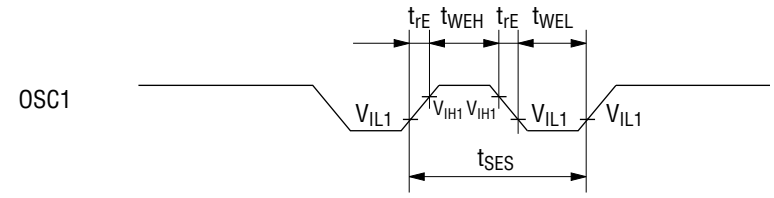
Clock synchronous serial interface input/output timing



Reset timing



External clock



FUNCTIONAL DESCRIPTIONS

Pin Functional Descriptions

Function	Symbol	Pin name	Type	No.of pins	Description
CPU interface	$\overline{CS}$	Chip Select	I	1	Chip select signal input pin
	$\overline{CP}$	Clock Pulse	I	1	Shift clock signal input pin. This pin is connected to an internal Schmitt circuit
	DI/O	Data I/O	I/O	1	Serial data signal I/O pin
	KREQ	Key Request	O	1	Key request signal output pin
Oscillation	OSC1	OSC1	I	1	Connect external resistors.
	OSC2	OSC2	O	1	
Control signals	$\overline{RESET}$	RESET	I	1	Initial settings can be established by pulling the reset input to a "L" level. This pin is connected to an internal Schmitt circuit.
	DT	Doubler Tripler Select	I	1	Input pin for selecting the voltage doubler or voltage tripler.
	TEST	TEST	I	1	Test input pin. This pin is connected to the V_{SS} pin.
Key scan signals	$\overline{C0}$ to $\overline{C4}$	Column Input	I	5	Input pins that detect status of key switches
	$\overline{R0}$ to $\overline{R4}$	Row Output	O	5	Key switch scan signal pins
Port outputs	PA0	Port Output	O	1	Port A output
	PB0 to PB7	Port Output	O	8	Port B outputs (for ML9090-01)
LCD driver outputs	SEG1 to SEG80	Seg Output	O	80	Outputs for LCD segment drivers
	COM1 to COM10	Com Output	O	10	Outputs for LCD common drivers (for ML9090-01)
	COM1 to COM18	Com Output	O	18	Outputs for LCD common drivers (for ML9090-02)
Power supply	V_{DD}	V_{DD}	—	1	Logic power supply pin
	V_{SS}	V_{SS}	—	1	GND pin
	V_{IN}	V_{IN}	—	1	Voltage multiplier reference voltage power supply pin
	V_{C1}, V_{C2}	V_{C1}, V_{C2}	—	2	Capacitor connection pins for voltage multiplier
	V_{S1}	V_{S1}	—	1	Voltage doubler output pin
	V_{S2}	V_{S2}	—	1	Voltage tripler output pin
	V_2, V_{3A}, V_{3B}	V_2, V_{3A}, V_{3B}	—	3	LCD bias pins

Register List

RS	R/W	Register number				Register symbol	Register name	Data bits							
		3	2	1	0			7	6	5	4	3	2	1	0
0	1	0	0	0	0	KR	Key scan register	ST2	ST1	ST0	S4	S3	S2	S1	S0
1	1/0	0	0	0	1	DRAM	Display data register	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	XAD	X address register	—	—	—	—	X3	X2	X1	X0
0	0	0	0	1	1	YAD	Y address register	—	—	—	Y4	Y3	Y2	Y1	Y0
0	0	0	1	0	0	PTA	Port register A	—	—	—	—	—	—	—	PA0
0	0	0	1	0	1	PTB	Port register B	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	1	0	0	0	FCR1	Control register 1	INC	WLS	KT	SHL	—	—	DTY1	DTY0
0	0	1	0	0	1	FCR2	Control register 2	—	—	T4	T3	T2	T1	—	DISP

RS Register select bit 1: RAM 0: Register
R/W Read/write select bit 1: Read 0: Write

ST0 to ST2 : Scan status
S0 to S4 : Key scan data
D0 to D7 : Display data and RAM read data
X0 to X3 : X address
Y0 to Y4 : Y address
PA0 : Port A data
PB0 to PB7 : Port B data (ML9090-01 only)
INC : Address increment 1: X direction, 0: Y direction
WLS : Word length select 1: 6 bits, 0: 8 bits
KT : Key scan cycle select 1: 10 ms, 0: 5 ms
DTY0, DTY1: Display duty select (1/8, 1/9, 1/10) (ML9090-01)
(1/16, 1/17, 1/18) (ML9090-02)
SHL : Common driver shift direction select bit
1: COM10→COM1, 0 : COM1→COM10 (ML9090-01)
1: COM18→COM1, 0 : COM1→COM18 (ML9090-02)
DISP : Display ON/OFF select 1: Display ON, 0: Display OFF
T1 to T4 : Write "0"
— : Don't care

Pin Functional Descriptions

• $\overline{CS}$

Chip select input pin. An "L" level selects the chip, and an "H" level does not select the chip. During the "L" level, internal registers can be accessed.

• $\overline{CP}$

Clock input pin for serial interface data I/O. An internal Schmitt circuit is connected to this pin. Data input to the DI/O pin is synchronized to the rising edge of the clock. Output from the DI/O pin is synchronized to the falling edge of the clock.

• DI/O

Serial interface data I/O pin. This pin is in the output state only during the interval beginning when key scan data read or RAM read commands (to be described later) are written (after the rising edge of the 8th $\overline{CP}$ clock during start byte setup, the CPU changes from output to input and the DI/O output interval begins at the $\overline{CP}$ falling edge) until the $\overline{CS}$ signal rises. At all other times this pin is in the input state. (When reset, the input state is set.) The relation between data level of this pin and operation is listed below.

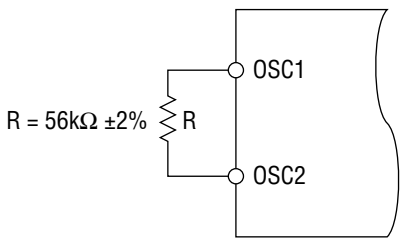
Data level	LCD display	Port	Key status
"H"	Light ON	"H"	ON
"L"	Light OFF	"L"	OFF

• KREQ

Key scan read READY signal output pin. Two scan cycles after a key switch is switched ON, this pin goes to an "H" level. When all key switches are OFF, this pin returns to an "L" level. Begin the key scan read operation after this pin goes to an "H" level.

• OSC1

Input pin for RC oscillation. An oscillation circuit is formed by connecting a resistor (R) of 56kΩ ±2% to this pin and the OSC2 pin. If an external master oscillation clock is to be input, input the master oscillation clock to this pin.



• OSC2

Input pin for RC oscillation. An oscillation circuit is formed by connecting a resistor (R) of 56kΩ ±2% to this pin and the OSC1 pin. If an external master oscillation clock is to be input, leave this pin unconnected (open).

• **$\overline{\text{RESET}}$**
Reset signal input pin. The initial state can be set by pulling this pin to an "L" level. Refer to the "Pin and Register States in Response to Reset Input" page for the initial states of each register and display.
An internal pull-up resistor is connected to this pin. An external capacitor is connected for power-on-reset operation.

• **TEST**
Test signal input pin. This pin is used for testing by Oki. Connect this pin to V_{SS}. When a different connection is made, proper operation cannot be guaranteed.

• **$\overline{\text{R0}}$ to $\overline{\text{R4}}$**
Key switch scan signal output pins. During the scan operation, "L" level signals are output in the order of R0, R1, ...R4. (Refer to the page entitled "Key scan" for further details.)

• **$\overline{\text{C0}}$ to $\overline{\text{C4}}$**
Input pins that detect the key switch status. Internal pull-up resistors are connected to these pins. Assemble a key matrix between these pins and the $\overline{\text{R0}}$ to $\overline{\text{R4}}$ pins.

• **PA0**
General-purpose port A output pin. Because this pin can output a current of 15mA, it is best suited as an LED driver. If this pin is used as an LED driver, insert an external current limiting resistor in series with the LED.

• **PB0 to PB7**
General-purpose port B output pins. Each of the PB5 to PB7 pins has the same driving capability as the PA0 pin. These pins are only applicable to the ML9090-01.

• **SEG1 to SEG80**
Segment signal output pins for LCD driving. Leave unused pins unconnected (open).

• **COM1 to COM10**
Common signal output pins for LCD driving. Leave unused pins unconnected (open).

• **COM1 to COM18**
Common signal output pins for LCD driving. Leave unused pins unconnected (open). These pins are applicable to the ML9090-02.

• **V_{DD}**
Logic power supply connection pin.

• **V_{SS}**
Power supply GND connection pin.

• DT

This pin selects the voltage multiplier circuit. If this pin is connected to the V_{SS} pin, the voltage doubler circuit is selected. If this pin is connected to the V_{DD} pin, the voltage tripler circuit is selected. Do not change the value of the setting after power is turned on.

• V_{C1}, V_{C2}

Capacitor connection pins for the voltage multiplier. Connect a 4.7µF capacitor between the V_{C1} and V_{C2} pins. If an electrolytic capacitor is used, connect the (+) side to pin V_{C2}.

• V_{S1}

Voltage doubler voltage output pin. This pin outputs the doubled voltage that has been input to V_{IN}. To increase stability of the power supply, connect a 4.7µF capacitor between this pin and V_{SS}. When using the doubled voltage, connect this pin and V_{S2}.

• V_{S2}

Voltage multiplier voltage output pin. Voltage multiplied by the factor specified by the DT pin setting is output from this pin. When the voltage tripler is used, to increase stability of the power supply, connect a 4.7µF capacitor between this pin and V_{SS}. When using the voltage doubler, connect this pin and V_{S1}.

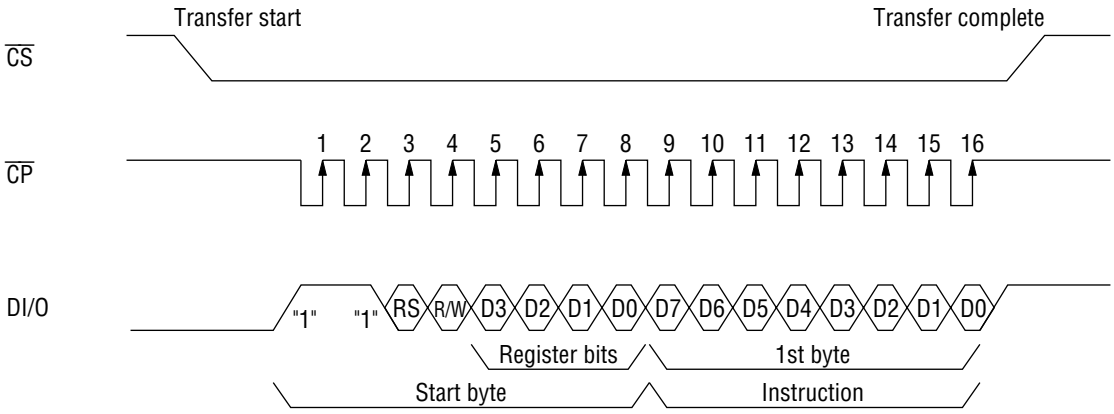
• V_{IN}

Voltage multiplier voltage input pin. The doubled or tripled voltage input to this pin is output from V_{S2}.

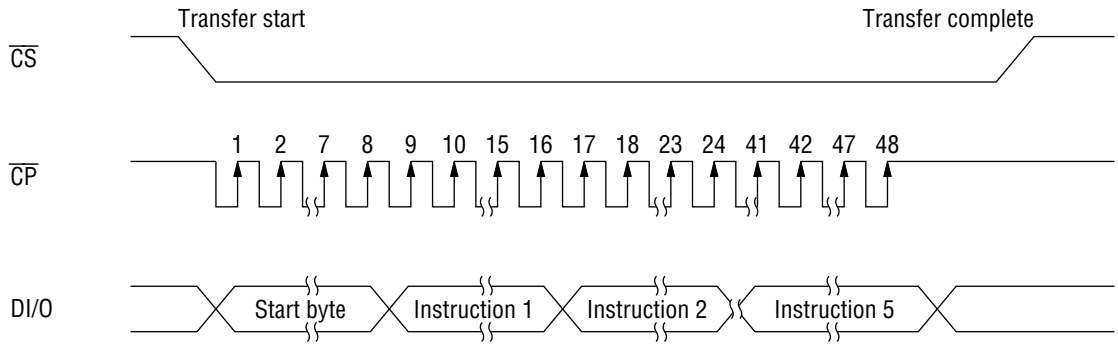
• V_2, V_{3A}, V_{3B}

LCD bias pins for segment drivers. These pins are connected to internal bias dividing resistors. When using the ML9090-01 (at 1/4 bias), connect V_2 and V_{3A} pins, and leave V_{3B} unconnected (open). When using the ML9090-02 (at 1/5 bias), connect V_{3A} and V_{3B} pins, and leave V_2 unconnected (open).

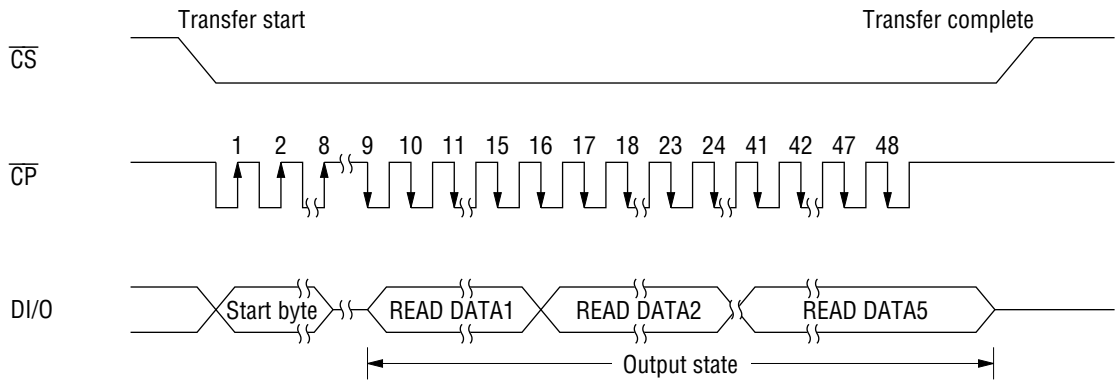
Clock Synchronous Serial Transfer Example (WRITE)



Clock Synchronous Serial Continuous Data Transfer Example (WRITE)



Clock Synchronous Serial Continuous Data Transfer Example (READ)



Register Descriptions

This IC is constructed from a start byte register and data registers.

1. Start byte register

D7	D6	D5	D4	D3	D2	D1	D0
"1"	"1"	RS	R/W	Register number			

The start byte register selects 8 types of data registers.
(1) D7, D6 (fixed at "1")
When selecting the start byte register, always write a "1" to bits D7 and D6.
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

(2) D5 RS (Register Select bit)
1: RAM is selected
0: Register is selected
This bit specifies whether the selected data register is DRAM (display data register) or registers different from the display data register. To select DRAM, write a "1" to this bit. To select registers other than DRAM, write a "0" to this bit. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this bit is reset to "0".

(3) D4 R/W (Read mode, Write mode select bit)
1: Read mode is selected
0: Write mode is selected
This bit specifies either read mode or write mode for the selected data register. To select read mode, write a "1" to this bit. To select write mode, write a "0" to this bit. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this bit is reset to "0".

(4) D3 to D0 (Register number)
These bits select the data register. The correspondence between each bit and each register is listed in the table below. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

Code	D3	D2	D1	D0	Register name
0	0	0	0	0	Key scan register
1	0	0	0	1	Display data register
2	0	0	1	0	X address register
3	0	0	1	1	Y address register
4	0	1	0	0	Port A register
5	0	1	0	1	Port B register
8	1	0	0	0	Control register 1
9	1	0	0	1	Control register 2

2. Instructions (Data Registers)

• Key scan register (KR)

D7	D6	D5	D4	D3	D2	D1	D0
ST2	ST1	ST0	S4	S3	S2	S1	S0

(1) D7 to D5 ST2 to ST0 (Scan read counter)
When reading 25-bit key scan data, these bits indicate the number of times scan data has been read. Every time key scan data is read, these bits (ST2 to ST0) are automatically incremented over the range of "000" to "100". After counting to "100", this key scan data read counter is reset to "000".
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

(2) D4 to D0 S4 to S0 (Key scan read data bits)
These bits are read as 25-bit serial data that expresses the key switch status (1 = ON, 0 = OFF). Data is divided into 5 groups and read. (For the read order, refer to the description below.) The read count is indicated by bits ST2 to ST0. S4 to S0 key scan data corresponds to each SWN0 of the key matrix shown in figure 1. The relation between the key scan data, key matrix signal and each SWN0 of the key matrix is shown below.
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

ST2	**ST1**	**ST0**	**S4**	**S3**	**S2**	**S1**	**S0**	
0	0	0	SW04	SW03	SW02	SW01	SW00	$\overline{\text{R0}}$
0	0	1	SW14	SW13	SW12	SW11	SW10	$\overline{\text{R1}}$
0	1	0	SW24	SW23	SW22	SW21	SW20	$\overline{\text{R2}}$
0	1	1	SW34	SW33	SW32	SW31	SW30	$\overline{\text{R3}}$
1	0	0	SW44	SW43	SW42	SW41	SW40	$\overline{\text{R4}}$

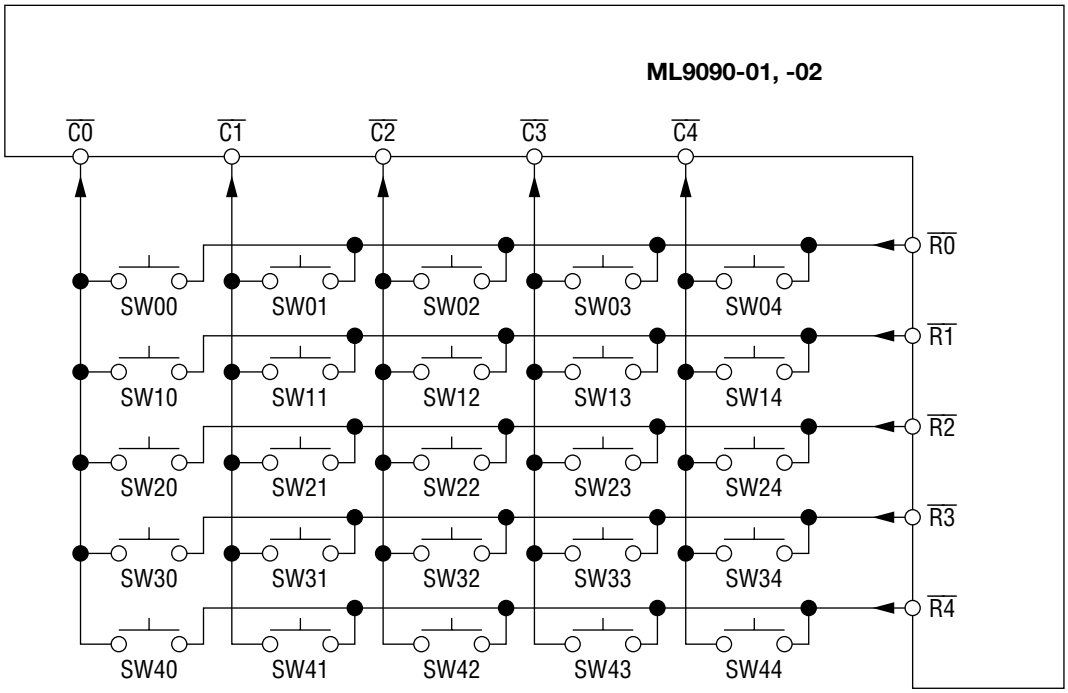

ML9090-01, -02
C0
C1
C2
C3
C4
R0
R1
R2
R3
R4
SW00
SW01
SW02
SW03
SW04
SW10
SW11
SW12
SW13
SW14
SW20
SW21
SW22
SW23
SW24
SW30
SW31
SW32
SW33
SW34
SW40
SW41
SW42
SW43
SW44

Figure 1

• Display data register (DRAM)

D7	D6	D5	D4	D3	D2	D1	D0
8-bit DATA							
—		6-bit DATA					

The display data register writes and reads display data to and from the liquid crystal display RAM. The contents of this register are written to or read from the address set by the X address register and Y address register. The bit length of display data can be selected by the WLS bit of control register 1. If 6-bit data has been selected, writing to D7 and D6 is invalid, and if read, their values will always be "0". D7 is the MSB (D5 in the case of 6-bit data) and D0 is the LSB.
The X address and Y address should be set immediately before writing or reading display data. However, only one-time settings of X address and Y address are required immediately before successive writings or readings. Either X address or Y address may be set first.
Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the contents of this register will not change.

• X address register (XAD)

D7	D6	D5	D4	D3	D2	D1	D0
—				XAD			

The X address register sets the X address for the display RAM. The address setting range is 0 to 9 (00H to 09H) when 8-bit data has been selected by the WLS bit (D6 bit) of control register 1, and 0 to 13 (00H to 0DH) when 6-bit data has been selected. Proper operation is not guaranteed if values outside this range are set. Writing to bits D7 through D4 is invalid, and if read, their values will always be "0".
If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

• Y address register (YAD)

D7	D6	D5	D4	D3	D2	D1	D0
—				YAD (ML9090-01)			
—			YAD (ML9090-02)				

The Y address register sets the Y address for the display RAM. The address setting range for the ML9090-01 is 0 to 7 (00H to 07H) when 1/8 duty has been selected by the DTY0 and DTY1 bits of control register 1, 0 to 8 (00H to 08H) when 1/9 duty has been selected, and 0 to 9 (00H to 09H) when 1/10 duty has been selected. The address setting range for the ML9090-02 is 0 to 15 (00H to 0FH) when 1/16 duty has been selected by the DTY0 and DTY1 bits of control register 1, 0 to 16 (00H to 10H) when 1/17 duty has been selected, and 0 to 17 (00H to 11H) when 1/18 duty has been selected. Proper operation is not guaranteed if values outside these ranges are set. Writing to the D4 bit of the ML9090-01 is valid. Therefore, memory (8×80 bits) corresponding to Y addresses 10 through 17 can be used as a general-purpose memory. Writing to bits D7 through D5 is invalid, and if read, their values will always be "0". When using the ML9090-02, writing to bits D7 through D5 is invalid, and if read, their values will always be "0". If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, these bits are reset to "0".

• Port register A (PTA)

D7	D6	D5	D4	D3	D2	D1	D0
			—				PTA

The port register A sets (to "1") and resets (to "0") general-purpose port A data. The setting of the PTA bit (D0 bit) corresponds to the PA0 output pin. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0" and the PA0 pin goes to high impedance. After the $\overline{\text{RESET}}$ pin is pulled to a "H" level, if port data is set in this register, the PA0 pin is released from its high impedance state and outputs the corresponding port data.

• Port register B (PTB)

D7	D6	D5	D4	D3	D2	D1	D0
PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0

The port register sets (to "1") and resets (to "0") general-purpose port B data. The settings of the PTB0 to PTB7 bits (D0 to D7 bits) correspond to the PTB0 to PTB7 output pins. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0" and pins PTB0 through PTB7 go to high impedance. After the $\overline{\text{RESET}}$ pin is pulled to a "H" level, if port data is set in this register, pins PTB0 through PTB7 are released from their high impedance states and output the corresponding port data.

• Control register 1 (FCR1)

D7	D6	D5	D4	D3	D2	D1	D0
INC	WLS	KT	SHL	—	—	DTY1	DTY0

(1) D7 INC Address increment direction

1: X direction address increment

0: Y direction address increment

This bit sets the address increment direction of the display RAM. The display RAM address is automatically incremented by 1 every time data is written to the display data register. Writing a "1" to this bit sets "X address increment", and writing a "0" sets "Y address increment". For further details regarding address incrementing, refer to the page entitled "X, Y Address Counter Auto Increment", Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(2) D6 WLS (Word Length Select)

1: 6-bit word length select

0: 8-bit word length select

This bit selects the word length of data to be written to and read from the display RAM. If "1" is written to this bit, data will be read from and written to the display RAM in 6-bit units. If "0" is written to this bit, data will be read from and written to the display RAM in 8-bit units. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(3) D5 KT (Key scan time) Key scan time select bit

1: 10ms

0: 5ms

This bit selects the key scan cycle time. In the case of a 740kHz oscillating frequency, writing a "1" to this bit sets the key scan cycle time at 10ms, writing a "0" sets the key scan cycle time at 5ms. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" level, the value of this bit will not change.

(4) D4 SHL (Common driver shift direction select bit)

This bit selects the shift direction of common drivers.

The relationship between this bit and shift directions are shown below.

Even if the $\overline{\text{RESET}}$ Pin is set to "L", this bit remains unchanged.

Model	SHL	Duty	Shift direction
ML9090-01	1	1/8	COM8 → COM1
		1/9	COM9 → COM1
		1/10	COM10 → COM1
	0	1/8	COM1 → COM8
		1/9	COM1 → COM9
		1/10	COM1 → COM10
ML9090-02	1	1/16	COM16 → COM1
		1/17	COM17 → COM1
		1/18	COM18 → COM1
	0	1/16	COM1 → COM16
		1/17	COM1 → COM17
		1/18	COM1 → COM18

(5) D1 to D0 DTY (Display duty select bit)

This bit selects the display duty. The correspondence between each bit and display duty is shown in the chart below. Even if the $\overline{\text{RESET}}$ pin is pulled to a "L" Level, the values of these bits will not change.

Model	Code	DTY1	DTY0	Display duty
ML9090-01	0	0	0	1/8
	1	0	1	1/9
	2	1	0	1/10
	3	1	1	1/10
ML9090-02	0	0	0	1/16
	1	0	1	1/17
	2	1	0	1/18
	3	1	1	1/18

• Control register 2 (FCR2)

D7	D6	D5	D4	D3	D2	D1	D0
—		T4	T3	T2	T1	—	DISP

(1) D0 DISP (Display ON/OFF mode bit)

1: Display ON mode

0: Display OFF mode

This bit selects whether the display is ON or OFF. Writing a "1" to this bit selects the display ON mode. Writing a "0" to this bit selects the display OFF mode. At this time, the COM and SEG pins will be at the VSS level. Even if this bit is set to "0", the display RAM contents will not change. If the $\overline{\text{RESET}}$ pin is pulled to a "L" level, this register is reset to "0".

(2) D2 to D5 T1 to T4 (Test mode select bit)

These bits are used to test the IC. "0" must be written to these bits.

Display screen and memory address

The ML9090 contains an internal bit-mapped display RAM (80 × 18 bits). As shown in figure 2, display data is written to display memory such that the MSB of the display data is written to the (Xn, Yn) memory address and the LSB is written to the (Xn+7, Yn) address. Writing a "1" to the display memory turns on the display of the LCD panel and writing a "0" turns off the display. As shown in figure 3, address allocation is different depending upon whether an 8-bit or 6-bit word length is selected. For an 8-bit word length, addresses are allocated from 0 to 9, and for a 6-bit word length, addresses are allocated from 0 to 13.
When 6-bits/word are selected and the X address is 13, the display memory is only 2 bits; 2 bits from the MSB of the display data (D5 and D4) are written to memory and the remaining 4 bits (D3 to D0) are invalid.

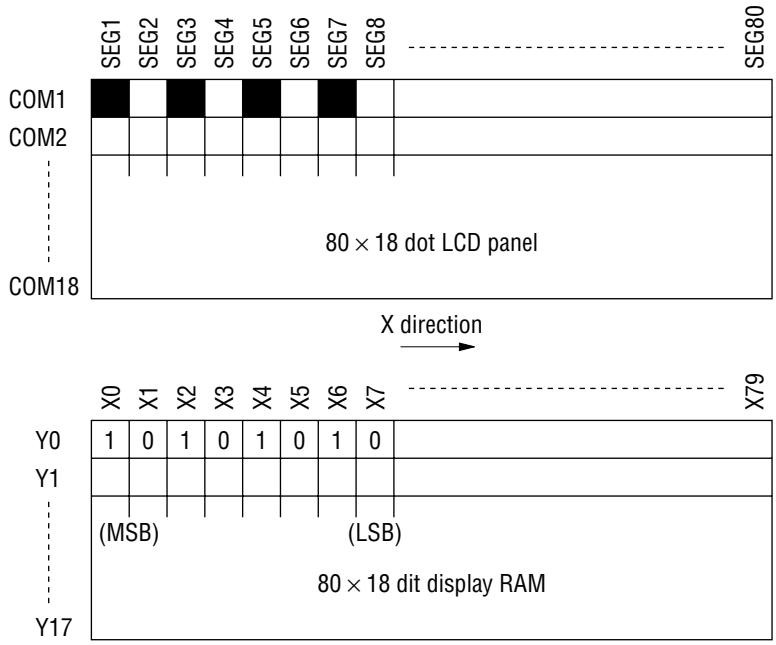


Figure 2 Correspondence Between Display Screen and Memory

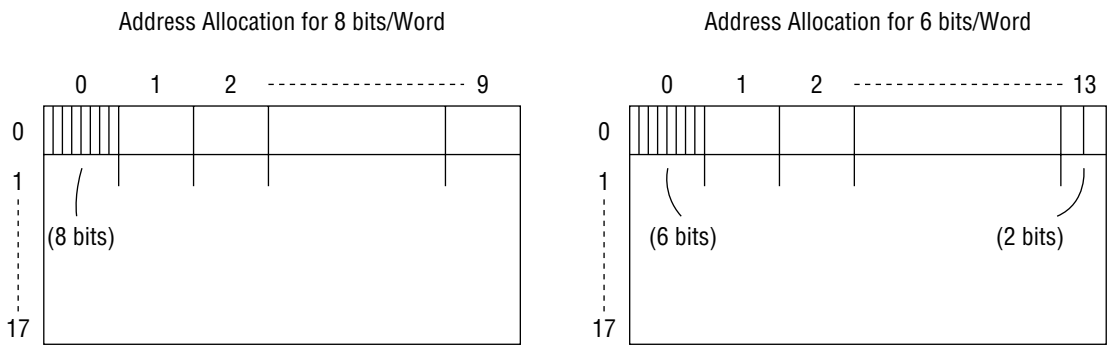


Figure 3 Display Memory Addresses

X, Y address Counter Auto Increment

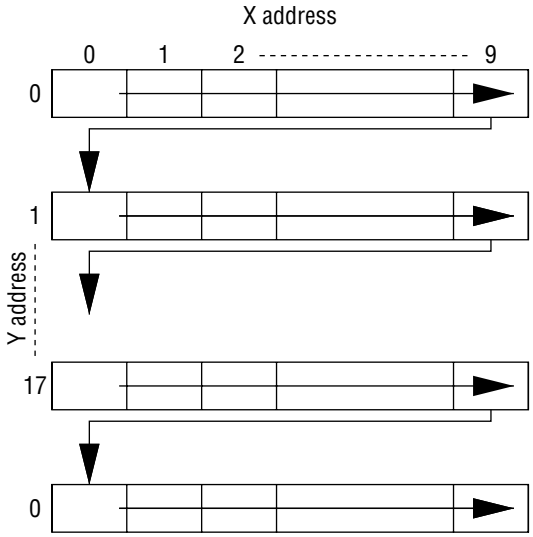
The display RAM of the ML9090-01 and ML9090-02 has an X address counter and a Y address counter. Both counters have an auto increment function. Writing or reading display data will cause either the X or Y address counter to be incremented. The INC bit (D7 bit) setting of control register 1 selects either the X address or Y address to be incremented.

(When X address is selected) (INC = "1")
The address count cycle of the X address counter differs depending upon whether the word length is 8 bits or 6 bits.
If the word length is 8 bits, X addresses in the range of 0 to 9 are counted.
If the word length is 6 bits, X addresses in the range of 0 to 13 are counted.
When the X address count value returns from its maximum value (9 in the case of 8-bit word length, 13 in the case of 6-bit word length) to 0, the Y address is also automatically incremented.

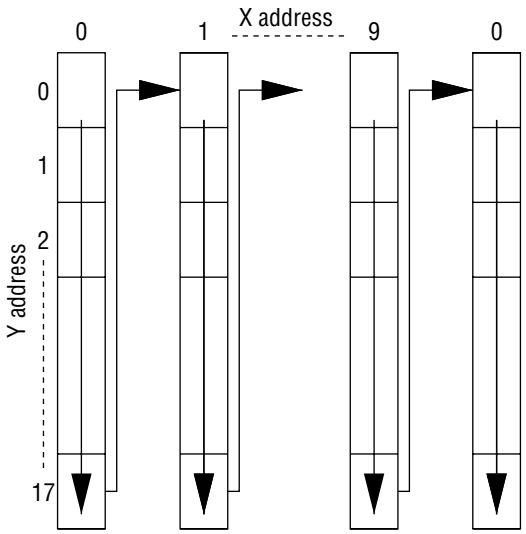
(When Y address is selected) (INC = "0")
The address count cycle of the Y address counter differs depending upon whether the display duty is 1/8, 1/9, 1/10, 1/16, 1/17, or 1/18.
If the display duty is 1/8, Y addresses in the range of 0 to 7 are counted.
If the display duty is 1/9, Y addresses in the range of 0 to 8 are counted.
If the display duty is 1/10, Y addresses in the range of 0 to 9 are counted.
If the display duty is 1/16, Y addresses in the range of 0 to 15 are counted.
If the display duty is 1/17, Y addresses in the range of 0 to 16 are counted.
If the display duty is 1/18, Y addresses in the range of 0 to 17 are counted.
When the Y address count value returns from its maximum value (7 in the case of 1/8 display duty, 8 in the case of 1/9 display duty, 9 in the case of 1/10 display duty, 15 in the case of 1/16 display duty, 16 in the case of 1/17 display duty, and 17 in the case of 1/18 display duty) to 0, the X address is also automatically incremented.

Note: If an address outside the count cycle range of the X, Y address counter is set, proper operation of the X, Y address counter is not guaranteed.

1. X address increment example
(8-bit word length, 1/18 duty)



2. Y address increment example
(8-bit word length, 1/18 duty)



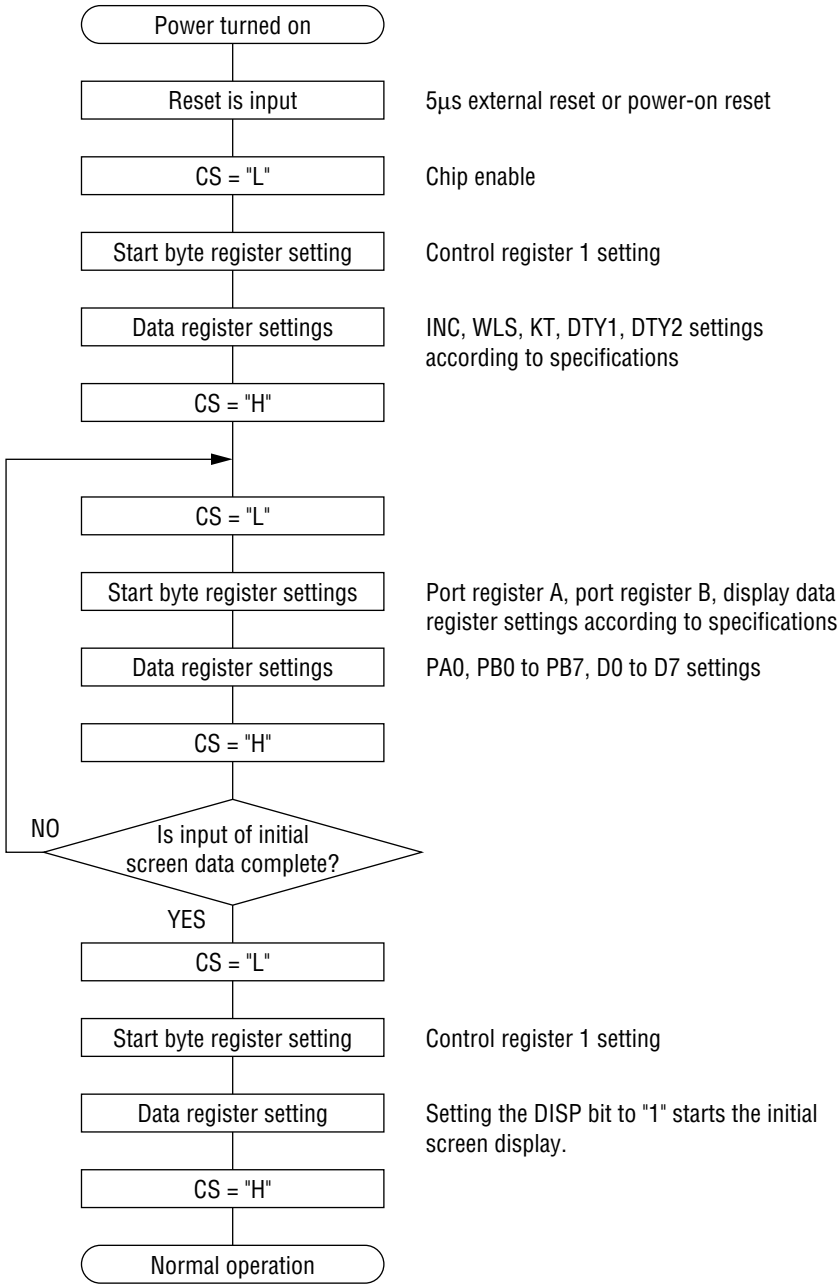
Output pin, I/O Pin and Register States When Reset is Input

Pin and register states while the $\overline{\text{RESET}}$ input is pulled to a "L" level are listed below.

Output pin, I/O pin	State
DI/O	Input state
KREQ	"L" (V_{SS})
OSC2	Oscillating state
$\overline{R0}$ to $\overline{R4}$	"L" (V_{SS})
PBA	High impedance
PB0 to PB7 (for ML9090-01)	High impedance
SEG1 to SEG80	"L" (V_{SS})
COM1 to COM10 (for ML9090-01)	"L" (V_{SS})
COM1 to COM18 (for ML9090-02)	"L" (V_{SS})

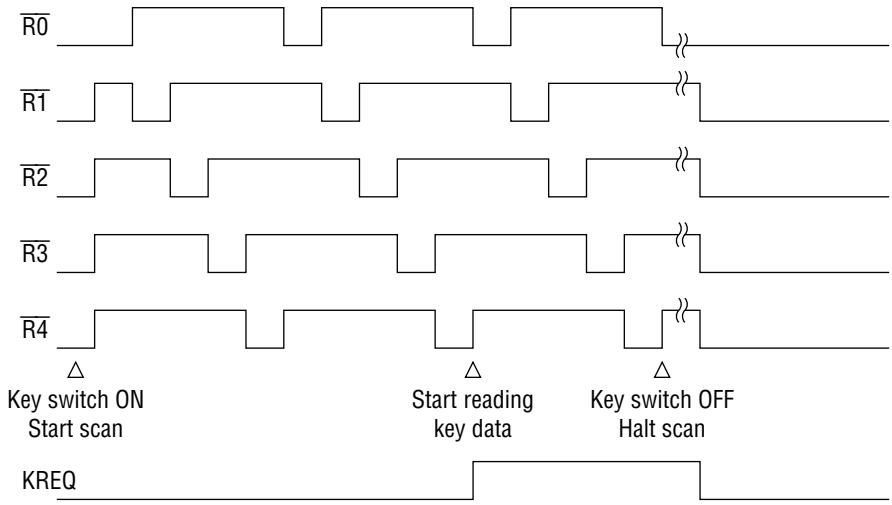
Register	State
Key scan register	Reset to "0"
Display data register	Display data is retained
X address register	Reset to "0"
Y address register	Reset to "0"
Port A register	Reset to "0"
Port B register	Reset to "0"
Control register 1	No change from value prior to reset input
Control register 2	Display OFF

Power-On Flow Chart



Key Scan

Key scan operation begins after a key switch turns ON. Key scan operation is halted after all key switches are detected as OFF. Two cycles after key scan operation starts, the KREQ signal changes from an "L" to "H" level. This signal can be used as a flag. The KREQ signal is reset when all key switches have been detected as OFF and an "L" level is input to the $\overline{\text{RESET}}$ pin.

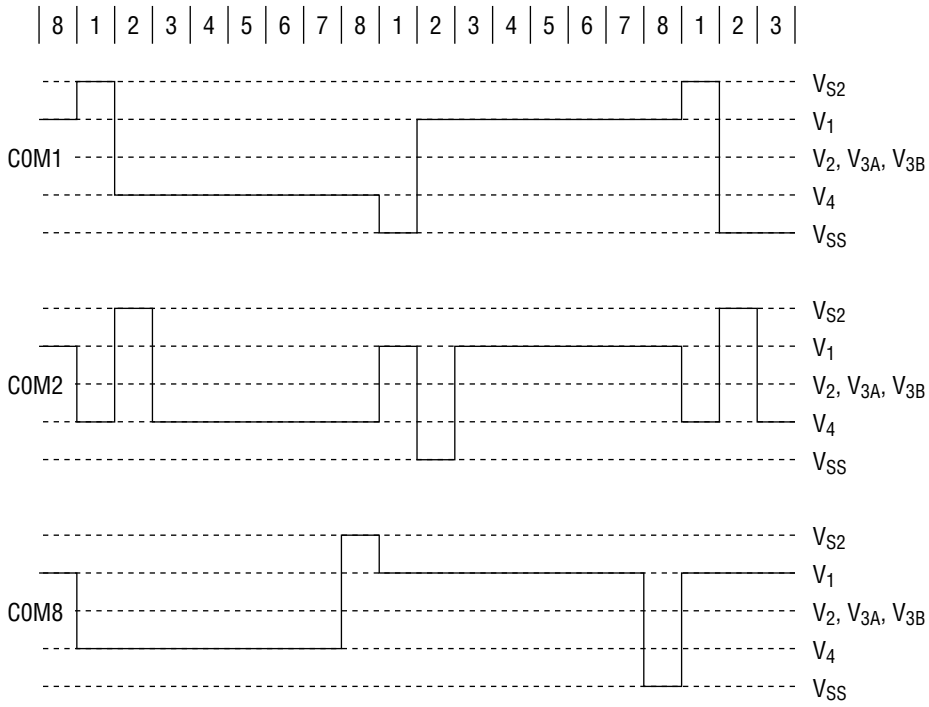


Note 1: Pressing three or more key switches simultaneously may result in incorrect recognition (a switch that was not pressed may be recognized as a switch that was pressed). Therefore, if it is necessary to recognize three or more pressed switches, connect a diode in series with each switch. If three or more pressed switches are not to be recognized, data should be ignored if there are three or more "1s" in the key data that is read by software.

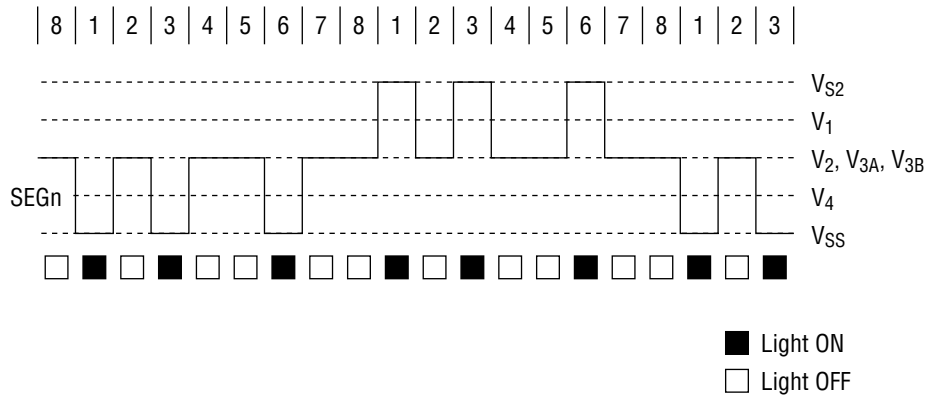
Note 2 : Because changes in the key status are detected as changes in the column inputs ($\overline{\text{C0}}$ to $\overline{\text{C4}}$), changes will not be detected if multiple switches connected to the same column are pressed.

Liquid Crystal Driving Waveform Example

1/8 duty (1/4 bias) (ML9090-01)

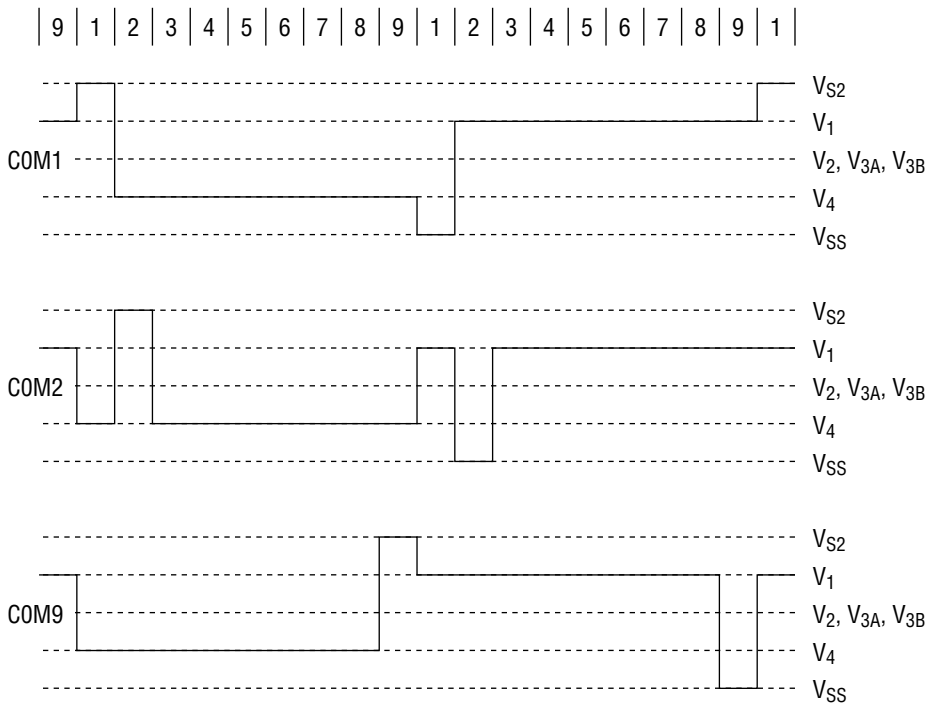


A non-selectable waveform is output from COM9 and COM10 outputs.

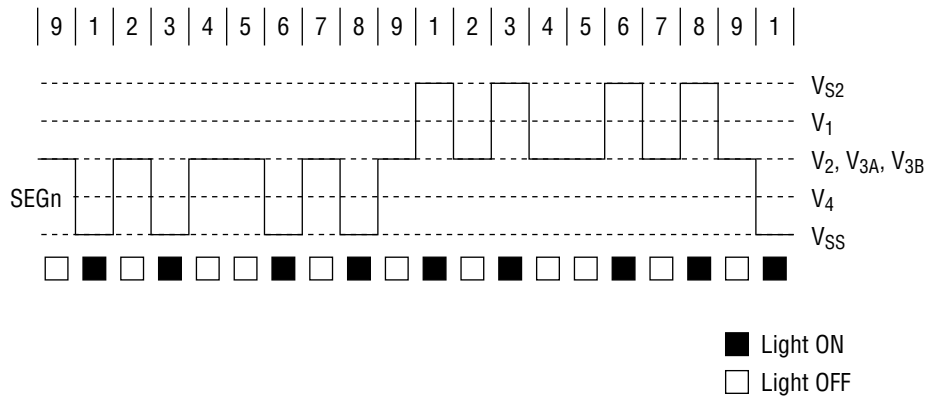


Liquid Crystal Driving Waveform Example

1/9 duty (1/4 bias) (ML9090-01)

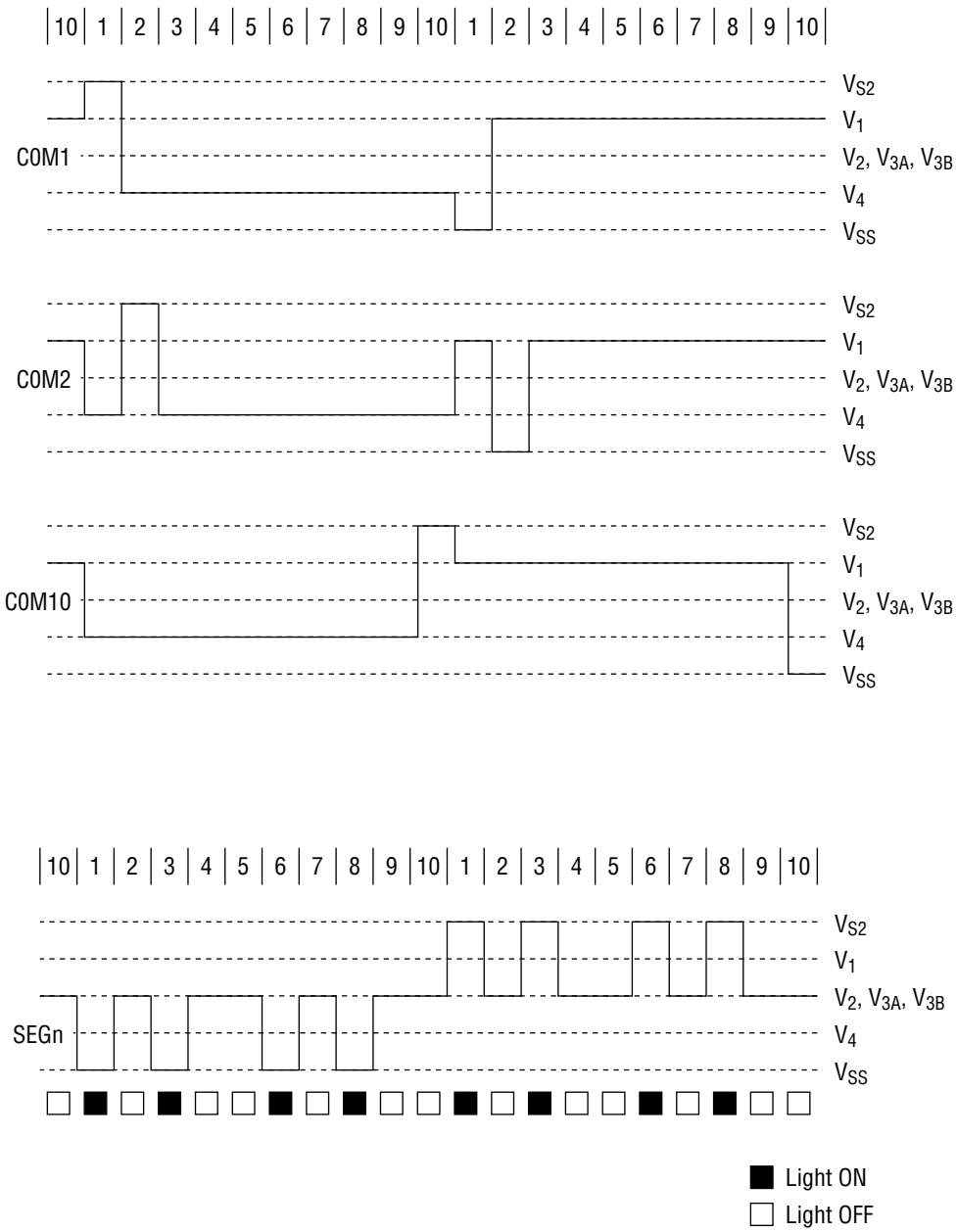


A non-selectable waveform is output from the COM10 output.



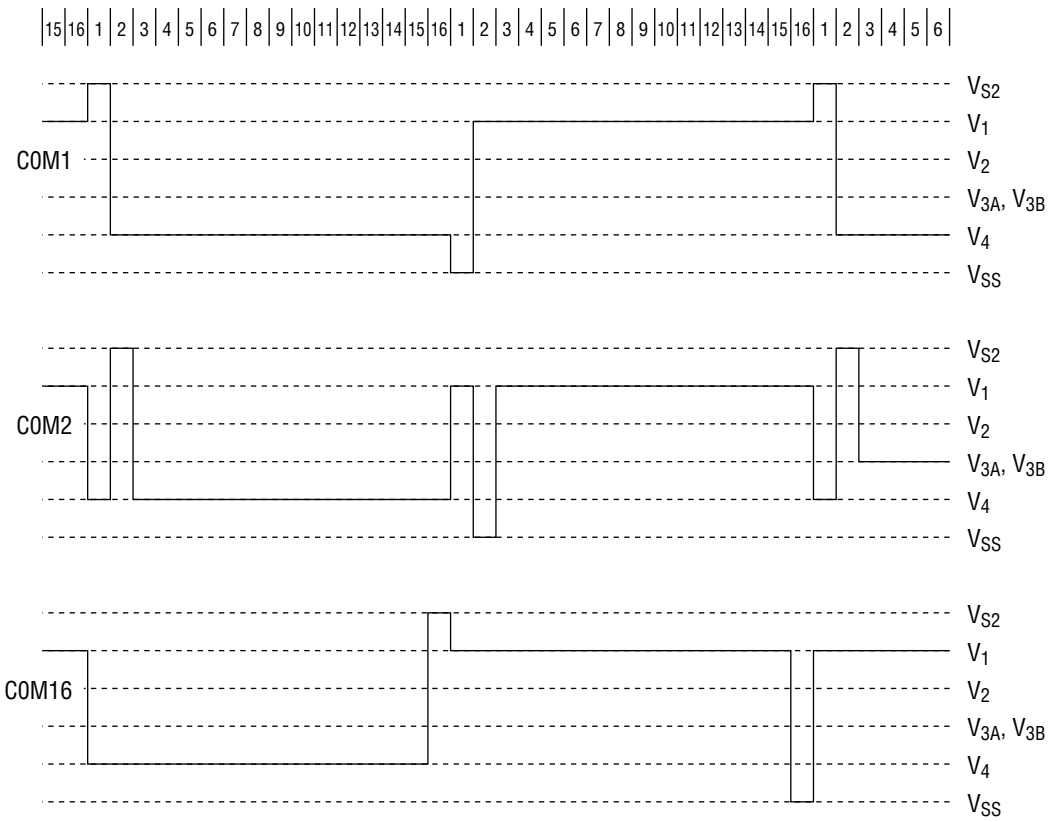
Liquid Crystal Driving Waveform Example

1/10 duty (1/4 bias) (ML9090-01)

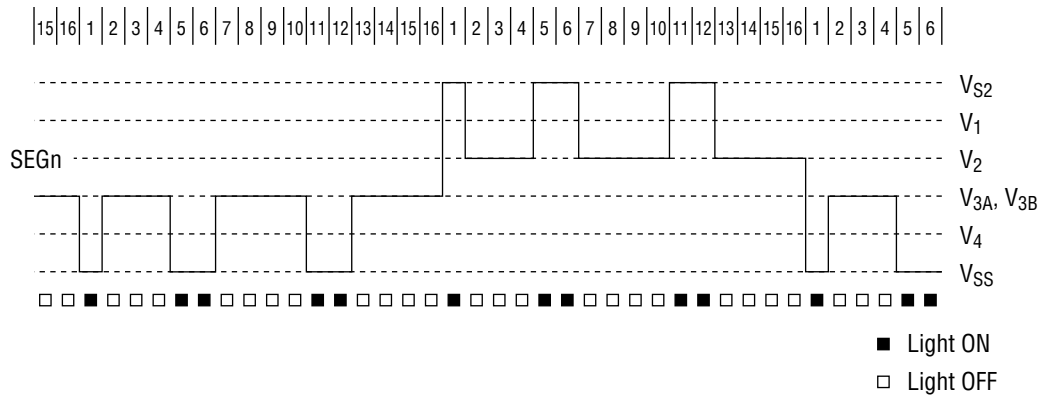


Liquid Crystal Driving Waveform Example

1/16 duty (1/5 bias) (ML9090-02)

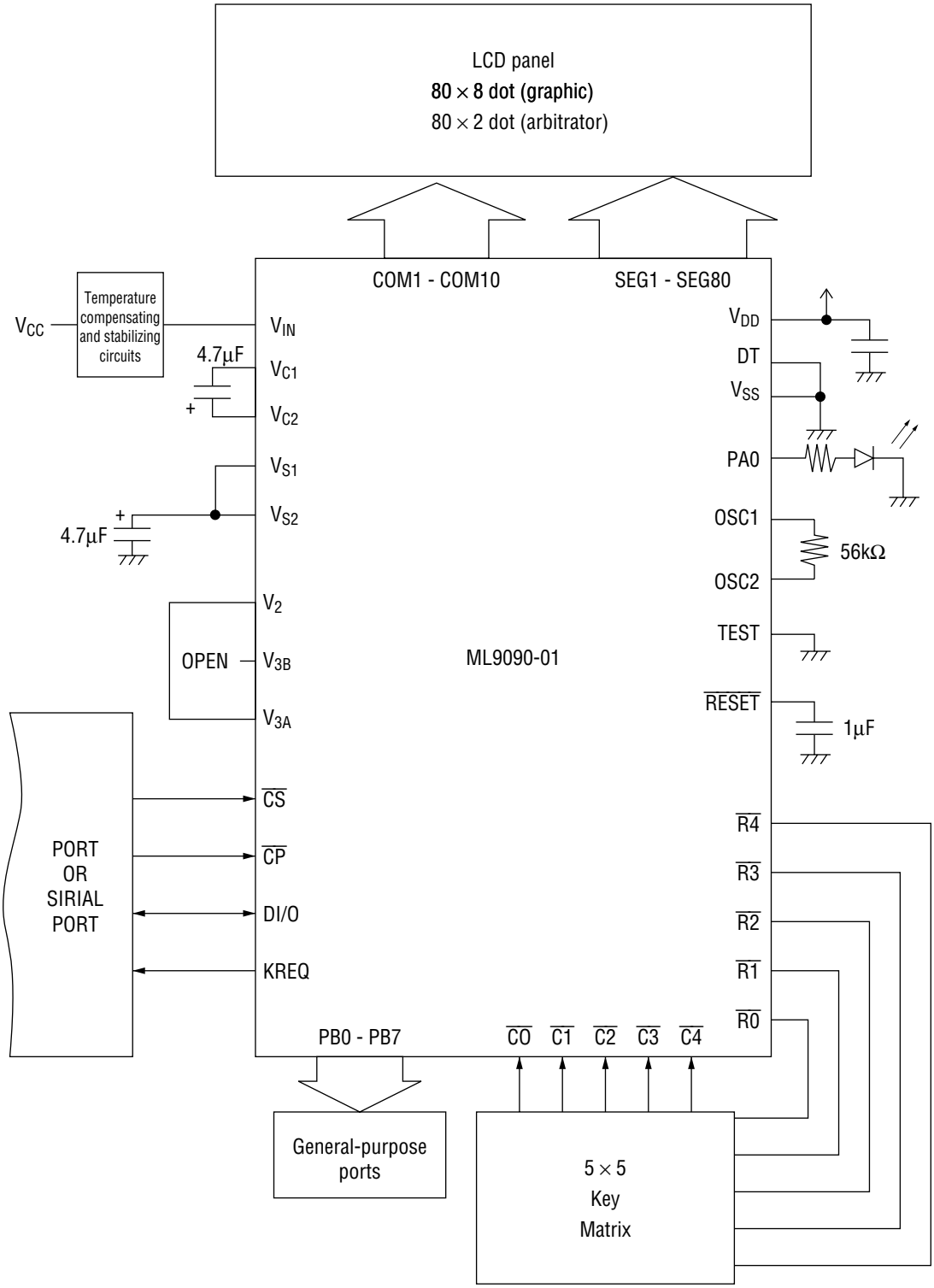


A non-selectable waveform is output from COM17 and COM18 outputs.

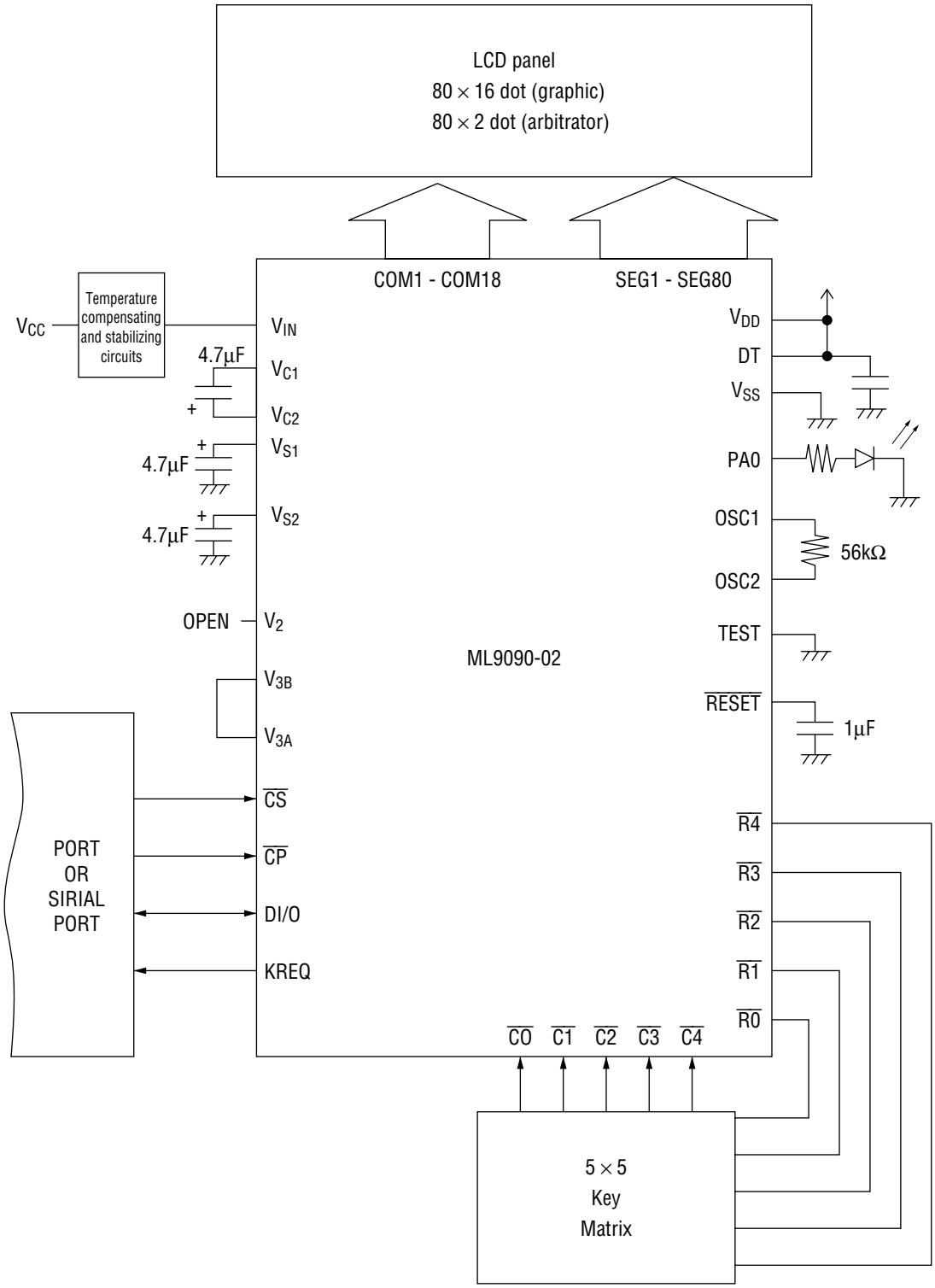


APPLICATION CIRCUITS

Application Example 1 (1/10 duty, voltage doubler)



Application Example 2 (1/18 duty, voltage tripler)



[Cautions]

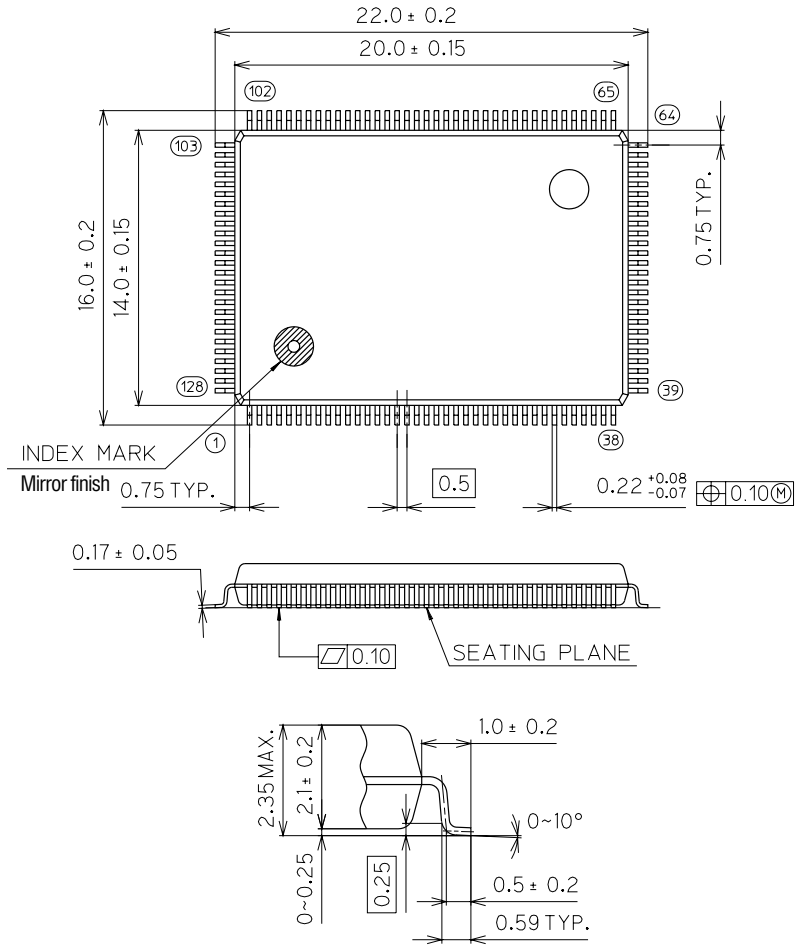
- When the power supply is ON or OFF, the following power supply sequence should be used.
  At the time of power supply ON:
  Logic power supply ON → multiplied reference voltage (V_{IN}) supply ON
  At the time of power supply OFF:
  Multiplied reference voltage (V_{IN}) supply OFF → logic power supply OFF or both OFF

- The lines between output pins, and between output pins and other pins (input pins, I/O pins or power supply pins) should not be short circuited.

PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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