Linear Output Magnetic Field Sensor

22151

FEATURES

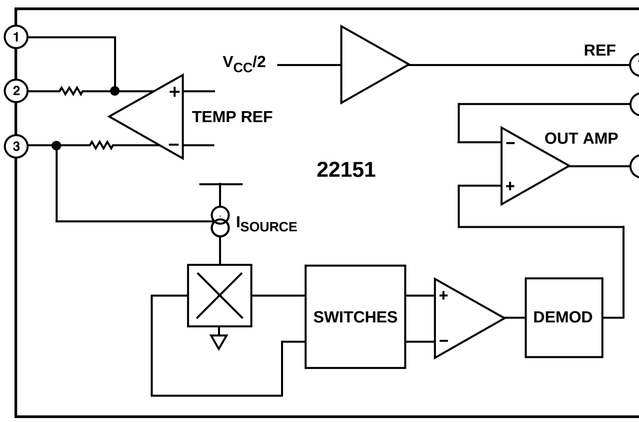
Adjustable Offset to Unipolar or Bipolar Operation
Low Offset Drift Over Temperature Range
Gain Adjustable Over Wide Range
Low Gain Drift Over Temperature Range
Adjustable First Order Temperature Compensation
Ratiometric to V_{CC}

APPLICATIONS

Automotive
- **Throttle Position Sensing**
- **Pedal Position Sensing**
- **Suspension Position Sensing**
- **Valve Position Sensing**

Industrial
- **Absolute Position Sensing**
- **Proximity Sensing**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The22151 is a linear magnetic field transducer. The sensor output is a voltage proportional to a magnetic field applied perpendicularly to the package top surface.

The sensor combines integrated bulk Hall cell technology and instrumentation circuitry to minimize temperature related drifts associated with silicon Hall cell characteristics. The architecture maximizes the advantages of a monolithic implementation while allowing sufficient versatility to meet varied application requirements with a minimum number of components.

Principle features include dynamic offset drift cancellation and a built-in temperature sensor. Designed for single +5 volt supply operation, the 22151 achieves low drift offset and gain operation over –40°C to +150°C. Temperature compensation can accommodate a number of magnetic materials commonly utilized in economic position sensor assemblies.

The transducer may be configured for specific signal gains dependent upon application requirements. Output voltage can be adjusted from fully bipolar (reversible) field operation to fully unipolar field sensing.

The voltage output achieves near rail-to-rail dynamic range, capable of supplying 1 mA into large capacitive loads. The signal is ratiometric to the positive supply rail in all configurations.

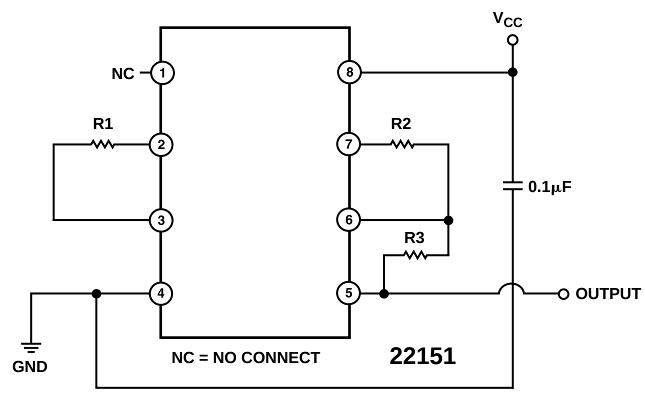


Figure 1. Typical Bipolar Configuration with Low (< –500 ppm) Compensation

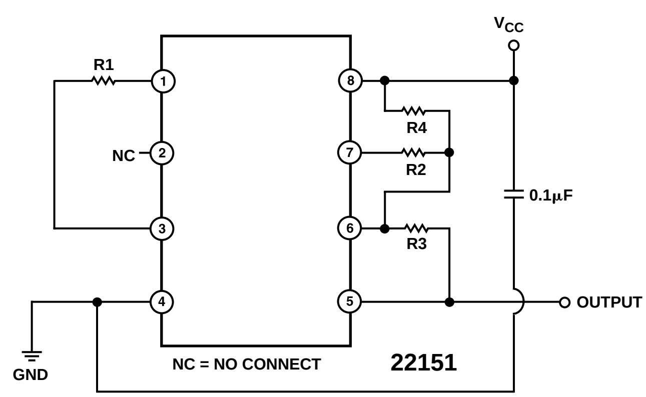


***Figure 2. Typical Unipolar Configuration with High** (≈ –2000 ppm) Compensation*

REV. 0

22151–SPECIFICATIONS (T_A = +25°C and V+ = +5 V unless otherwise noted)

Parameters	Min	Typ	Max	Units
OPERATION				
V_{CC} Operating	4.5	5.0	6.0	V
I_{CC} Operating		6.0	10	mA
INPUT				
TC3 (Pin 3) Sensitivity/Volt		160		µV/G/V
Input Range[1]		$\frac{V_{CC}}{2} \pm 0.5$		V
OUTPUT[2]				
Sensitivity (External Adjustment, Gain = 1)		0.4		mV/G
Linear Output Range	10		90	% of V_{CC}
Output Min		5		% of V_{CC}
Output Max (Clamp)		93		% of V_{CC}
Drive Capability		1.0		mA
Offset @ 0 Gauss		$\frac{V_{CC}}{2}$		V
Offset Adjust Range	5		95	% of V_{CC}
Output Short Circuit Current		5.0		mA
ACCURACIES				
Nonlinearity (10% to 90% Range)		0.1		% FS
Gain Error (Over Temperature Range)		±1		%
Offset Error (Over Temperature Range)		±6.0		G
Uncompensated Gain TC (G_{TCU})		950		ppm
RATIOMETRICITY ERROR			1	%V/V_{CC}
3 dB ROLL-OFF (5 mV/G)		5.7		kHz
OUTPUT NOISE FIGURE (6 kHz BW)		2.4		mV/rms
PACKAGE		8-Lead SOIC		
OPERATING TEMPERATURE RANGE	–40		+150	°C

NOTES
[1]–40°C to +150°C.
[2]R_L = 4.7 kΩ.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATING*

Supply Voltage . . . . 12 V
Package Power Dissipation . . . . 25 mW
Storage Temperature . . . . –50°C to +160°C
Output Sink Current, I_O . . . . 15 mA
Magnetic Flux Density . . . . Unlimited
Lead Temperature (Soldering 10 sec) . . . . +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

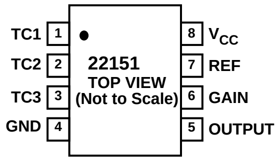
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
22151YR	–40°C to +150°C	8-Lead SOIC	SO-8

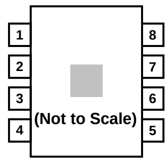
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the 22151 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



AREA OF SENSITIVITY*



* SHADED AREA REPRESENTS MAGNETIC FIELD AREA OF SENSITIVITY (20MILS × 20MILS)

• POSITIVE B FIELD INTO TOP OF PACKAGE RESULTS IN A POSITIVE VOLTAGE RESPONSE

PIN FUNCTION DESCRIPTIONS

Pin No.	Description	Connection
1	Temperature Compensation 1	Output
2	Temperature Compensation 2	Output
3	Temperature Compensation 3	Input/Output
4	Ground	
5	Output	Output
6	Gain	Input
7	Reference	Output
8	Positive Power Supply	

CIRCUIT OPERATION

The 22151 consists of epi Hall plate structures located at the center of the die. The Hall plates are orthogonally sampled by commutation switches via a differential amplifier. The two amplified Hall signals are synchronously demodulated to provide a resultant offset cancellation (see Figure 3). The demodulated signal passes through a noninverting amplifier to provide final gain and drive capability. The frequency at which the output signal is refreshed is 50 kHz.

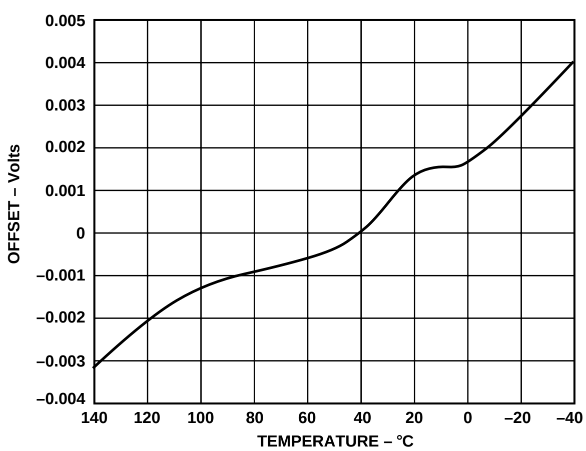


Figure 3. Relative Quiescent Offset vs. Temperature

TEMPERATURE DEPENDENCIES

The uncompensated gain temperature coefficient (G_{TCU}) of the AD22151 is the result of fundamental physical properties associated with silicon bulk Hall plate structures. Low doped Hall plates operated in current bias mode exhibit a temperature relationship determined by the action of scattering mechanisms and doping concentration.

The relative value of sensitivity to magnetic field can be altered by the application of mechanical force upon silicon. The mechanism is principally the redistribution of electrons throughout the "valleys" of the silicon crystal. Mechanical force on the sensor is attributable to package-induced stress. The package material acts to distort the encapsulated silicon altering the Hall cell gain by ±2% and G_{TCU} by ±200 ppm.

Figure 4 shows the typical G_{TCU} characteristic of the AD22151. This is the observable alteration of gain with respect to temperature with Pin 3 (TC3) held at a constant 2.5 V (uncompensated).

If a permanent magnet source used in conjunction with the sensor also displays an intrinsic TC (B_{TC}), it will require factoring into the total temperature compensation of the sensor assembly.

Figures 5 and 6 represent typical overall temperature/gain performance for a sensor and field combination (B_{TC} = –200 ppm). Figure 5 is the total drift in volts over a –40°C to +150°C temperature range with respect to applied field. Figure 6 represents typical percentage gain variation from +25°C. Figures 7 and 8 show similar data for a B_{TC} = –2000 ppm.

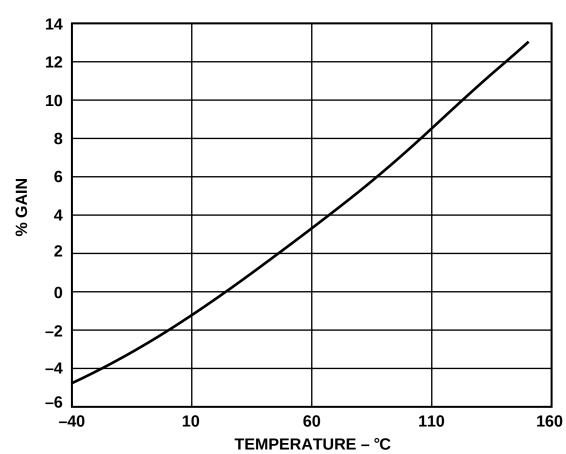


Figure 4. Uncompensated Gain Variation (from +25°C) vs. Temperature

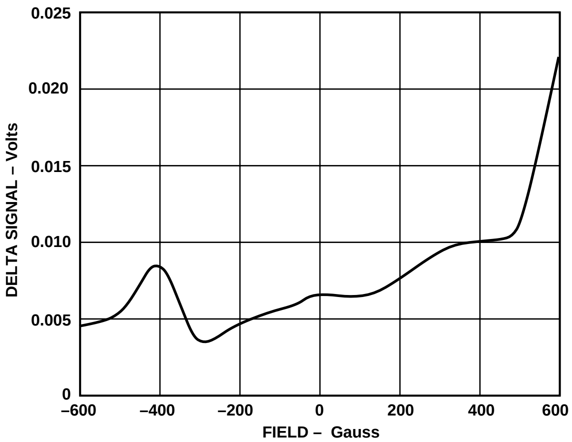


Figure 5. Signal Drift Over Temperature (–40°C to +150°C) vs. Field (–200 ppm); +5 V Supply

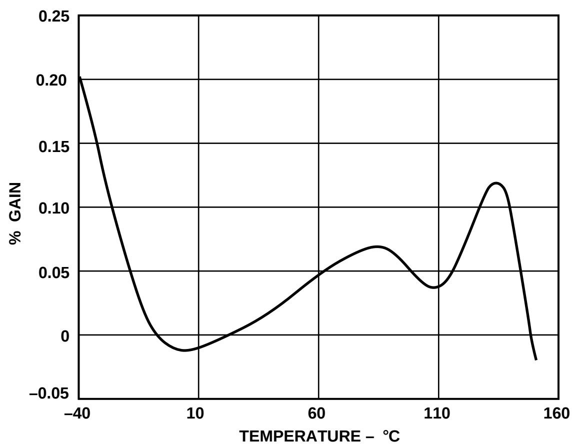


Figure 6. Gain Variation from +25°C vs. Temperature (–200 ppm) Field; R1 –15 kΩ

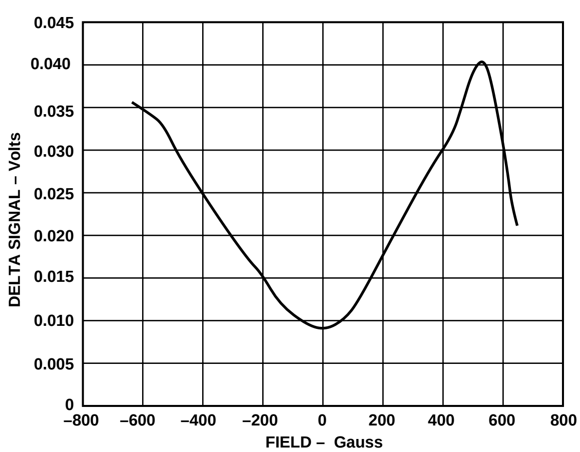


Figure 7. Signal Drift Over Temperature (–40°C to +150°C) vs. Field (–2000 ppm); +5 V Supply

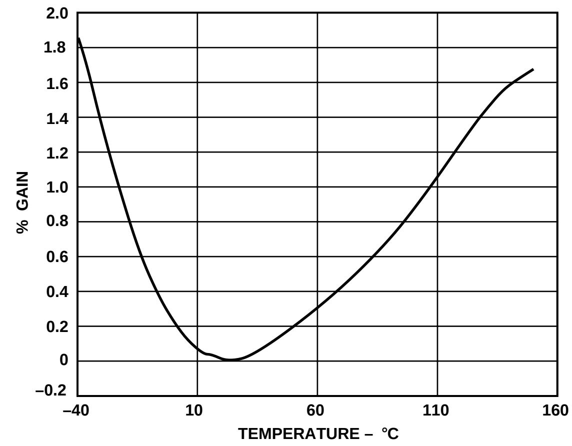


Figure 8. Gain Variation (from +25°C) vs. Temperature (–2000 ppm Field; R1 = 12 kΩ)

TEMPERATURE COMPENSATION

The 22151 incorporates a "thermistor" transducer that detects relative chip temperature within the package. This function provides a compensation mechanism for the various temperature dependencies of the Hall cell and magnet combinations. The temperature information is accessible at Pins 1 and 2 (≈ +2900 ppm /°C) and Pin 3 (≈ –2900 ppm/°C) as represented by Figure 9. The compensation voltages are trimmed to converge at $V_{CC}/2$ at +25°C. Pin 3 is internally connected to the negative TC voltage via an internal resistor (see Functional Block Diagram). An external resistor connected between Pin 3 and Pins 1 or 2 will produce a potential division of the two complementary TC voltages to provide optimal compensation. The aforementioned Pin 3 internal resistor provides a secondary TC designed to reduce second order Hall cell temperature sensitivity.

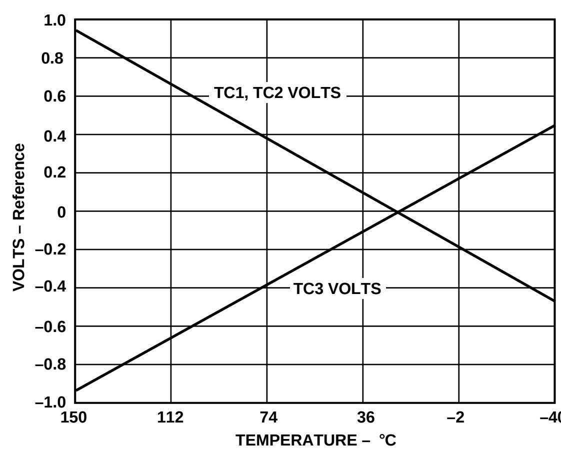


Figure 9. TC1, TC2 and TC3 with Respect to Reference vs. Temperature

The voltages present at Pins 1, 2 and 3 are proportional to the supply voltage. The presence of the Pin 2 internal resistor distinguishes the effective compensation ranges of Pins 1 and 2 (see temperature configuration in Figures 1 and 2, and typical resistor values in Figures 10 and 11).

Variation occurs in the operation of the gain temperature compensation for two reasons. First, the die temperature within the package is somewhat higher than the ambient temperature due to self-heating as a function of power dissipation. Second, package stress effect alters the specific operating parameters of the gain compensation, particularly the specific cross over temperature of TC1, TC3 (≈ ±10°C).

CONFIGURATION AND COMPONENT SELECTION

There are three areas of sensor operation that require external component selection. Temperature compensation (R1), signal gain (R2 and R3), and offset (R4).

Temperature

If the internal gain compensation is used, an external resistor is required to complete the gain TC circuit at Pin 3. A number of factors contribute to the value of this resistor.

a. The intrinsic Hall cell sensitivity TC ≈ 950 ppm.
b. Package induced stress variation in a. ≈ ±150 ppm.
c. Specific field TC ≈ –200 ppm (Alnico), –2000 ppm (Ferrite), 0 ppm (electromagnet) etc.
d. R1, TC.

The final value of target compensation also dictates the use of either Pin 1 or Pin 2. Pin 1 is provided to allow for large negative field TC such as ferrite magnets, thus R1 would be connected to Pins 1 and 3.

Pin 2 uses an internal resistive TC to optimize smaller field coefficients such as Alnico, down to 0 ppm coefficients when only the sensor gain TC itself is dominant. The TC of R1 itself will also effect the compensation and as such a low TC resistor (±50 ppm) is recommended.

Figures 10 and 11 indicate R1 resistor values and their associated effectiveness for Pins 1 and 2 respectively. Note that the indicated drift response in both cases incorporates the intrinsic Hall sensitivity TC (B_{TCU}).

For example, the 22151 sensor is to be used in conjunction with an Alnico material permanent magnet. The TC of such magnets is ≈ –200 ppm (see Figures 5 and 6). Figure 11 indicates that a compensating drift of +200 ppm at Pin 3 requires a nominal value of R1 = 18 kΩ (assuming negligible drift of R1 itself).

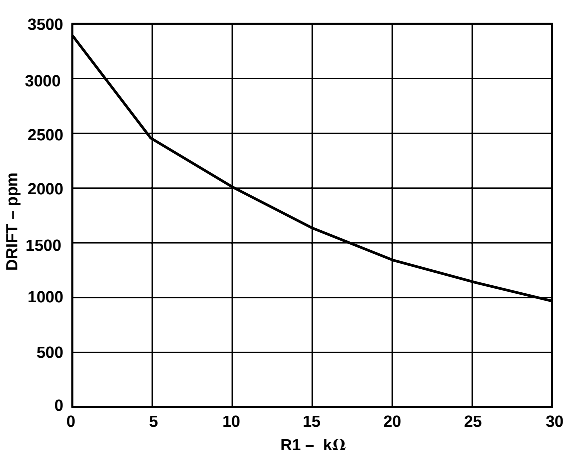


Figure 10. Typical Resistor Value R1 vs. (Pins 1 and 3) Drift Compensation

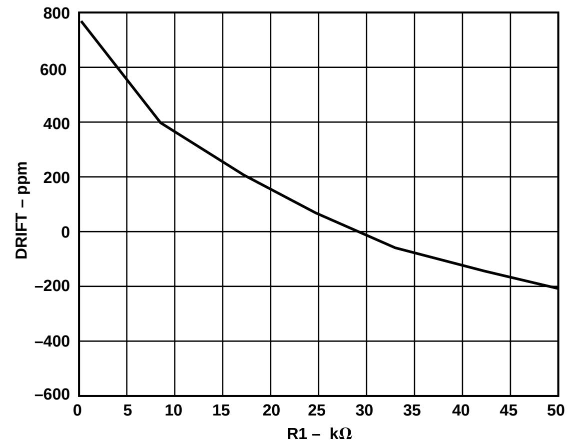


Figure 11. Typical Resistor Value R1 (Pins 2 and 3) vs. Drift Compensation

GAIN AND OFFSET

The operation of the 22151 can be bipolar (i.e., 0 Gauss = $V_{CC}/2$) or a ratiometric offset can be implemented to Position Zero Gauss point at some other potential (i.e., 0.25 V).

The gain of the sensor can be set by the appropriate R2 and R3 resistor values (see Figure 1) such that:

$$Gain = 1 + \frac{R3}{R2} \times 0.4\, mV/G \tag{1}$$

However, if an offset is required to position the quiescent output at some other voltage then the gain relationship is modified to:

$$Gain = 1 + \frac{R3}{(R2 \| R4)} \times 0.4\, mV/G \tag{2}$$

The offset that R4 introduces is:

$$Offset = \frac{R3}{(R3 + R4)} \times \left(V_{CC} - V_{OUT}\right) \tag{3}$$

For example:

At V_{CC} = 5 V at room temperature, the internal gain of the sensor is approximately 0.4 mV/Gauss. If a sensitivity of 6 mV/Gauss is required with a quiescent output voltage of 1 V, the following calculations apply (see Figure 2).

A value for R3 would be selected that complied with the various considerations of current and power dissipation, trim ranges (if applicable), etc. For the purpose of example assume a value of 85 kΩ.

To achieve a quiescent offset of 1 V requires a value for R4 as:

$$\frac{\left(\frac{V_{CC}}{2}\right) - 1}{V_{CC} - 1} = 0.375 \tag{4}$$

Thus:

$$R4 = \left(\frac{85\ k\Omega}{0.375}\right) - 85\ k\Omega = 141.666\ k\Omega \tag{5}$$

The gain required would be 6/0.4 (mV/Gauss) = 15

Knowing the values of R3 and R4 from above, and noting Equation 2, the parallel combination of R2 and R4 required is:

$$\frac{85\ k\Omega}{(15-1)} = 6.071\ k\Omega$$

Thus:

$$R2 = \left(\frac{1}{\left(\frac{1}{6.071\ k\Omega}\right) - \left(\frac{1}{141.666\ k\Omega}\right)}\right) = 6.342\ k\Omega$$

NOISE

The principle noise component in the sensor is thermal noise from the Hall cell. Clock feedthrough into the output signal is largely suppressed with application of a supply bypass capacitor.

Figure 12 shows the power spectral density (PSD) of the output signal for a gain of 5 mV/Gauss. The effective bandwidth of the sensor is approximately 5.7 kHz. This is shown by Figure 13 small signal bandwidth vs. gain. The PSD indicates an rms noise voltage of 2.8 mV within the 3 dB bandwidth of the sensor. A wideband measurement of 250 MHz indicates 3.2 mV rms (see Figure 14a).

In many position sensing applications bandwidth requirements can be as low as 100 Hz. Passing the output signal through an LP filter, for example 100 Hz, would reduce the rms noise voltage to ≈1 mV. A dominant pole may be introduced into the output amplifier response by connection of a capacitor across feedback resistor R3, as a simple means of reducing noise at the expense of bandwidth. Figure 14b indicates the output signal of a 5 mV/G sensor bandwidth limited to 180 Hz with a 0.01 µF feedback capacitor.

Note: Measurements taken with 0.1 µF decoupling capacitor between V_{CC} and GND at +25°C.

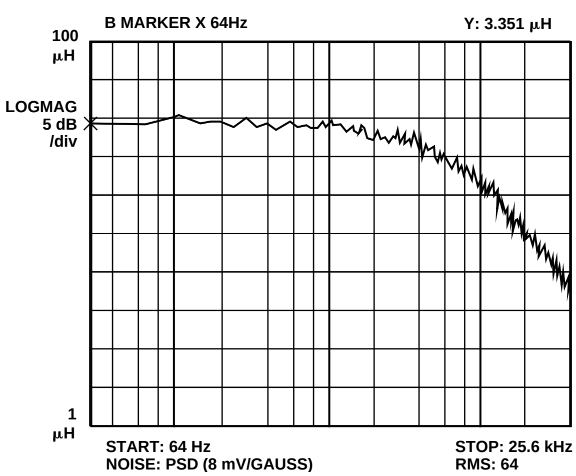


Figure 12. Power Spectral Density (5 mV/G)

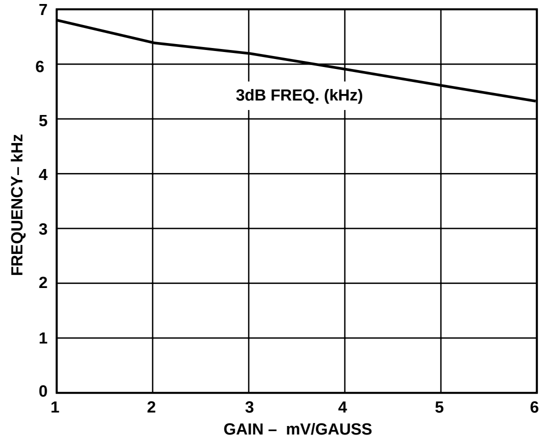


Figure 13. Small-Signal Gain Bandwidth

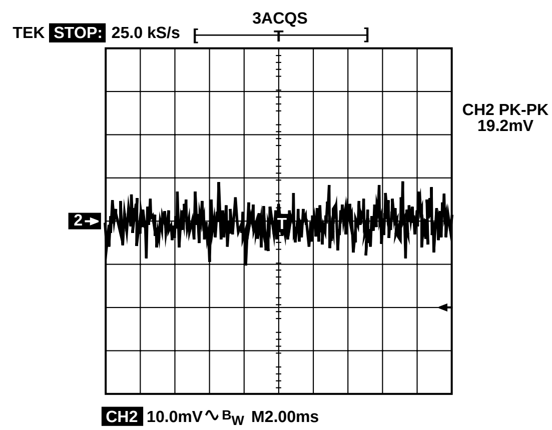


Figure 14a. Peak-to-Peak Full Bandwidth (10 mV/Division)

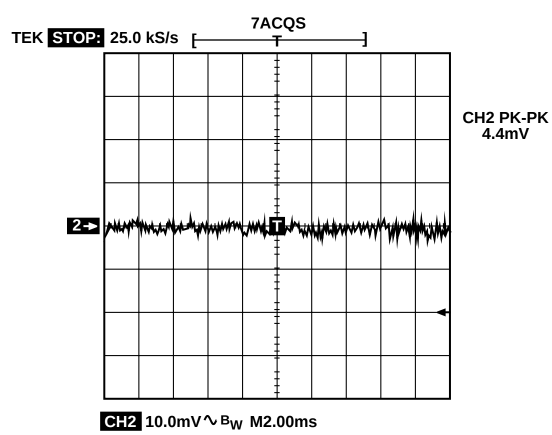


Figure 14b. Peak-to-Peak 180 Hz Bandwidth (10 mV/Division)

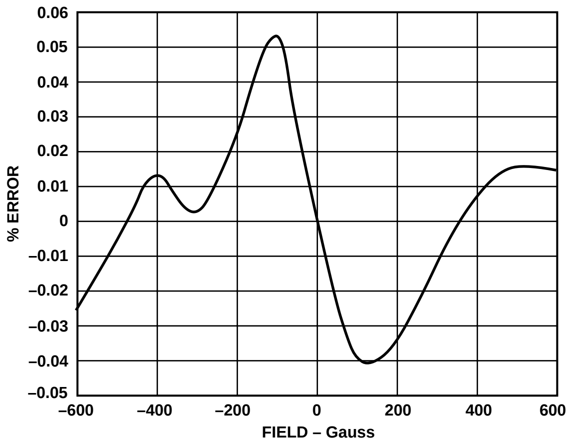


Figure 15. Integral Nonlinearity vs. Field

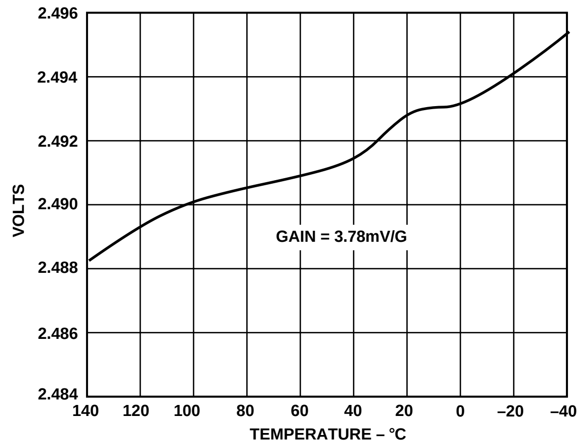
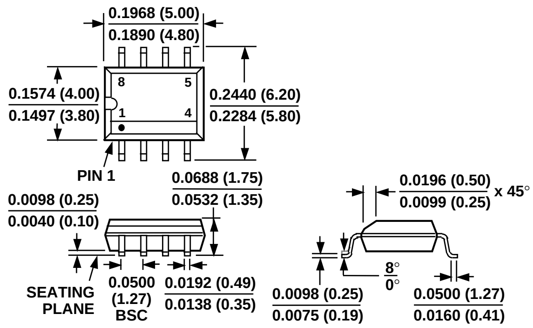


Figure 16. Absolute Offset Volts vs. Temperature

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
(SO-8)



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