# LED Driver IC

## DESGRIPTION

is an LED Controller driven on a 1/7to 1/8 duty factor. Eleven segment output lines, six grid output lines, 1 segment/grid output lines, one display memory, control circuit , key SGan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to DL8836 via a four-line serial interface. Housed in a 32-pin SO Package, DL8836 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

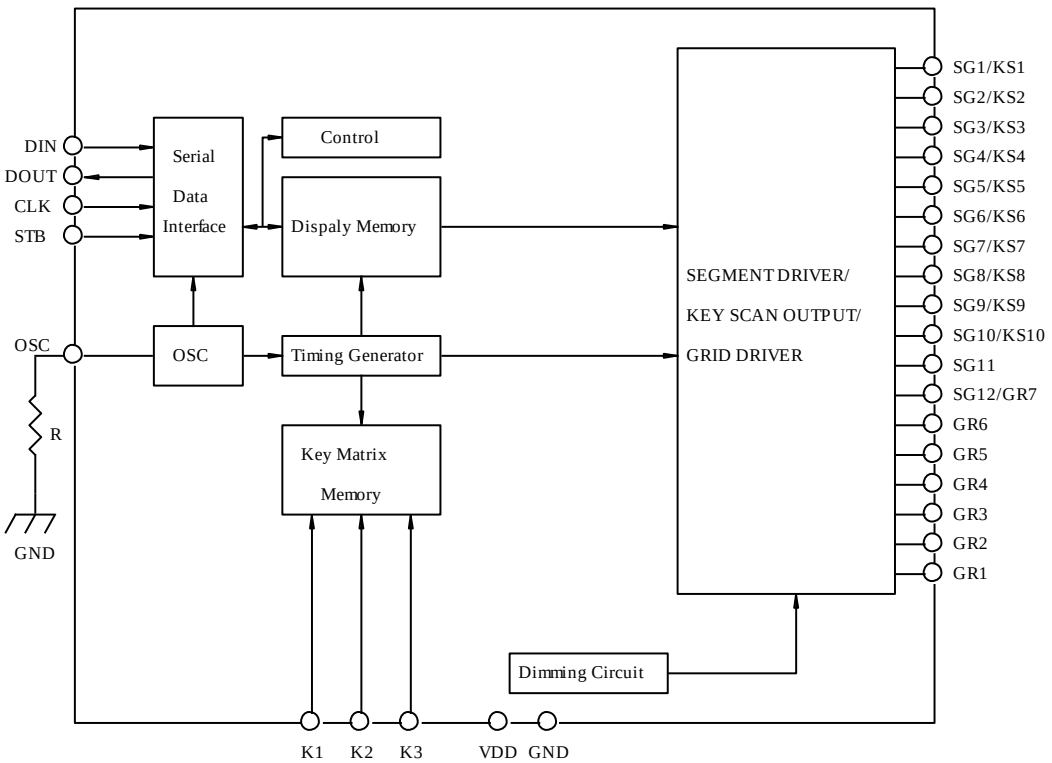
## FEATURES

- CMOS Technology
- Low Power Consumption
- Multiple Display Modes ( 12 segment, 6 Grid to 11 segment, 7 Grid )
- Key SGanning ( 10x 3 Matrix )
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- Available in 32-Pin, SOP Package

## APPLICATION

- Micro-computer Peripheral Device
- VCR set
- Combi set

## BLOCK DIAGRAM





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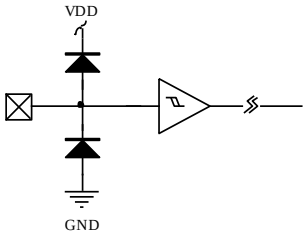
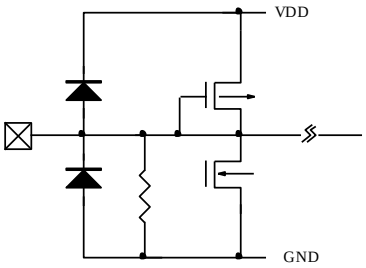
# INPUT/OUTPUT CONFIGURATIONS

The SGhematic diagrams of the input and output circuits of the logic section are shown below.

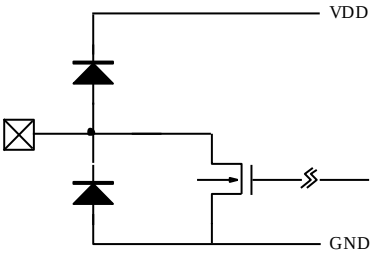
***Input Pins: CLK, STB & DIN***



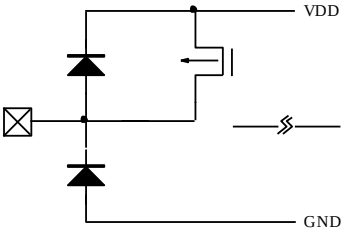

***Input Pins: K1 to K3***



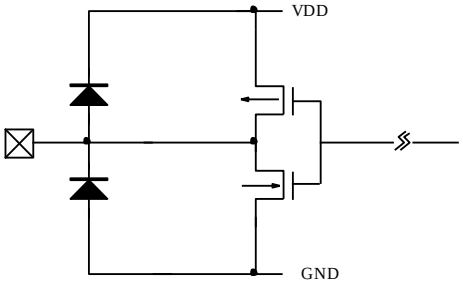

***Output Pins: DOUT, GR1 to GR4***



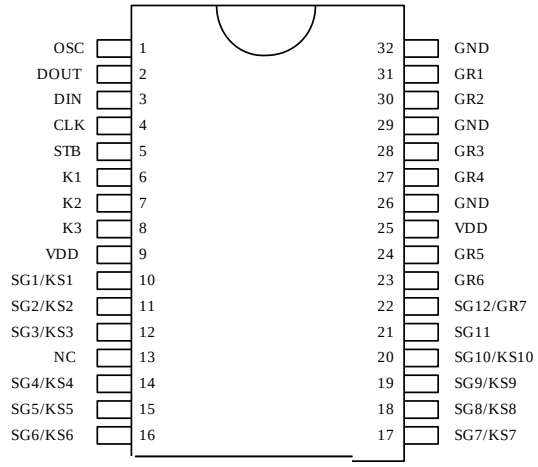

***Output Pins: SG1 to SG11***




***Output Pins: GR5, GR6 and SG12/GR7***



# PIN CONFIGURATION




IC：DL8836

# PIN DESGRIPTION

| Pin Name | I/O | DeSGription | Pin No. |
|---|---|---|---|
| OSG | I | OSGillator Input Pin<br>A resistor is connected to this pin to determine the oSGillation frequency | 1 |
| DOUT | O | Data Output Pin ( N-Channel, Open-Drain )<br>This pin outputs serial data at the falling edge of the shift clock. | 2 |
| DIN | I | Data Input Pin. This Pin inputs serial data at the rising edge of the shift clock ( starting from the lower bit) | 3 |
| CLK | I | Clock Input Pin<br>This pin reads serial data at the rising edge and outputs data at the falling edge. | 4 |
| STB | I | Serial Interface Strobe Pin<br>The data input after the STB has fallen is processed as a command<br>When this pin is “HIGH”, CLK is ignored. | 5 |
| K1 to K3 | I | Key Data Input Pins. The data sent to these pins are latched at the end of the display cycle. ( Internal Pull-Low Resistor) | 6, 7, 8 |
| GND | - | Ground Pin | 26,29,32 |
| SG1/KS1 to SG10/KS10 | O | Segment Output Pins ( p-channel, open drain )<br>Also acts as the Key Source | 10~12<br>14~20 |
| SG11 | O | Segment Output Pins ( p-channel, open drain ) | 21 |
| SG12/GR7 | O | Segment/Grid Output Pins | 22 |
| VDD | - | Power Supply | 9,25 |
| GR6 to GR1 | O | Grid Output Pins | 23,24,27<br>28,30,31 |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| | | | |
|---|---|---|---|
| NC | - | No Connection | 13 |



# FUNCTIONAL DESGRIPTION

## COMMANDS

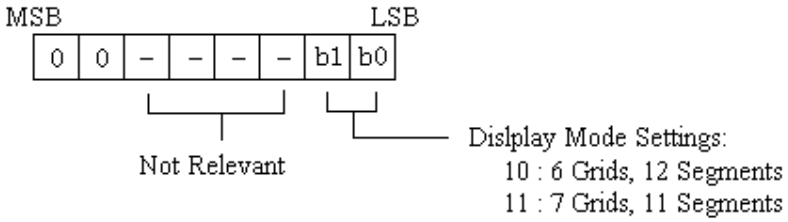
A command is the first byte ( b0 to b7 ) inputted to DL8836 via the DIN Pin after STB pin has changed from HIGH to LOW Stage. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communications is initialized, and the data/commands being transmitted are considered invalid.

### *Command 1: Display Mode Setting Commands*

DL8836 provides 2 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte ( b0 to b7 ) transmitted to DL8836 via the DIN Pin when STB is LOW. However, for these commands, the bit 3 to bit 6 (b2 to b5) are ignored, bit 7 & bit 8 (b6 to b7) are given value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (12 to 11 segments, 6 to 7 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

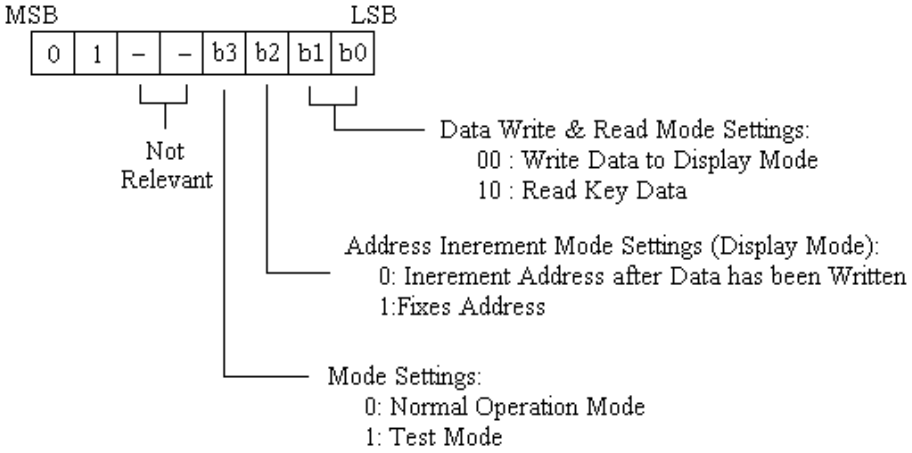
When Power is turned ON, the 7-grid, 11-segment modes is selected.




### *Command 2: Data Setting Commands*

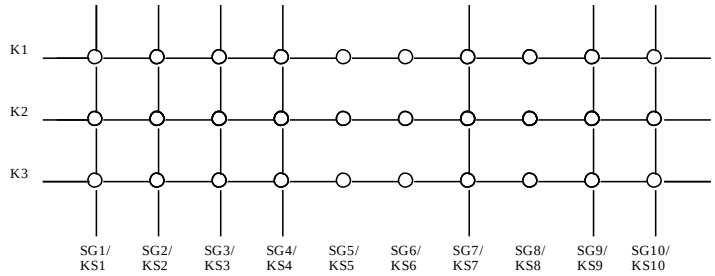
The Data Setting Commands executes the Data Write or Data Read Modes for DL8836. The data Setting Command, the bits 5 and 6 (b4,b5) are ignored, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.

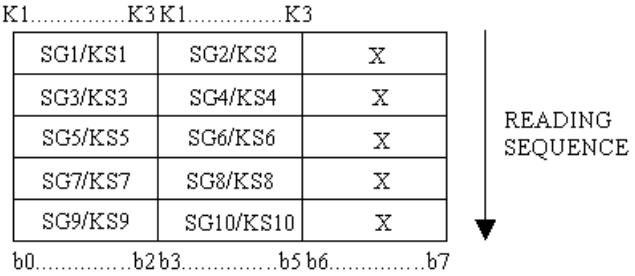


## DL8836 KEYMATRIX & KEYINPUT DATA STORAGE RAM

DL8836 Key Matrix consists of 10 x 3 array as shown below:




Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.

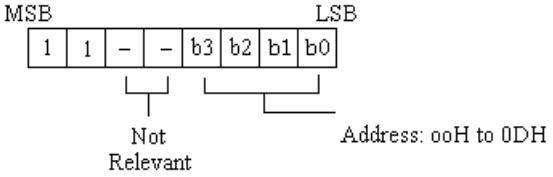



Note: b6 and b7 do not care

### *Command 3: Address Setting Commands*

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at at 00H.

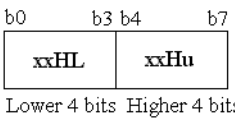
Please refer to the diagram below.




## DISPALYMODE AND RAMADDRESS

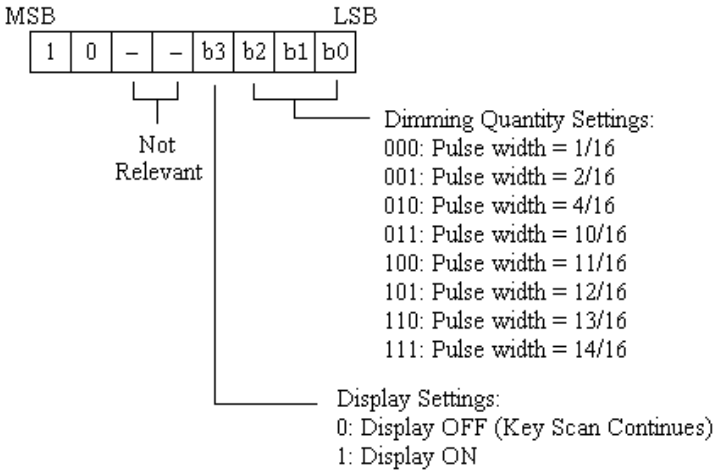
Data transmitted from an external device to DL8836 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of DL8836 are given below in 8 bits unit.

| SG1 | SG4 SG5 | SG8 SG9 SG12 | |
|---|---|---|---|
| 00HL | 00Hu | 01HL | DIG1 |
| 02HL | 02Hu | 03HL | DIG2 |
| 04HL | 04Hu | 05HL | DIG3 |
| 06HL | 06Hu | 07HL | DIG4 |
| 08HL | 08Hu | 09HL | DIG5 |
| 0AHL | 0AHu | 0BHL | DIG6 |
| 0CHL | 0CHu | 0DHL | DIG7 |



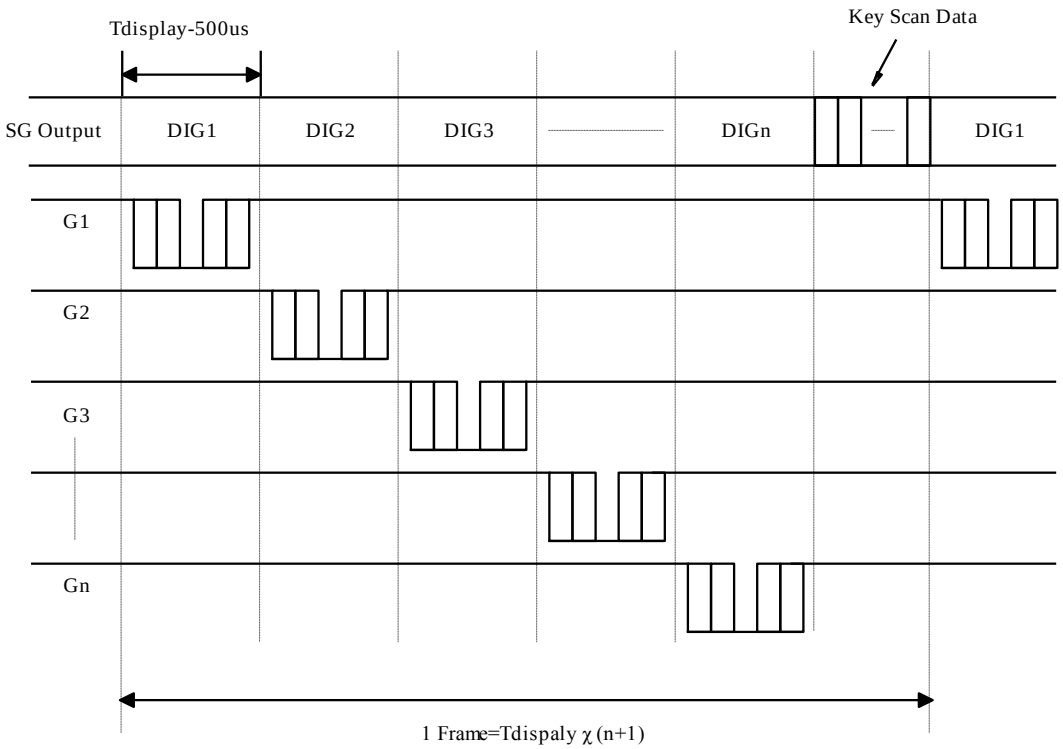
***Command 4: Display Control Commands***

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 Pulse width is selected and the displayed is turned OFF (the key SGanning is started).




## SGANNING AND DISPLAY TIMING

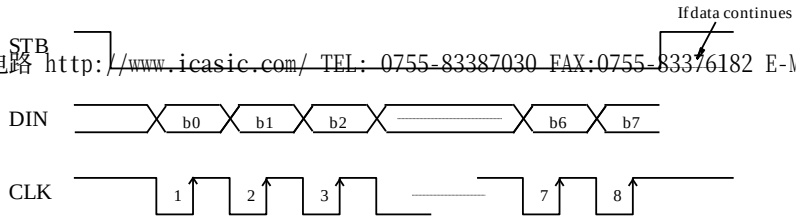
The key SGanning and Display Timing diagram is given below. One cycle of key SGanning consists of 2 frames. The data of the are 10 x 3 matrix is stored in the RAM.



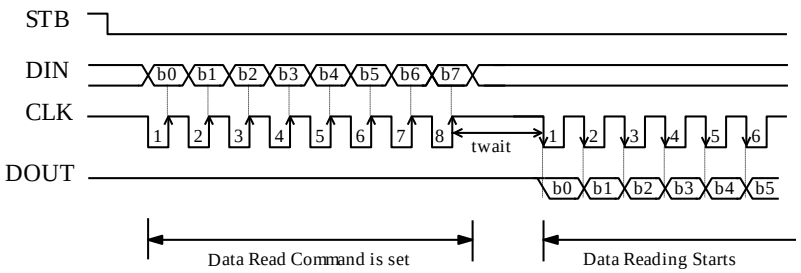

## SERIAL COMMUNICATION FROMAT

The following diagram shows the DL8836 serial communication format. The DOUT Pin is an N-channel, opendrain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KOhms to 10 KOhms) must be connected to DOUT.

***RECEPTION (Data/Command Write)***




***TRANSMISSION (Data Read)***

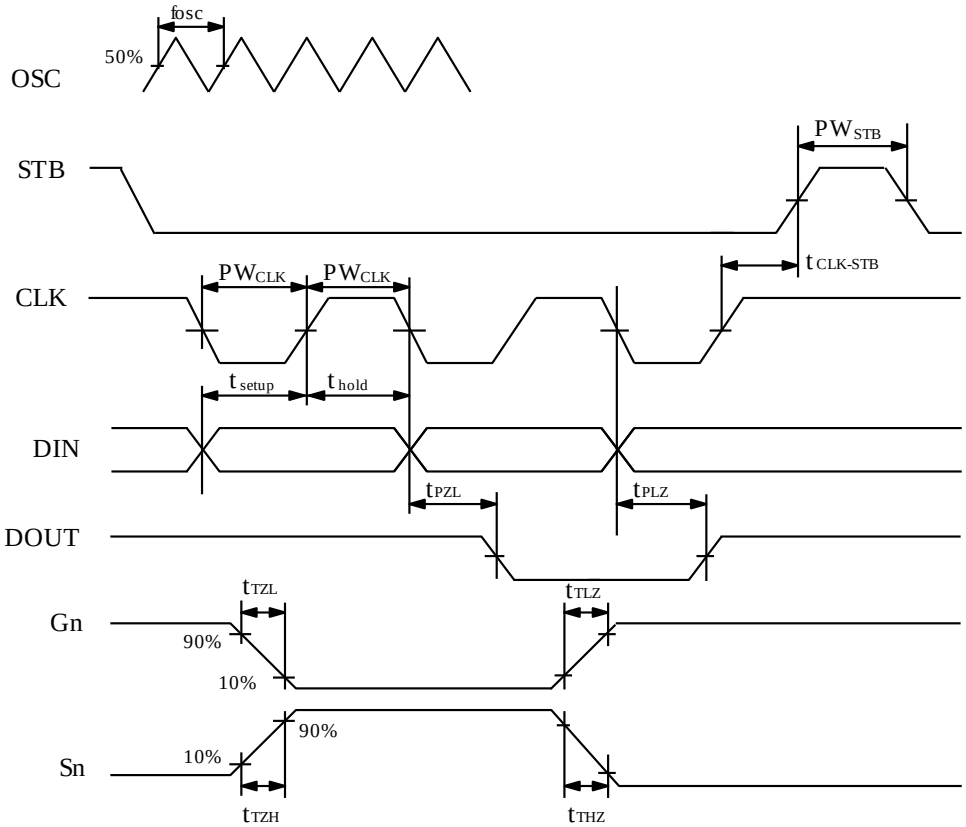



where: $t_{wait}$ (waiting time) ≥ 1μ s

It must be noted that when the data is read, the waiting time ($t_{wait}$) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μ s.

## SWITCHING CHARACTERISTIC WAVEFORM

DL8836 Switching Characteristics Waveform is given below.




where: $PW_{CLK}$ (Clock Pulse Width) ≥ 400nS $PW_{STB}$ (Strobe Pulse Width) ≥1μ s

$t_{setup}$ (Data Setup Time) ≥100nS $t_{hold}$ (Data Hold Time) ≥100nS

$t_{CSTB}$ (Clock-Strobe Time) ≥1μ s $t_{TTZ}$(Fall Time)≤10μ s



$t_{TZH}$(Rise Time) ≤1μ s $t_{PZL}$(Propagation Delay Time) ≤100nS

$f_{oSG}$=OSGillation Frequency $t_{PLZ}$(Propagation Delay Time) ≤300uS

$t_{TZL}$< 1μ s $t_{TLZ}$<10μ s

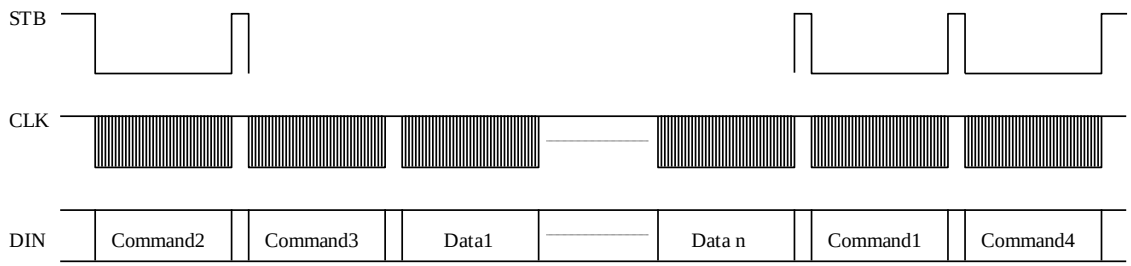
Note: Test condition under

$t_{THZ}$ ( Pull low risistor=100k ohms, Loading capacitor =300pf)

$t_{TLZ}$ (Pull high risistor =100k ohms, Loading capacitor=300pf )

## APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.




where: Command 1: Display Mode Setting Command

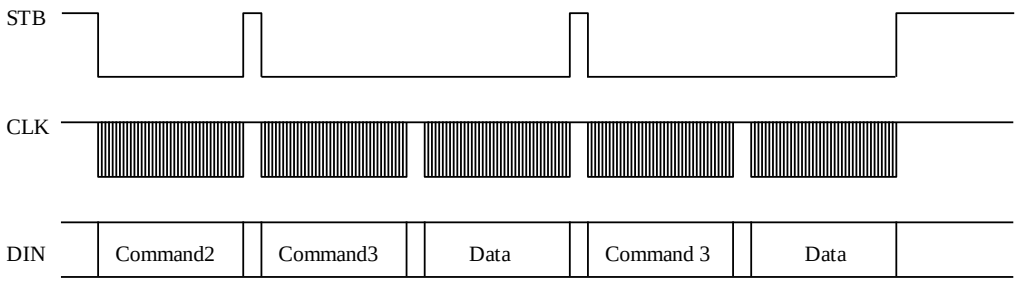
Command 2: Data Setting Command

Command 3: Address Setting Command

Data 1 to n : Transfer Display Data (14 Bytes max.)

Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.

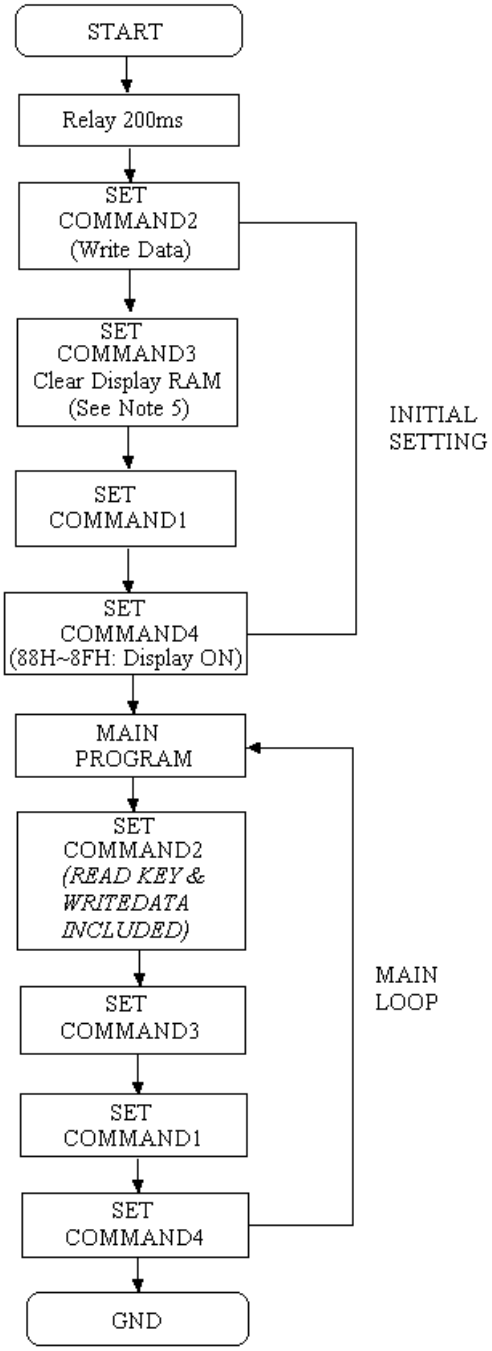



where: Command 2 — Data Setting Command

Command 3 — Address Setting Command

Data — Display Data

# RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART




Note: 1. Command 1: Display Mode Commands

2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

# ABSOLUTE MAXIMUM RATINGS



(Unless otherwise stated, Ta=25℃, GND=0V)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +7 | Volts |
| Logic Input Voltage | $V_I$ | -0.5 to $V_{DD}$ +0.5 | Volts |
| Driver Output Current | $I_{OLGR}$ | +250 | mA |
| | $I_{OHSG}$ | -50 | mA |
| Maximum Driver Output Current/Total | $I_{TOTAL}$ | 400 | mA |

# RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-20 to +70℃, GND=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V |
| Dynamic Current (see Note) | $I_{DDdyn}$ | - | - | 10 | mA |
| High-Level Input Voltage | $V_{IH}$ | $0.8V_{DD}$ | - | $V_{DD}$ | V |
| Low-Level Input Voltage | $V_{IL}$ | 0 | - | $0.3V_{DD}$ | V |

*Note: Test Condition: Set Display Control Commands = 80H (Display Turn OFF State & under no load)*

# ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, $V_{DD}$=5V, GND=0V, Ta=25℃)

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High-Level Output Current | IOHSG1 | Vo=VDD-2V<br>SG1 to SG11, SG12/GR7 | -20 | -25 | -40 | mA |
| | IOHSG2 | Vo=VDD-3V<br>SG1 to SG12, SG12/GR7 | -25 | -30 | -50 | mA |
| Low-Level Output Current | IOLGR | Vo=0.3V<br>GR1 to GR6, SG12/GR7 | 100 | 140 | - | mA |
| Low-Level Output Current | IOLDOUT | Vo=0.4V | 4 | - | - | mA |
| Segment High-Level Output Current Tolerance | ITOLSG | Vo=VDD-3V<br>SG1 to SG11, SG12/GR7 | - | - | ±5 | mA |
| High-Level Input Voltage | VIH | - | 0.8 $V_{DD}$ | - | 5 | V |
| Low-Level Input Voltage | VIL | - | 0 | - | $0.3V_{DD}$ | V |
| OSGillation Frequency | foSG | R=33 KOhms | 350 | 500 | 650 | KHz |
| K1 to K3 Pull Down Resistor | RKN | K1 to K3<br>VDD=5V | 40 | - | 100 | KOhms |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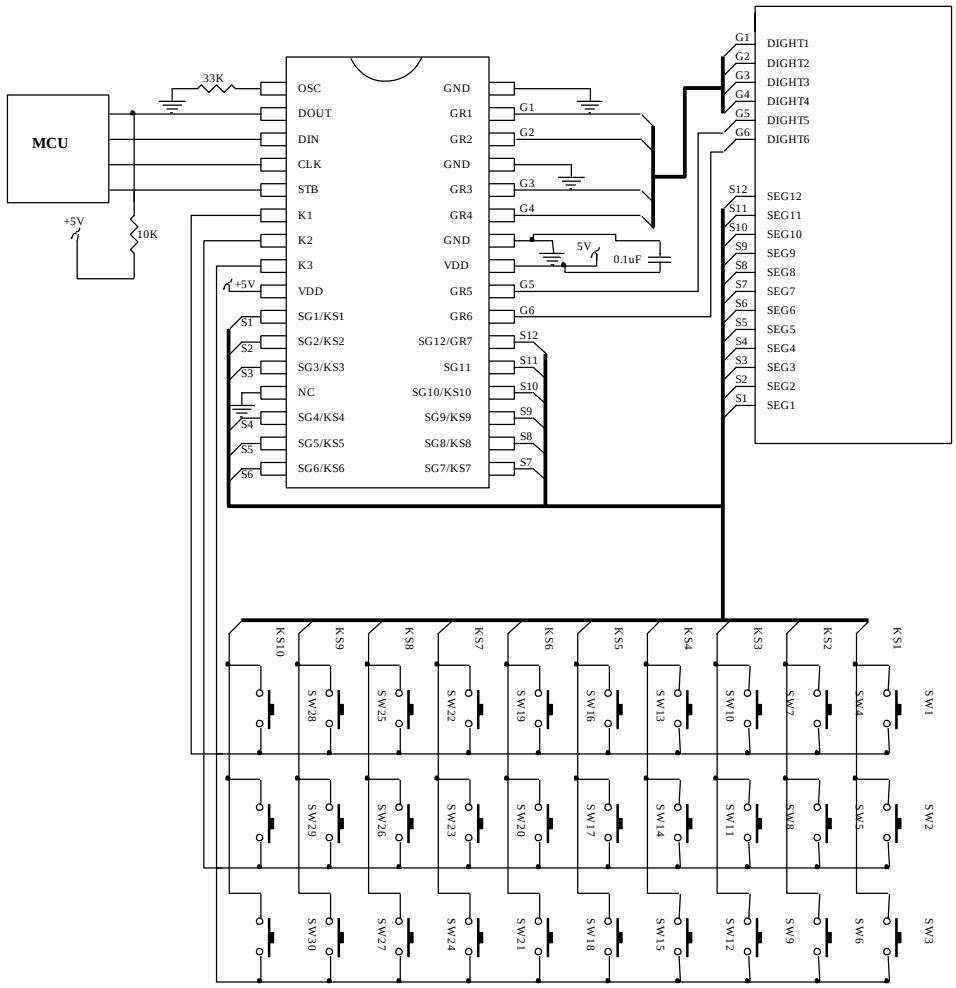
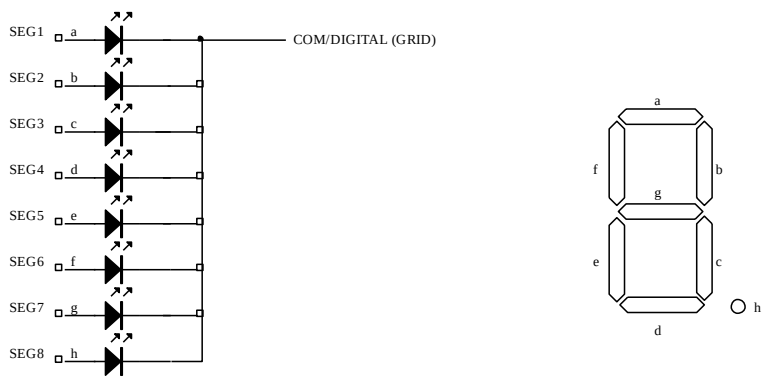
# APPLICATION CIRCUIT



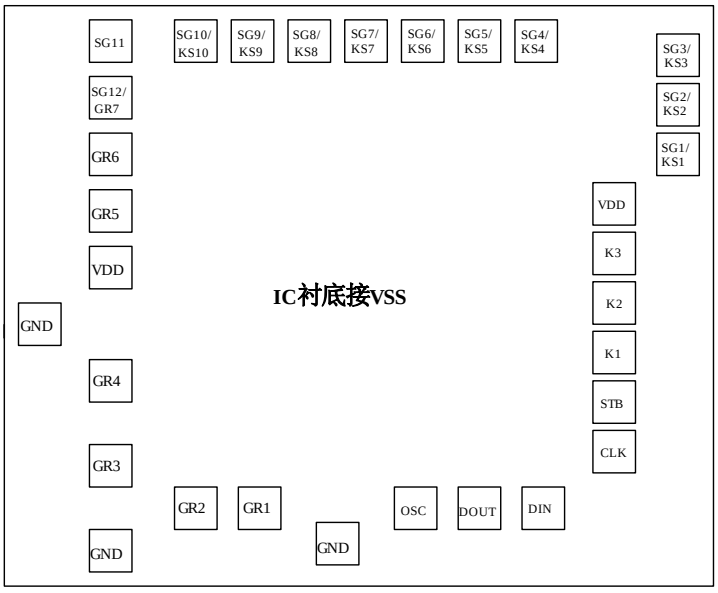

COMMON CATHODE TYPE LED PANEL:




Note: 1、The capacitor (0.1uF) connected between the GND and the VDD pins must be located as close as possible to the DL8836 chip.

2、It is strongly suggested that the NC Pin(pins 13) be connected to the GND.

3、The DL8836 power supply is separate from the application system power supply.


SG11
SG10/ KS10
SG9/ KS9
SG8/ KS8
SG7/ KS7
SG6/ KS6
SG5/ KS5
SG4/ KS4
SG3/ KS3
SG2/ KS2
SG1/ KS1
SG12/ GR7
GR6
GR5
VDD
GND
IC衬底接VSS
VDD
K3
K2
K1
STB
CLK
GR4
GR3
GR2
GR1
GND
OSC
DOUT
DIN
GND