

# VF230C

## XO Low Jitter 3.3V

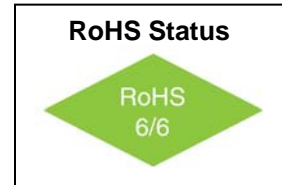
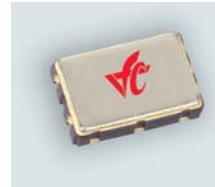
### 5x7mm SMD, LVPECL / LVDS

### 750KHz to 800MHz



#### Features

- 750KHz to 800MHz Frequency Range
- <5ps jitter over 12KHz – 20MHz
- Tristate



#### Applications

- Optical Networking, SONET / SDH
- Gigabit Ethernet
- Fibre channel
- DSL
- Extended temperature applications

#### Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		0.75		800	MHz	
Frequency Stability	$\Delta F/F$	Vs. Operating Temperature			$\pm 100$ $\pm 50$ $\pm 25$ $\pm 20$	ppm	See "How to Order" chart
		Vs. Supply Voltage Vs. Aging / Year		$\pm 3$ $\pm 3$ $\pm 1$		ppm/V ppm ppm/y	First Year After first year
Operating Temperature	T		-55 -55		+85 +125	°C	Order Code A Order Code B
Output		LVPECL LVDS					See "How to Order" chart
Supply Voltage	Vcc		3.15	3.3	3.45	V	
Period Jitter RMS		19.44MHz 77.76 MHz 155.52 MHz 622.08 MHz		5 8 9 10		ps	
Integrated Jitter RMS 12KHz to 20MHz		@155.52MHz		3	5	ps	



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**Electrical Specifications**

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Symmetry		$(V_{DD}-1.3) V_{DC}$ $1.25V_{DC}$			45/55	%	PECL LVDS
Phase Noise		10Hz		-60		dBc/Hz	@19.44MHz
		100Hz		-90			
		1KHz		-112			
		10KHz		-140			
		100KHz		-140			
		10Hz		-60		dBc/Hz	@106.25MHz
		100Hz		-90			
		1KHz		-112			
		10KHz		-127			
		100KHz		-125			
		10Hz		-60		dBc/Hz	@155.52MHz
		100Hz		-90			
		1KHz		-112			
		10KHz		-125			
		100KHz		-123			
		10Hz		-60		dBc/Hz	@622.08MHz
		100Hz		-90			
		1KHz		-109			
		10KHz		-110			
		100KHz		-109			
Input Current	I <sub>CC</sub>	0.75 – 24MHz			25	mA	PECL
		24 – 160MHz			65		
		160 – 800MHz			100		
		0.75 – 24MHz			25	mA	LVDS
		24 – 96MHz			45		
		96 – 800MHz			80		
Load	50 Ohm to $V_{DD}-2V$ (PECL) 100 Ohm (LVDS)						
Output High Voltage	V <sub>OH</sub>			$V_{DD}-1.025$ 1.4	1.6	V	PECL LVDS
Output Low Voltage	V <sub>OL</sub>		0.9	1.1	$V_{DD}-1.620$	V	PECL LVDS
Output Differential Voltage	V <sub>OD</sub>		247	355	454	mV	LVDS
Offset Voltage	V <sub>OS</sub>		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	Tr/Tf	20% to 80%		0.3	0.35	ns	PECL LVDS
				0.3	0.4		
Tristate	"1": On – Pin 1 may float or 2.8V min "0": Tristate – Pin 1 requires 0.4V max						



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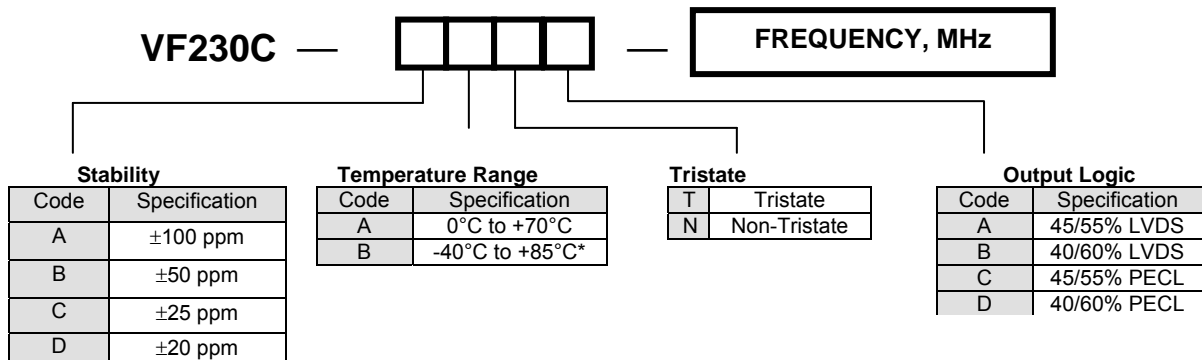
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### Testing

<b>Stabilization Bake</b>	MIL-STD-883 Method 1008, Cond. B
<b>Temperature Cycling</b>	MIL-STD-883 Method 1010, Cond. B
<b>Constant Acceleration</b>	MIL-STD-883, Method 2001, Cond. A
<b>Burn-in</b>	MIL-STD-883 Method 1015, Cond. B (125°C for 168 hours with bias)
<b>Fine Leak</b>	MIL-STD-883, Method 1014, Cond. A1
<b>Gross Leak</b>	MIL-STD-883, Method 1014, Cond. C

### How to Order



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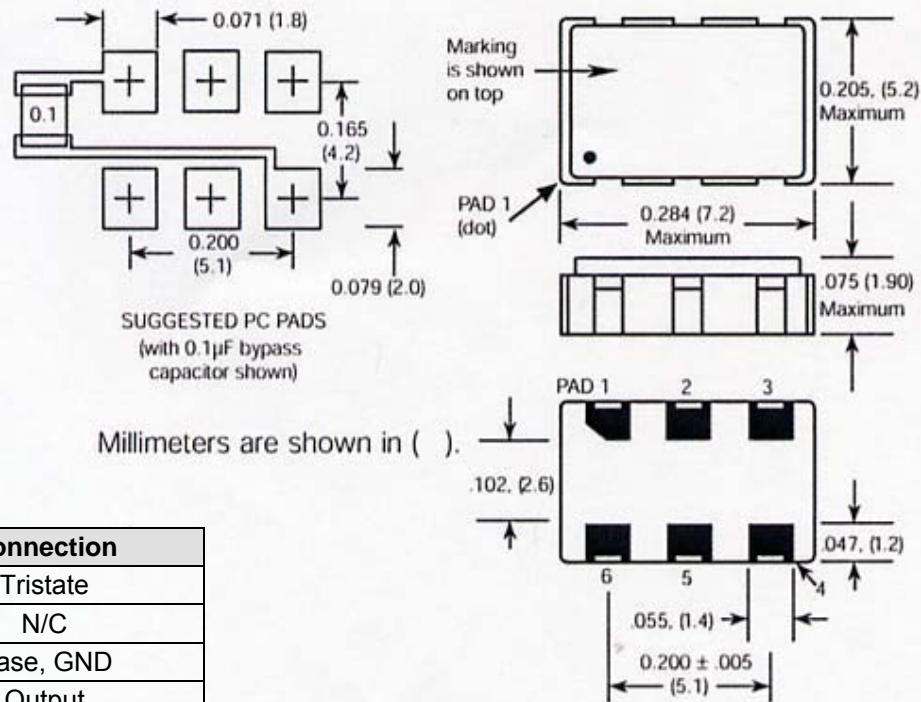
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#### Environmental and Mechanical Conditions

Parameter	Specification
<b>Shock</b>	MIL-STD 883, Method 2002, Cond. B (1500 peak g, 0.5 ms duration, ½ sine wave, 5 shocks in 6 planes)
<b>Humidity</b>	Resistant to 85° R.H. at 85°C
<b>Vibration</b>	MIL-STD 883, Method 2007, Cond. A (20-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less)
<b>Leak</b>	MIL STD 883, Method 1014, Cond. A1 and C1
<b>Case</b>	Hermetically sealed ceramic LCC
<b>Pads</b>	60 microinch of gold over nickel
<b>Marking</b>	Epoxy ink or laser engraved
<b>Resistance to solvents</b>	MIL STD 202, Method 215



Outline Drawing

Pin #	Connection
1	Tristate
2	N/C
3	Case, GND
4	Output
5	Output
6	Supply Voltage

