Features

- Capacitive solid-state device
- 256 × 300 sensor array, 50 µm pitch
- 1.28 cm x 0.1.50 cm (0.5” x 0.6”) sensor area
- 500-dpi resolution
- 3.3V to 5V operating range
- Exceptionally hard protective coating
- Integrated 8-bit analog-to-digital converter
- One of three bus interfaces:
  - 8-bit microprocessor bus interface
  - Integrated USB Full-Speed Interface
  - Integrated Serial Peripheral Interface
- Standard CMOS technology
- Low power, less than 200 mW operating
- Automatic finger detection

Applications

- Secure access for databases, networks, local storage
- Portable fingerprint acquisition
- Smart cards
- Identity verification for ATM transactions
- Cellular phone-based security access
- Access control and monitoring (home, auto, office, etc.)

Overview

The Veridicom FPS200 Solid-State Fingerprint Sensor is a direct contact, fingerprint acquisition device. It is a high performance, low power, low cost, capacitive sensor composed of a two-dimensional array of metal electrodes in the sensing array. Each metal electrode acts as one plate of a capacitor and the contacting finger acts as the second plate. A passivation layer on the device surface forms the dielectric between these two plates. Ridges and valleys on the finger yield varying capacitor values across the array, and the resulting varying discharge voltages are read to form an image of the fingerprint.

The FPS200 is manufactured in standard CMOS technology. The 256 × 300 sensor array has a 50 µm pitch and yields a 500-dpi image. The sensor surface is protected by a patented, ultra-hard, abrasion and chemical resistant coating.

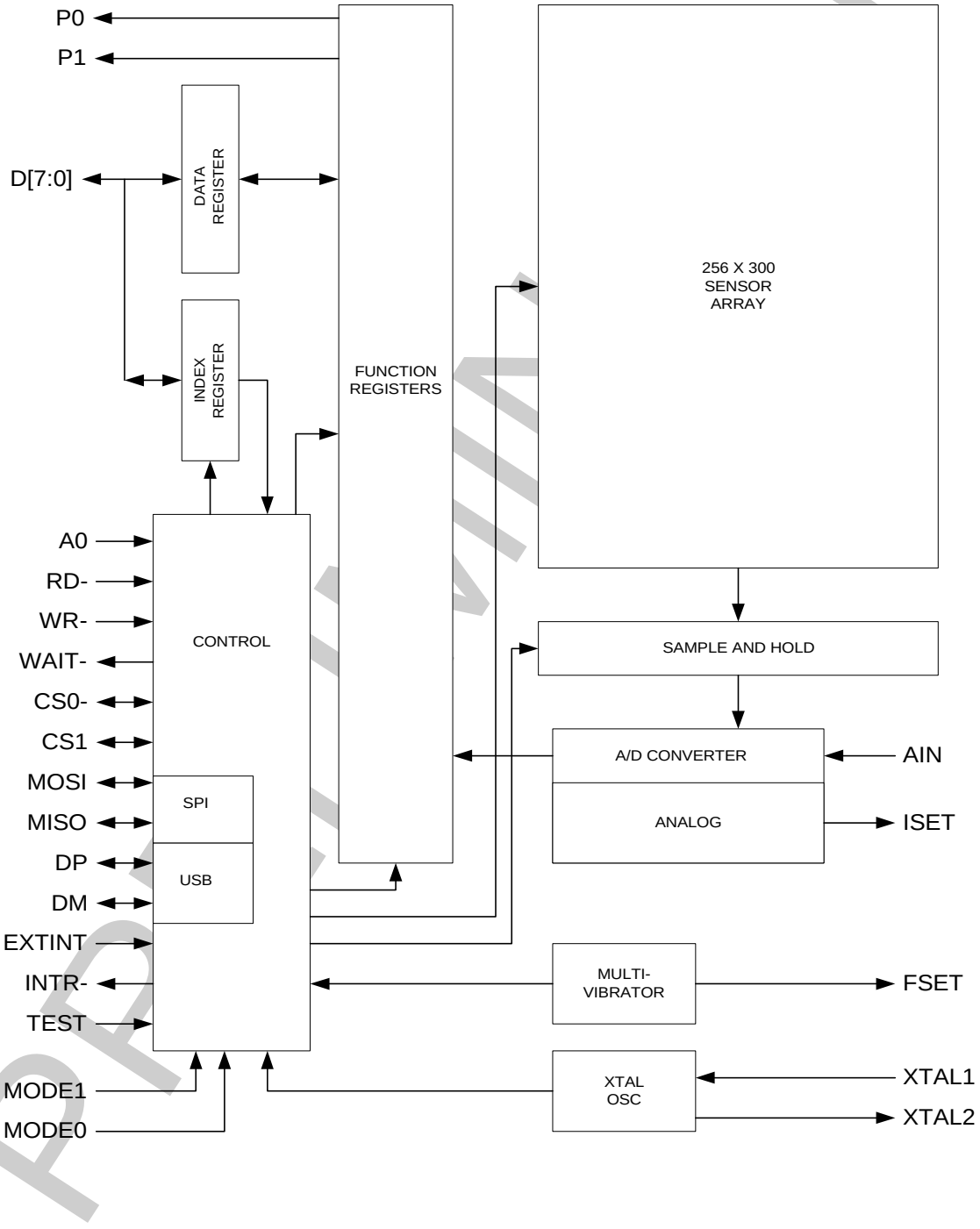
Chip Operation

The sensor array includes 256 columns and 300 rows of sensor plates. Associated with each column are two sample-and-hold circuits. A fingerprint image is sensed or captured one row at a time. This “row capture” occurs in two phases. In the first phase, the sensor plates of the selected row are pre-charged to the VDD voltage. During this pre-charge period, an internal signal enables the first set of sample-and-hold circuits to store the pre-charged plate voltages of the row.

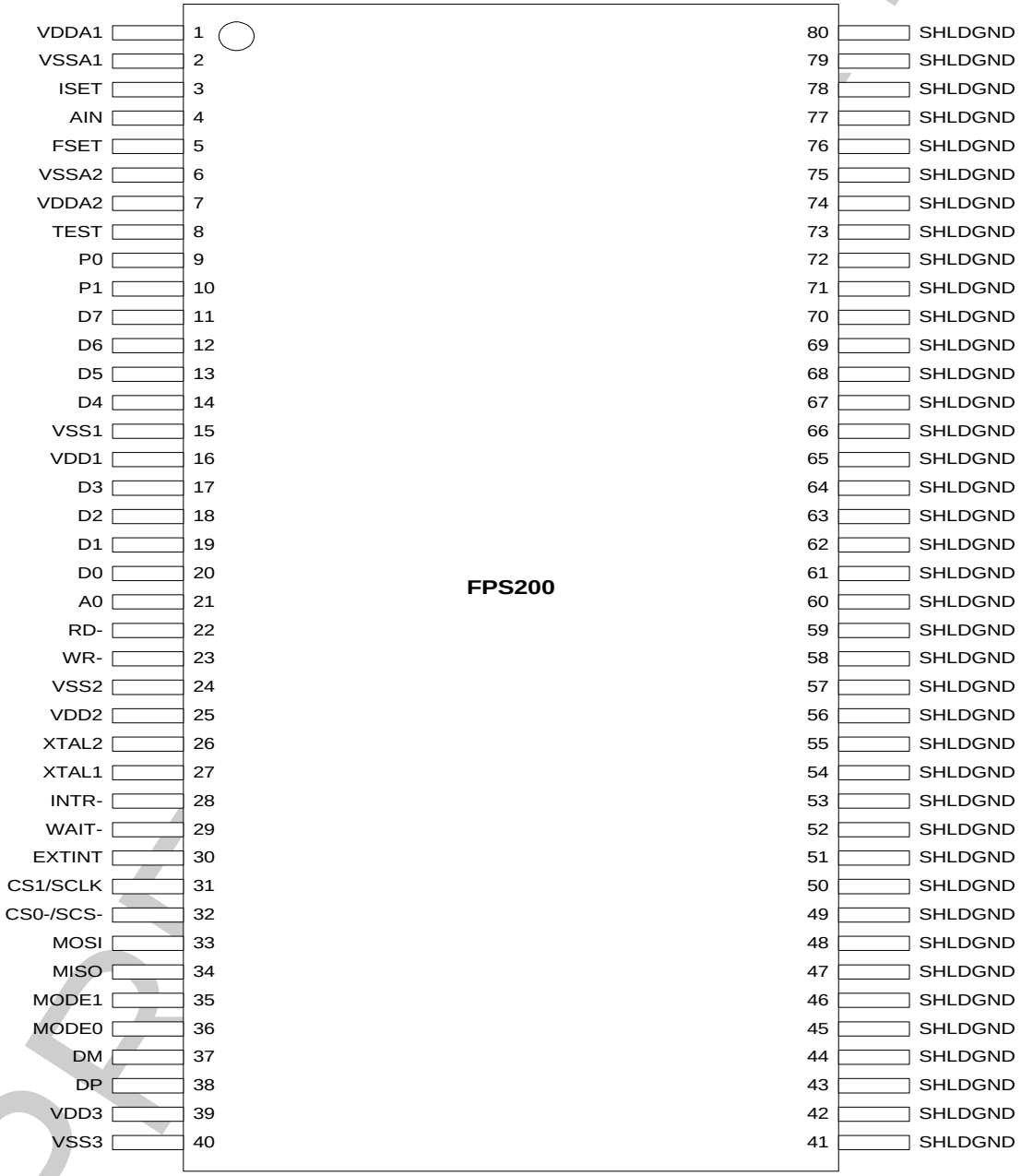
In the second phase, the row of sensor plates is discharged with a current source. The rate at which a cell is discharged is proportional to the “discharge current.” After a period of time (referred to as the “discharge time”), an internal signal enables the second set of sample-and-hold circuits to store the final plate voltages. The difference between the pre-charged and discharged plate voltages is a measure of the capacitance of a sensor cell. After the row capture, the cells within the row are ready to be digitized.

The sensitivity of the chip is adjusted by changing the discharge current and discharge time. The nominal value of the current source is controlled by an external resistor connected between the ISET pin and ground. The current source is controlled from the Discharge Current Register (DCR). The discharge time is controlled by the Discharge Time Register (DTR).

Block Diagram



Connection Diagram



Pin List

Pin Number	Name	Type	(5.0 V) IOL	(5.0 V) IOH	Description
1	VDDA1	PWR			Analog Power Supply
2	VSSA1	GND			Analog Ground
3	ISET	O			Sets Reference Current
4	AIN	I			Analog Input
5	FSET	O			Sets Internal Multi-vibrator Frequency
6	VSSA2	GND			Analog Ground
7	VDDA2	PWR			Analog Power Supply
8	TEST	I			Test Mode Enable
9	P0	O	8 mA	4 mA	Output Port 0
10	P1	O	8 mA	4 mA	Output Port 1
11	D7	I/O	8 mA	4 mA	Data Bit 7
12	D6	I/O	8 mA	4 mA	Data Bit 6
13	D5	I/O	8 mA	4 mA	Data Bit 5
14	D4	I/O	8 mA		Data Bit 4
15	VSS1	GND			Digital Ground
16	VDD1	PWR			Digital Power Supply
17	D3	I/O	8 mA	4 mA	Data Bit 3
18	D2	I/O	8 mA	4 mA	Data Bit 2
19	D1	I/O	8 mA	4 mA	Data Bit 1
20	D0	I/O	8 mA	4 mA	Data Bit 0
21	A0	I			Address Input
22	RD-	I	8 mA	4 mA	Read Enable, Active Low
23	WR-	I	8 mA	4 mA	Write Enable , Active Low
24	VSS2	GND			Digital Ground
25	VDD2	PWR			Digital Power Supply
26	XTAL2	O			Internal Oscillator Output
27	XTAL1	I			Internal Oscillator Input
28	INTR-	O	8 mA		Interrupt Output, Active Low
29	WAIT-	O	8 mA		Wait, Active Low
30	EXTINT	I			External Interrupt Input
31	CS1/SCLK	I/O			Chip Select, Active High
32	CS0-/SCS-	I/O			Chip Select, Active Low
33	MOSI	I/O	8 mA	4 mA	SPI Master Output / Slave Input
34	MISO	I/O	8 mA	4 mA	SPI Master Input / Slave Output
35	MODE1	I			Mode Select 1
36	MODE0	I			Mode Select 0
37	DM	I/O			USB D-
38	DP	I/O			USB D+
39	VDD3	PWR			Digital Power Supply
40	VSS3	GND			Digital Ground
[41:80]	SHLDGND				Shield Ground

Pin Descriptions

VDDA1, VDDA2 (Pins 1 and 7)

Power Supply to the analog section of the sensor. VDDA1 powers the array, row drivers, column receivers, A/D converter, and sample/hold amplifier. VDDA2 powers the multi-vibrator and bias circuits.

VSSA1, VSSA2 (Pins 2 and 6)

Ground for the analog section of the sensor. VSSA1 is the ground return for the array, row drivers, column receivers, A/D converter, and sample hold amplifier. VSSA2 is the ground return for the multi-vibrator and bias circuits.

VDD1, VDD2, VDD3 (Pins 25, 16, and 39)

Power supply to the digital logic and I/O drivers. VDD2 powers the core digital logic, oscillators, phase-locked loops, and digital inputs. VDD1 and VDD3 supply power to the digital output circuits and USB transceivers.

VSS1, VSS2, VSS3 (Pins 24, 15, and 40)

Ground for the digital logic and I/O drivers.

VSS2 is the ground connection for the core digital logic, oscillators, phase-locked loops, and digital inputs. VSS1 and VSS3 are the ground connections for the digital outputs and USB transceivers.

ISET (Pin 3)

Connect a 470k ohm resistor between ISET and analog ground VSSA1 to set the internal reference current. The discharge current is a scalar function of the internal reference current.

AIN (Pin 4)

Alternate analog input to the A/D converter. Set the AINSEL bit in register CTRLA to select AIN as the input to the A/D converter.

FSET (Pin 5)

Connect a resistor between FSET and ground to set the internal multi-vibrator and automatic finger detection frequency. Use a 100K ohm resistor for standard 12 MHz (±20%) multi-vibrator operation and 120KHz (±20%) automatic finger detection sampling rate.

XTAL1 (Pin 27)

Input to the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, connect its output to this pin.

XTAL2 (Pin 26)

Output from the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, leave this pin unconnected.

D[7:0] (Pins 11-14, 17-20)

Bi-directional data bus.

A0 (Pin 21)

Address input. Drive A0 low to select the address index register. Drive A0 high to select the data buffer.

RD- (Pin 22)

Read enable, active low. To read from the chip, drive RD- low while WR- is high and the chip is selected.

WR- (Pin 23)

Write enable, active low. To write to the chip, drive WR- low while RD- is high and the chip is selected.

CS0-/SCS- (Pin 32)

Chip select, active low. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)

CS0-/SCS- functions as an active-low chip select input. Drive CS0-/CSC- low while CS1 is high to select the chip.

MODE[1:0] = 01b (SPI Slave Mode)

CS0-/SCS- functions as an active-low slave chip select input. Connect a pull-up resistor between CS0-/SCS- and VDD.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)

CS0-/SCS- has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)

CS0-/SCS- functions as the master chip select output, active low to the slave serial ROM chip select. Connect a pull-up resistor between CS0-/CSC- and VDD.

CS1/SCLK (Pin 31)

Chip select, active high. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)

CS1/SCLK functions as an active-high chip select input. Drive CS1/SCLK high while CS0-/CSC- is low to select the chip.

MODE[1:0] = 01b (SPI Slave Mode)

CS1/SCLK functions as the slave serial clock input.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)

CS1/SCLK has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)

CS1/SCLK functions as the master serial clock output to the slave serial ROM clock input. Connect a pull-up resistor between CS1/SCLK and VDD.

EXTINT (Pin 30)

External Interrupt input. This pin can be programmed to be edge or level sensitive, active-high or active-low.

INTR- (Pin 28)

Interrupt output, active low. INTR- is high impedance when it is not active and is driven low when an enabled interrupt event occurs.

WAIT- (Pin 29)

Wait output, active low. WAIT- is driven low when active and high-impedance when not active. WAIT- goes low if the A/D converter is read while an A/D conversion is in progress. WAIT- will remain low until the A/D conversion is completed.

MOSI (Pin 33)

SPI Master Output/Slave input. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)

MOSI has no function.

MODE[1:0] = 01b (SPI Slave Mode)

MOSI functions as the slave serial input.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)

MOSI has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)

MOSI functions as the master serial data output to the slave serial ROM data input. Unlike standard SPI, MOSI is actively driven high and low when transmitting data and is high impedance when idle. Connect a pull-up resistor between MOSI and VDD to pull MOSI high when idle.

MISO (Pin 34)

SPI Master Input/Slave Output. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[0:1] = 00b (Microprocessor Bus Interface Mode)

MISO has no function.

MODE[1:0] = 01b (SPI Slave Mode)

MISO functions as the slave serial data output. Unlike standard SPI, the MISO connection is actively driven high and low when transmitting data and is high impedance when idle. Connect a pull-up resistor between MISO and VDD to pull MISO high when idle.

MODE1/MODE0 = 10b (USB Interface Mode, Using Internal ROM)

MISO has no function.

MODE1/MODE0 = 11b (USB Interface Mode, Using External ROM)

MISO functions as the master serial data input from the slave serial ROM data output.

P0 (Pin 9)

Port Output 0. This output is controlled by bit 0 of the CTRLC register.

P1 (Pin 10)

Port Output 1. This output is controlled by bit 1 of the CTRLC register.

DP (Pin 38)

USB D+ data line. In USB mode, connect a 1.5k ohm resistor between DP and VDD3, which must be 3.3V in this mode.

DM (Pin 37)

USB D- data line.

MODE[1:0] (Pins 35 and 36)

Mode Select pins. MODE[1:0] select one of four operating modes.

MODE[1:0]	Description
00b	Microprocessor Bus Mode
01b	SPI Bus Mode
10b	USB Mode, Using Internal ROM
11b	USB Mode, Using External ROM

TEST (Pin 8)

Test Mode Enable. It is intended for factory use only. Connect this pin to VSS.

SHLDGND (Pins 41–80)

Shield Ground. These pins connect to the metal ring on the top of the package. Connect these pins to ground and/or shield ground.

Device Bus Operation

Microprocessor Bus Interface

The microprocessor bus interface mode uses the following pins: D[7:0], A0, RD-, WR-, CS0-, CS1, EXTINT, INTR-, and WAIT-. Either the internal multi-vibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The SPI and USB interfaces are disabled.

The fingerprint sensor chip uses an indexed addressing scheme to access its function registers. The chip has 8 data lines (D[7:0]) and one address line (A0). The address line selects between the index register and the data register. Drive A0 low to select the index register. Drive A0 high to access the function register selected by the index register. The index register retains its value until it is rewritten or the chip is reset.

The chip has four control inputs: CS0-, CS1, RD-, and WR-. Drive CS0- low and CS1 high to select the chip. Data is latched on the rising edge of WR-.

The chip has two status lines: INTR- and WAIT-. The INTR- signal is asserted when an interrupt event occurs. The WAIT- signal goes low when the A/D converter is read while an A/D conversion is in progress. The WAIT- signal will be high impedance when the A/D conversion is completed. Both the WAIT- and INTR- outputs are high impedance when they are not active. As a result, they can be active-low WIRE-ORed in conjunction with other interrupts or wait signals.

The SPI and USB interfaces are disabled when the microprocessor bus interface is selected. A truth table for the microprocessor bus interface is shown below:

Truth Table for the Microprocessor Bus Interface

CS0-	CS1	A0	RD-	WR-	Mode	Data Lines
H	X	X	X	X	De-selected	High Impedance
X	L	X	X	X	De-selected	High Impedance
L	H	X	H	H	Standby	High Impedance
L	H	L	L	H	Read Index Register	Output
L	H	L	H	L	Write Index Register	Input
L	H	H	L	H	Read Data Register	Output
L	H	H	H	L	Write Data Register	Input

Serial Peripheral Interface (SPI) Slave

SPI Bus Mode

SPI (Slave) bus mode uses the following pins: SCLK, SCS-, MOSI, MISO, and EXTINT. Either the internal multi-vibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The microprocessor bus and USB interface are disabled.

SPI Slave Mode

In SPI Slave Mode, the sensor can operate in either SPI mode (0, 0) where CPOL = 0 and CPHA = 0 or SPI mode (1, 1) where CPOL = 1 and CPHA = 1. The SPI Master may clock in commands and clock out data up to 12 Mbits per second. The SPI Master can write and read the registers of the sensor even when the internal 12 MHz multi-vibrator or XTAL1/XTAL2 oscillator is halted.

- MOSI bits are sampled on the rising edge of SCK
- MISO bits change on the falling edge of SCK
- SCK can be idle in either a high or low state
- The most significant bits are shifted out first

Register Read Command in SPI Slave Mode

The Register Read command includes a command byte and address byte. The command sequence begins when the SPI master drives SCS- low and sends the Read Command byte (encoded as 0x03) on the MOSI pin. Following the command byte, the master sends the address byte, which is the index to the register to be read. After receiving the least significant bit (LSB) of the address byte, the SPI slave sensor sends the contents of the selected register on the MISO pin. Finally, the master drives SCS- high after it has sampled the LSB of the data byte. However, when reading the A/D converter, the master may keep SCS- low to read consecutive pixels; the SPI slave sensor will automatically increment to the address of the next pixel. The SPI Master must drive SCS- high before beginning another command.

Register Write Command for SPI Slave Mode

The Register Write command includes a command byte and address byte followed by the data to be written. The command sequence begins when the SPI Master drives SCS- low and sends the Write Command byte (encoded as 0x02) on the MOSI pin. Then the master sends the address byte, which is the index to the register to be written. Finally, the master sends the data byte and thereafter drives SCS- high.

USB Interface Mode, Using Internal ROM

This USB mode uses the following pins: DP, DM, EXTINT, XTAL1, and XTAL2. XTAL1 must be driven from a 12 MHz source or a 12 MHz crystal circuit must be connected to XTAL1 and XTAL2. The internal 12 MHz multi-vibrator, the microprocessor bus, and SPI interface are disabled.

The internal USB descriptor ROM will be accessed in response to a USB GET_DESCRIPTOR command.

USB Interface Mode, Using External ROM

This USB mode the uses following pins: DP, DM, SCLK, SCS-, MOSI, MISO, EXTINT, XTAL1, and XTAL2. XTAL1 must be driven from a 12 MHz source or a 12 MHz crystal circuit must be connected to XTAL1 and XTAL2. The internal 12 MHz multi-vibrator and the microprocessor bus are disabled.

The SPI interface is enabled as an SPI Master. The external SPI serial ROM will be accessed in response to a USB GET_DESCRIPTOR command. The internal USB descriptor ROM is disabled. This mode allows an external serial ROM to override the internal descriptor ROM.

Note: When the FPS200 is directly connected to USB in either of the modes above, the VDD and VDDA pins must be powered between 3.3V and 3.6V so that the FPS200 DP and DM pins do not drive the USB beyond 3.6V.

SPI Master Mode

In SPI Master Mode the sensor operates in SPI mode (1,1) where CPOL = 1, and CPHA = 1. SCK is limited to 1 MHz.

- MOSI bits change on the falling edge of SCK
- MISO bits are sampled on the rising edge of SCK
- SCK is idle in the high state
- The most significant bits are shifted out first

Function Register Descriptions

The function registers are accessed by indexed addressing. Write the index register to select a function register. Read or write the data register to access the contents of the function register. All registers can be read and written except as noted in the following descriptions.

Function Register Map

Index	Name	Description	Read/Write Access
0x00	RAH	Row Address, High	R/W
0x01	RAL	Row Address, Low	R/W
0x02	CAL	Column Address, Low	R/W
0x03	REH	Row Address End, High	R/W
0x04	REL	Row Address End, Low	R/W
0x05	CEL	Column Address End, Low	R/W
0x06	DTR	Discharge Time Register	R/W
0x07	DCR	Discharge Current Register	R/W
0x08	CTRLA	Control Register A	R/W
0x09	CTRLB	Control Register B	R/W
0x0A	CTRLC	Control Register C	R/W
0x0B	SRA	Status Register A	R
0x0C	PGC	Programmable Gain Control Register	R/W
0x0D	ICR	Interrupt Control Register	R/W
0x0E	ISR	Interrupt Status Register	R/W
0x0F	THR	Threshold Register	R/W
0x10	CIDH	Chip Identification, High	R
0x11	CIDL	Chip Identification, Low	R
0x12	TST	Test Mode Register	R/W

Note: In the following descriptions, "sub-image" means a rectangular region of the sensor array, up to and including the entire array.

RAH 0x00

Row Address Register High.
Reset State: 0x00

This register holds the high order bit of the address of the first row of a sub-image.

Bit Number	Bit Name	Function
[7:1]	-	Reserved. Write 0 to these bits.
0	RA[8]	Most Significant Bit of Row Address Register

RAL 0x01

Row Address Register Low.
Reset State: 0x00

This register holds the low order byte of the address of the first row of a sub-image.

Bit Number	Bit Name	Function
[7:0]	RA[7:0]	Low eight bits of Row Address Register

CAL 0x02

Column Address Register.
Reset State: 0x00

This register holds the address of the first column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CA[7:0]	Column Address Register

REH 0x03

Row Address End Register High.
Reset State: 0x00

This register holds the most significant bit of the address of the last row of a sub-image.

Bit Number	Bit Name	Function
[7:1]	-	Reserved. Write 0 to these bits.
0	REND[8]	Most Significant Bit of Row Address Register

REL 0x04

Row Address End Register Low.
Reset State: 0x00

This register holds the least significant byte of the address of the last row of a sub-image.

Bit Number	Bit Name	Function
[7:0]	REND[7:0]	Low eight bits of Row Address Register

CEL 0x05

Column Address End Register.
Reset State: 0x00

This register holds the address of the last column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CEND[7:0]	Column Address Register

DTR 0x06

Discharge Time Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7]	-	Reserved. Write 0 to these bits.
[6:0]	DT[6:0]	Sets the discharge time in oscillator clock periods.

DCR 0x07

Discharge Current Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	-	Reserved. Write 0 to these bits.
[4:0]	DC[4:0]	Sets the discharge current rate.

CTRLA 0x08

Control Register A.
Reset State: 0x00

Write this register to initiate image conversion. Read this register to read the A/D converter.

The GETSUB, GETIMG, and GETROW bits select an image access mode and initiate an A/D conversion sequence. The AINSEL bit selects the input source to the A/D converter.

Set the GETSUB bit to initiate the capture of a rectangular sub-image defined by the RAH, RAL, CAL, REH, REL, and CEL registers. In CPU or SPI mode, the sub-image can be an arbitrary rectangle ranging from a single pixel to the entire array. In USB mode, the number of columns in the sub-image must be an integral multiple of 64.

Set the GETIMG bit to initiate the capture of a whole image starting from row zero and column zero through row 299 and column 255, regardless of the RAH, RAL, CAL, REH, REL, and CEL registers.

Set the GETROW bit to initiate the capture of a row specified by the RAH and RAL registers.

Writing a 1 to any of GETSUB, GETIMG, or GETROW abandons the current image access operation and restarts at the beginning of the sub-image, image, or row. Set at most one of these three bits. If more than one these three bits are set, image conversion will not start.

Set the AINSEL bit along with one of the other three bits to begin the analog to digital conversion of the voltage on the AIN pin instead of the sensor array.

Writing 0 to the CTRLA register has no effect other than clearing AINSEL; the current image access operation is not abandoned.

Bit Number	Bit Name	Function
7	-	Reserved. Write 0 to this bit.
6	-	Reserved. Write 0 to this bit.
5	-	Reserved. Write 0 to this bit.
4	-	Reserved. Write 0 to this bit.
3	AINSEL	0=Select Array for Conversion 1=Select External Analog Input Pin and start Conversion
2	GETSUB	Initiates Auto-increment for sub-image
1	GETIMG	Initiates Auto-increment for whole image
0	GETROW	Initiates Auto-increment for selected row

Parameter Description	Min	Max	Units
Rising Edge of WR- to First Data Valid	155 + n	156 + n	Clock Cycles
Rising Edge of RD- to Next Data Valid	6	7	Clock Cycles

CTRLB 0x09

Control Register B.
Reset State: CTRLB[7:6] = state of MODE[1:0].
CTRLB[5] = 1.
CTRLB [4:0] = 0x00, Chip is disabled, oscillator is stopped.

Bit Number	Bit Name	Function
[7:6]	MODE[1:0]	Reflects the state of the MODE[1:0] pins. These bits are read-only. Writing to these bits has no effect. Write 0 to these bits.
5	RDY	This is a read-only bit that indicates the status of the A/D Converter. 0 = A/D Conversion is in progress. 1 = A/D Converter is idle. Writing this bit has no effect. Write 0 to this bit.
4	-	Reserved. Write 0 to this bit.
3	AFDEN	Set this bit to enable the automatic finger detection circuit. In USB mode, automatic finger detection will generate an interrupt on endpoint 2. In CPU or SPI mode, automatic finger detection will generate a finger detect interrupt on the INTR- pin as controlled by the Interrupt Control Register (ICR). In any mode, the automatic finger detection can be combined with ENABLE=0 to save power.
2	AUTOINCEN	0 = Column and row addresses do not automatically increment after the A/D converter is read. 1 = Column addresses increment and another A/D conversion is initiated after the A/D converter is read. The row address increments at the end of each column.
1	XTALSEL	In USB mode this bit has no function. In CPU and SPI mode this bit selects the clock source for the digital logic. 0 = Selects the internal 12 MHz multi-vibrator. 1 = Selects the XTAL1 pin.
0	ENABLE	0 = Place the sensor array, digital, and analog block into low-power state (12 MHz clock is halted, A/D Converter is shut down). 1= Enable the sensor array, digital, and analog blocks (12 MHz clock and A/D Converter are enabled).

CTRLC 0x0A

Control Register C. This register controls the behavior of general output port pins P0 and P1.
Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	PT1[2:0]	Programs the toggle rate of the P1 pin. If PT1[2:0] = 000, then the P1 pin follows the state of the P1 bit. Otherwise PT1[2:0] selects the number of times the P1 pin toggles per second. 000 = P1 pin follows state of bit P1. 001 = P1 pin toggles 0.75 times per second. 010 = P1 pin toggles 1.5 times per second. 011 = P1 pin toggles 3 times per second. 100 = P1 pin toggles 6 times per second. 101 = Reserved. 110 = Reserved. 111 = Reserved.
[4:2]	PT0[2:0]	Programs the toggle rate of the P0 pin. If PT0[2:0] = 000, then the P0 pin follows the state of the P0 bit. Otherwise PT0[2:0] selects the number of times the P0 pin toggles per second. 000 = P0 pin follows state of bit P0. 001 = P0 pin toggles 0.75 times per second. 010 = P0 pin toggles 1.5 times per second. 011 = P0 pin toggles 3 times per second. 100 = P0 pin toggles 6 times per second. 101 = Reserved. 110 = Reserved. 111 = Reserved.
1	P1	General Purpose Output Port. When PT1[2:0] bits are 000, this bit controls the P1 pin. 0 = P1 pin low. 1 = P1 pin high.
0	P0	General Purpose Output Port. When PT0[2:0] bits are 000, this bit controls the P0 pin. 0 = P0 pin low. 1 = P0 pin high.

SRA 0x0B

Status Register A. Read Only. This register shadows the state of CTRLA.
Reset State: 0x00

Bit Number	Bit Name	Function
7	-	Reserved. Returns 0.
6	-	Reserved. Returns 0.
5	-	Reserved. Returns 0.
4	-	Reserved. Returns 0.
3	AINSEL	This bit is set or cleared when the AINSEL bit (CTRLA bit 3) is set or cleared by software.
2	GETSUB	This bit is set when the GETSUB bit (CTRLA bit 2) is set by software. This bit is cleared after the last byte is read.
1	GETIMG	This bit is set when the GETIMG bit (CTRLA bit 1) is set by software. This bit is cleared after the last byte is read.
0	GETROW	This bit is set when the GETROW bit (CTRLA bit 0) is set by software. This bit is cleared after the last byte is read.

PGC 0x0C

Programmable Gain Control Register.
Reset State: 0x00

Bit Number	Bit Name	Function
[7:4]	-	Reserved. Write 0 to these bits. Returns 0 when read.
[3:0]	PG[3:0]	Sets the gain of the amplifier. 0000 = To BeDetermined (default) 0001 = TBD 0010 = TBD 0011 = TBD 0100 = TBD 0101 = TBD 0110 = TBD 0111 = TBD 1000 = TBD 1001 = TBD 1010 = TBD 1011 = TBD 1100 = TBD 1101 = TBD 1110 = TBD 1111 = TBD

ICR 0x0D

Interrupt Control Register.
Reset State 0x00.

This register controls the behavior of the two interrupt sources of the fingerprint sensor. Interrupt request 0 corresponds to the finger detect interrupt. Interrupt request 1 corresponds to the external interrupt pin EXTINT.

Set bits IE[1:0] to enable the corresponding interrupt. Disabling an interrupt prevents the interrupt event from causing the chip to assert INTR-. However, the interrupt event is not prevented from setting its corresponding bit in the ISR register.

Set bits IM[1:0] to prevent an interrupt event from setting the corresponding bit in the ISR. Setting or clearing IM[1:0] will not clear ISR bits IR[1:0].

Set bits IT[1:0] to program the interrupts as edge or level sensitive. If IT1 is programmed as edge triggered, then IR1 (interrupt request 1) will be set by the falling edge of EXTINT.

IP[1:0] select the polarity of the interrupt source. To detect finger down and finger up states with the internal finger detect circuit, set the IP0 bit to detect finger down (rising or high signal). After the finger down interrupt occurs, clear the IP0 bit to detect finger up (falling or low signal). Similarly, IP1 can be programmed to select the polarity of the EXTINT signal.

Bit Number	Bit Name	Function
7	IP1	0=EXTINT Interrupt Polarity is Falling Edge or Active Low 1=EXTINT Interrupt Polarity is Rising Edge or Active High
6	IP0	0=Finger Detect Interrupt Polarity is Falling Edge or Active Low 1=Finger Detect Interrupt Polarity is Rising Edge or Active High
5	IT1	0=EXTINT Interrupt is Edge Triggered 1=EXTINT Interrupt is Level Triggered
4	IT0	0=Finger Detect Interrupt is Edge Triggered 1=Finger Detect Interrupt is Level Triggered
3	IM1	0=EXTINT Interrupt Not Masked 1=EXTINT Interrupt Masked
2	IM0	0=Finger Detect Interrupt Not Masked 1=Finger Detect Interrupt Masked
1	IE1	0=EXTINT Interrupt Disabled 1=EXTINT Interrupt Enabled
0	IE0	0=Finger Detect Interrupt Disabled 1=Finger Detect Interrupt Enabled

ISR 0x0E

Interrupt Status Register.
Reset State 0x00.

Read this register to determine source(s) of interrupt(s).
Write a 1 to IR[1:0] to acknowledge and clear the corresponding interrupt bit.

Bits IS[1:0] reflect the state of the finger detect sensor and the EXTINT pin, regardless of the bit settings in the ICR register.

Bit Number	Bit Name	Function
[7:4]	-	Reserved. Write 0 to these bits. Returns 0 when read.
3	IS1	Reflects the state of the EXTINT Pin. Write 0 to this bit.
2	IS0	Reflects the state of the Finger Detect Sensor. Write 0 to this bit.
1	IR1	EXTINT Interrupt Request Pending.
0	IR0	Finger Detect Interrupt Request Pending.

THR 0x0F

Threshold Register.
Reset State 0x00.

This register controls the threshold at which a finger is detected by the automatic finger detection circuit.

Bit Number	Bit Name	Function
[7:6]	-	Reserved. Write 0 to these bits.
[5:4]	THV[1:0]	Threshold voltage level.
[3:0]	THC[3:0]	Sharing capacitor size.

CIDH 0x10

Chip Identification Register High. This register holds the high order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDH[7:0]	Returns 0x20 when read.

CIDL 0x11

Chip Identification Register Low. This register holds the low order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDL[7:0]	Returns 0x0A when read.

TST 0x12

Test Mode Register. Reserved for factory use only.
Reset State 0x00.

Bit Number	Bit Name	Function
[7:0]	TST[7:0]	Reserved. Write only 0 to these bits.

Image Read Procedure

Microprocessor Interface

Get Whole Image

Write CTRLA with bit 1 set (GETIMG). This causes these events to happen:

- Row address resets to zero
- Column address resets to zero
- Row capture automatically starts
- ADC automatically starts

Read CTRLA for the ADC result. The rising edge of RD- at this address causes the next ADC to start. Automatic increment and ADC will stop after the pixel at row 299 column 255 is converted.

Get Sub-Image

Write CTRLA with bit 2 set (GETSUB). This causes the following events to happen:

- Row address loaded with contents of RAH and RAL register
- Column address loaded with contents of CAL
- Row capture automatically starts
- ADC automatically starts

Read CTRLA for the ADC result. The rising edge of RD- at this address causes the next ADC to start. Automatic increment and ADC will stop when the pixel specified by RENDH, RENDL, and CENDL has been converted.

Get Whole Row

Write CTRLA with bit 0 set (GETROW). This causes the following events to happen:

- Row address loaded with contents of RAH and RAL register.
- Column address resets to zero
- Row capture automatically starts
- ADC automatically starts

Read CTRLA for the ADC result. The rising edge of RD- at this address causes the next ADC to start. Automatic increment and ADC will stop after column 255 is converted.

Serial Peripheral Interface

The “Get Image,” “Get Sub-Image,” and “Get Row” functions are initiated by writing the same registers as described in the microprocessor interface, except that the commands are written to the MOSI pin and the data is read back on the MISO pin.

USB Interface

The “Get Image,” “Get Sub-Image,” and “Get Row” functions are initiated by writing the same registers as described in the microprocessor interface, except that the registers are written and read on endpoint 0 and the image data is read from endpoint 1.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
VDD	Power Supply Voltage	TBD	V
VIN, VOUT	Voltage on Any Pin Relative to VSS	TBD	V
IOUT	Output Current per I/O	TBD	mA
TA	Ambient Temperature	TBD	°C
TSTG	Storage Temperature	TBD	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGE

Symbol	Description		Min	Max	Unit
VDD	Supply Voltage		3.3	5.5	V
		USB Mode	3.3	3.6	V
TA	Ambient Temperature		TBD	TBD	°C

DC CHARACTERISTICS

(VDD = 5.0 V)

Symbol	Description	Test Conditions	Min	Max	Units
VIL	Input LOW Voltage		-0.5	0.8	V
VIH	Input HIGH Voltage		2.0	VDD	V
VOL	Output LOW Voltage	VDD = MIN, IOL = 8 mA	-	0.4	V
VOH	Output HIGH Voltage	VDD = MIN, IOH = -4 mA	2.4	-	V
ILI	Input Leakage Current	VDD = MAX, VIN = VSS to VDD	TBD	TBD	µA
ILO	Output Leakage Current	VDD = MAX, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	TBD	TBD	µA

(VDD = 3.3 V)

Symbol	Description	Test Conditions	Min	Max	Units
VIL	Input LOW Voltage		TBD	TBD	V
VIH	Input HIGH Voltage		TBD	TBD	V
VOL	Output LOW Voltage	VDD = 3.6V, IOL = 4 mA	-	TBD	V
VOH	Output HIGH Voltage	VDD = 3.0V, IOH = -2 mA	TBD	-	V
ILI	Input Leakage Current	VDD = 3.6V VIN = VSS to VDD	TBD	TBD	µA
ILO	Output Leakage Current	VDD = 3.6V, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	TBD	TBD	µA

POWER SUPPLY CONSUMPTION

(Microprocessor Mode, VDD = 5.0 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA

(SPI Slave Mode, VDD = 5.0 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA

(Microprocessor Mode, VDD = 3.3 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA

(SPI Slave Mode, VDD = 3.3 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA

(USB Mode, Using Internal ROM, VDD = 3.3 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDSPF	Digital Current, USB Suspend with Auto Finger Detection Enabled		TBD	TBD	µA
IDDSP	Digital Current, USB Suspend		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA
IDDASPF	Digital Current, USB Suspend with Auto Finger Detection Enabled		TBD	TBD	µA
IDDASP	Digital Current, USB Suspend		TBD	TBD	µA

(USB Mode, Using External ROM, VDD = 3.3 V)

Symbol	Description	Test Conditions	Min	Max	Units
IDD	Digital Current, Dynamic		TBD	TBD	mA
IDDSB	Digital Current, Standby		TBD	TBD	mA
IDDPDF	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDPD	Digital Current, Power Down		TBD	TBD	µA
IDDSPF	Digital Current, USB Suspend with Auto Finger Detection Enabled		TBD	TBD	µA
IDDSP	Digital Current, USB Suspend		TBD	TBD	µA
IDDA	Analog Current, Dynamic		TBD	TBD	mA
IDDASB	Analog Current, Standby		TBD	TBD	mA
IDDAPDF	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	TBD	µA
IDDAPD	Analog Current, Power Down		TBD	TBD	µA
IDDASPF	Digital Current, USB Suspend with Auto Finger Detection Enabled		TBD	TBD	µA
IDDASP	Digital Current, USB Suspend		TBD	TBD	µA

AC CHARACTERISTICS

MICROPROCESSOR BUS MODE

READ CYCLE

Symbol	Description		Min	Max	Units
tACC	Address to Output Delay		TBD	TBD	ns
tCE	Chip Select to Output Delay		TBD	TBD	ns
tOE	Read Enable to Output Delay		TBD	TBD	ns
tOH	Output Hold Time from Address, CS0-, CS1, or RD-, which ever occurs first		TBD	TBD	ns
tDF	RD- high to Output High Z		TBD	TBD	ns
tDF	CS0- high or CS1 low to Output High Z		TBD	TBD	ns

WRITE CYCLE

Symbol	Description		Min	Max	Units
tAS	Address Setup to WR- low		TBD	-	ns
tCS	CS0- Setup to WR- low		TBD	-	ns
tCS	CS1 Setup to WR- low		TBD	-	ns
tAH	Address Hold Time from WR- high		TBD	-	ns
tCH	CS0- Hold Time from WR- high		TBD	-	ns
tCH	CS1 Hold Time from WR- high		TBD	-	ns
tWP	WR- Pulse Width Low		TBD	-	ns
tWPH	WR- Pulse Width High		TBD	-	ns
tDS	Data Setup Time to WR- low		TBD	-	ns
tDH	Data Hold Time to WR- high		TBD	-	ns

SPI SLAVE MODE

Symbol	Description		Min	Max	Units
fSCK	SCLK Clock Frequency		TBD	TBD	MHz
tCSS	SCS- Setup Time		TBD	TBD	ns
tCSH	SCS- Hold Time		TBD	TBD	ns
tWL	SCLK Low		TBD	TBD	ns
tWH	SCLK High		TBD	TBD	ns
tCS	SCS- High Time		TBD	TBD	ns
tSU	Data-In Setup Time		TBD	TBD	ns
tH	Data-In Hold Time		TBD	TBD	ns
tV	Data-Out Valid Time		TBD	TBD	ns
tHD	Data-Out Hold Time		TBD	TBD	ns
tDIS	Data-Out Disable Time		TBD	TBD	ns

SPI MASTER

Symbol	Description		Min	Max	Units
fSCKM	SCLK Clock Frequency		TBD	TBD	MHz
tCSSM	SCS- Setup Time		TBD	-	ns
tCSHM	SCS- Hold Time		-	TBD	ns
tWLM	SCLK Low		-	TBD	ns
tWHM	SCLK High		-	TBD	ns
tCSM	SCS- High Time		-	TBD	ns
tSUM	Data-In Setup Time		-	TBD	ns
tHM	Data-In Hold Time		-	TBD	ns
tVM	Data-Out Valid Time		-	TBD	ns
tHDM	Data-Out Hold Time		-	TBD	ns
tDISM	Data-Out Disable Time		-	TBD	ns

TIMING DIAGRAMS

UNDER CONSTRUCTION

ORDERING INFORMATION

TBD

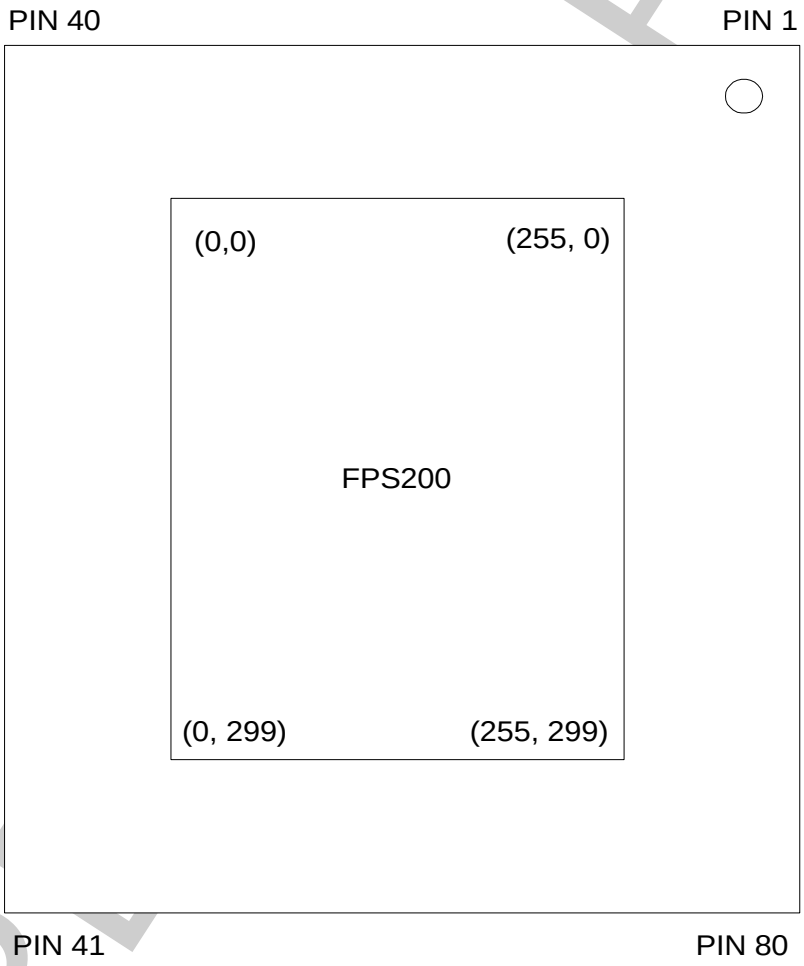
PHYSICAL DIMENSIONS

TBD

RECOMMENDED LAND PATTERN

TBD

ARRAY ORIENTATION



DEVICE REVISION SUMMARY

Revision	Date	Description
-	-	-

DATASHEET REVISION SUMMARY

Revision	Date	Description
Advance Information		
0.2	April 29, 2000	Datasheet short.
0.3	May 5, 2000	Added more text.
0.4	May 27, 2000	Corrected block diagram. Added more text.

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