Veridicom

**FPS100**

Solid-State Fingerprint Sensor

## Features

- 300 × 300 sensor array
- 500-dpi resolution
- Standard CMOS technology
- Sensor pitch: 50 µm
- 1.5 cm × 1.5 cm sensor area
- Ultra-hard protective coating
- Integrated 8-bit flash analog-to-digital converter
- 8-bit microprocessor interface
- VSPA 80/1 package
- Low power, 100 mW
- Low cost
- Non-optical solid-state device

## Applications

- Database and network access
- Portable fingerprint acquisition
- Access control (home, auto, office, etc.)
- ATM
- Smart cards
- Cellular phone security access

## Overview

The Veridicom FPS100 Solid-State Fingerprint Sensor is a direct contact, fingerprint acquisition device. It is a high performance, low power, low cost, capacitive sensor with an integrated two-dimensional array of metal electrodes in the sensing array. Each metal electrode acts as one plate of a capacitor and the contacting finger acts as the second plate. A passivation layer on the device surface forms the dielectric between these two plates. Ridges and valleys on the finger yield varying capacitor values across the array, which is read to form an image of the fingerprint.

The FPS100 is manufactured in standard CMOS technology and is available in an 80-pin, VSPA 80/1. The 300 × 300 sensor array has a 50 µm pitch and yields a 500-dpi image. The sensor surface is protected by a patented, ultra-hard, abrasion and chemical resistant coating.

A block diagram of the FPS100 is shown in Figure 1. The FPS100 has an integrated 8-bit flash analog-to-digital converter to digitize the output of the sensor array. The Fingerprint Sensor has an 8-bit bi-directional bus interface compatible with most microprocessors.

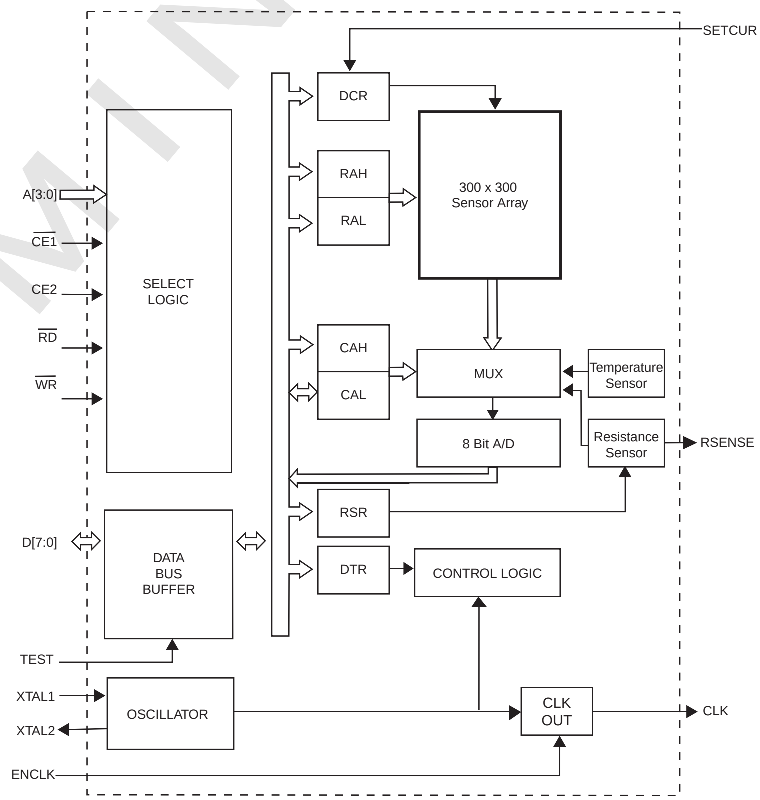



**Figure 1. FPS100 Block Diagram**

## Chip Operation

The sensor array is composed of 300 rows and 300 columns of sensor plates. Associated with each column are two sample-and-hold circuits. A fingerprint image is sensed or captured one row at a time. This “row capture” occurs in two phases. In the first phase, the sensor plates of the selected row are pre-charged to the $V_{DD}$ voltage. During this pre-charge period, an internal signal enables the first set of sample-and-hold circuits to store the pre-charged plate voltages of the row.

In the second phase, the row of sensor plates is discharged with a current source. The rate at which a cell is discharged is proportional to the “discharge current.” After a period of time (referred to as the “discharge time”), an internal signal enables the second set of sample-and-hold circuits to store the final plate voltages. The difference between the pre-charged and discharged plate voltages is a measure of the capacitance of a sensor cell. After the row capture, the cells within the row are ready to be digitized.

The sensitivity of the chip is adjusted by changing the discharge current and discharge time. The nominal value of the current source is controlled by an external resistor connected between the SETCUR pin and ground. The current source is controlled from the Discharge Current Register (DCR). The discharge time is controlled by the Discharge Time Register (DTR).

The sensor array is a row-oriented device. Images are read out one row at a time. The High-Order Row Address Register (RAH) and the Low-Order Row Address Register (RAL) must be programmed to select a row to be captured. Writing to RAL initiates a row capture. The capture time is a function of the external clock and the DTR. After the discharge cycle, the outputs of the row elements will be stored in analog sample and hold circuits.

After the row capture is completed, the High-Order Column Address Register (CAH) and Low-Order Column Address Register (CAL) must be programmed to select an element within the captured row to be digitized. Writing to CAL causes the analog-to-digital (A/D) converter to digitize the difference between the outputs of the two sample-and-holds of the selected column cell. The output of the A/D converter is accessed by reading the CAL register.

Rows can be accessed in any order; however, the selected row must be captured before the column cells are read. The column cells within a row can be accessed in any order.

## Special Features

The FPS100 has an integrated temperature sensor and resistance sensor. The temperature sensor output changes by 1 DAC step per degree Celsius. This can be used as a relative measurement to determine temperature changes in the fingerprint sensor.

The resistance sensor can be used to measure the value of a resistance external to the chip. A current source controlled by the Resistance Sensor Register (RSR) drives the RSENSE pin. The A/D Converter can read the voltage developed at the RSENSE pin.

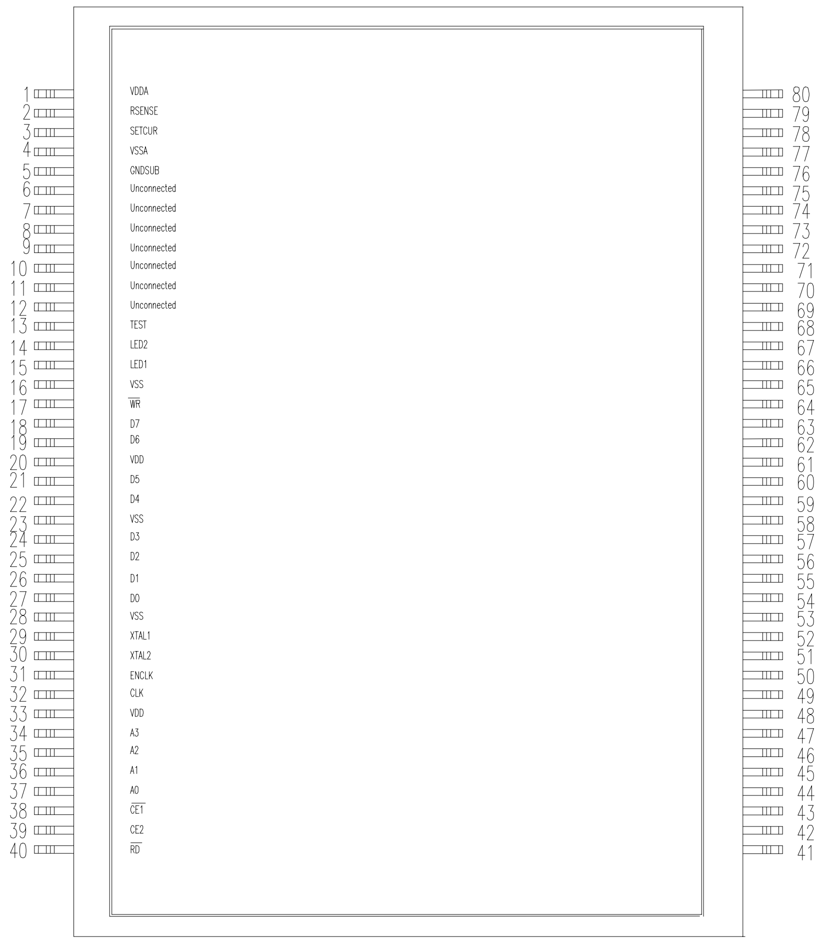
There are two programmable open-drain outputs that can be used for driving LEDs.

The CLK pin can be enabled to output a square-wave clock of the same frequency as the oscillator clock. CLK can be used to drive external circuitry. When ENCLK is high, the clock signal is present at the CLK pin. When ENCLK is low or unconnected, the CLK output is held low.

## FPS100 Pin Information for VSPA 80/1

| Pin Number | Pin Name | Type | Description | Notes |
|---|---|---|---|---|
| 34 | A3 | Input | Address Inputs | Address signals connected to these pins select a register to read from or write to during data transfer. |
| 35 | A2 | | | |
| 36 | A1 | | | |
| 37 | A0 | | | |
| 38 | $\overline{CE1}$ | | Chip Enable, Active Low | When $\overline{CE1}$ is low and CE2 is high, the chip is selected. |
| 39 | CE2 | | Chip Enable, Active High | When $\overline{CE1}$ is low and CE2 is high, the chip is selected. |
| 40 | $\overline{RD}$ | | Read Enable, Active Low | This pin must be low while $\overline{WR}$ is high and the chip selected in order to read a register on the chip. |
| 17 | $\overline{WR}$ | | Write Enable, Active Low | This pin must be low while the chip is selected to write to a register on the chip. |
| 18 | D7 | Bi-directional | Data Bus | Inputs when $\overline{WR}$ is low and chip is selected. Outputs when $\overline{RD}$ is low, $\overline{WR}$ is high, and chip is selected. |
| 19 | D6 | | | |
| 21 | D5 | | | |
| 22 | D4 | | | |
| 24 | D3 | | | |
| 25 | D2 | | | |
| 26 | D1 | | | |
| 27 | D0 | | | |
| 32 | CLK | Output | Clock Output | This pin outputs the oscillator clock frequency when ENCLK is high. |
| 31 | ENCLK | Input | Enable Clock Output | A high on this pin enables the CLK pin. A low on this pin holds CLK low. ENCLK has an internal pull-down resistor. |
| 15 | LED1 | Open-drain Output | LED driver | This pin can be used to drive an LED. |
| 14 | LED2 | Open-drain Output | | |
| 2 | RSENSE | Output | Resistor Sense | An external resistance can be sensed across this pin to GND. |
| 3 | SETCUR | Input | Set Discharge Current | An external resistor from this pin to GND sets the nominal value of the Discharge Current. |
| 13 | TEST | | Reserved pin | Must be left disconnected. |
| 20, 33 | $V_{DD}$ | Power | Digital Power Supply | |
| 1 | $V_{DDA}$ | | Analog Power Supply | |
| 16, 23, 28 | $V_{SS}$ | Ground | Digital ground | |
| 4 | $V_{SSA}$ | | Analog ground | |
| 5* | GNDSUB | | Ground substrate | *Applies to package FPS100-P2 only. |
| 29 | XTAL1 | Input | Input to the On-Chip Oscillator | To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing. |
| 30 | XTAL2 | Output | Output of the On-Chip Oscillator | If an external oscillator is used, leave XTAL2 unconnected. |
| 41-80 | GNDSHLD | Shield Ground | Connected to Package Top Plate | These pins should connect to chassis ground. |
| 6-12 | N/A | N/A | | Not connected. |

## FPS100 Connection Diagram



## Function Table

| $\overline{CE1}$ | CE2 | $\overline{RD}$ | $\overline{WR}$ | Mode | Data Lines |
|---|---|---|---|---|---|
| H | X | X | X | De-selected | High-Z |
| X | L | X | X | De-selected | High-Z |
| L | H | H | H | Standby | High-Z |
| L | H | L | H | Read | Data Out |
| L | H | H | L | Write | Data In |

## Register Map

| A3 | A2 | A1 | A0 | Access | Register | Description |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Write | RAL | Low Order Row Address Register |
| 0 | 0 | 0 | 1 | Write | RAH | High Order Row Address Register |
| 0 | 0 | 1 | 0 | Read/Write | CAL | Low Order Column Address Register |
| 0 | 0 | 1 | 1 | Write | CAH | High Order Column Address Register |
| 0 | 1 | 0 | 0 | Write | DTR | Discharge Time Register |
| 0 | 1 | 0 | 1 | Write | DCR | Discharge Current Register |
| 0 | 1 | 1 | 0 | Write | RSR | Resistance Sense Register |

## Address Register Descriptions

Refer to *Row Capture and A/D Conversion Timing* on page 10 to calculate row capture and A/D conversion times.

### RAL (A3-A0 Address 0000) Write Only

**Low Order Row Address Register**
This register and bit 0 of RAH form the 9-bit Row Address Register that selects the row to be captured. The 9-bit Row Address Register selects a row address from 0 through 299. Writing the RAL starts a row capture. Only RAL has to be written if RAH doesn't change, otherwise RAH has to be written before RAL.

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |

| Bit Number | Bit Name | Function |
|---|---|---|
| [7:0] | RA[7:0] | Low eight bits of Row Address Register. |

### RAH (A3-A0 Address 0001) Write Only

**High Order Row Address Register**
Bit 0 of this register and RAL form the 9-bit Row Address Register that selects the row to be converted. The L1 and L2 bits control two open-drain outputs that can be used to drive LEDs.

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| L1 | L2 | - | - | - | - | - | RA8 |

| Bit Number | Bit Name | Function |
|---|---|---|
| 7 | L1 | L1=0, LED1 output low<br>L1=1, LED1 output high-Z |
| 6 | L2 | L2=0, LED 2 output low<br>L2=1, LED 2 output high-Z |
| [5:1] | - | Reserved, write 0 to these bits. |
| 0 | RA8 | MSB of Row Address |

## CAL (A3-A0 Address 0010) Read/Write

**Low Order Column Address Register**

CAL is a read/write register. Writing to this address writes to the low-order 8 bits of the 9-bit Column Address Register. The 9-bit Column Address Register selects a column from 0 through 299. Writing to CAL causes the analog-to-digital (A/D) converter to begin digitizing its input. The input of the A/D converter is selected by bits 7 and 6 of the CAH register. The user should wait until the row capture is completed before writing to the CAL.

Reading from this address returns the output of the A/D converter. After writing to CAL, the user should wait until A/D conversion completes before reading the A/D converter.

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| CA7 | CA6 | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |

| Bit Number | Bit Name | Function |
|---|---|---|
| [7:0] | CA[7:0] | (WRITE) Low eight bits of Column Address Register.<br>(READ) Output of A/D converter. |

## CAH (A3-A0 Address 0011) Write Only

**High Order Column Address Register**

Bit 0 of this register and CAL form the 9-bit Column Address Register that selects a cell from the current row for digitizing. The user should wait until the row capture is completed before writing to CAH.

Bits 7 and 6 of the CAH register select the source of the input to the A/D converter. These two bits select whether the A/D converter digitizes: 1) the cell from the selected row and column, 2) the output of the Temperature Sensor, or 3) the Resistance Sensor. After writing bits R and T, the CAL register must be written in order to cause the A/D converter to digitize its input.

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| R | T | - | - | - | - | - | CA8 |

| Bit Number | Bit Name | Function |
|---|---|---|
| [7:6] | R, T | These bits select the input to the A/D converter.<br><br>R   T   Selects<br>0   0   Cell of Sensor Array<br>0   1   Temperature Sensor<br>1   0   Resistance Sensor<br>1   1   Not allowed |
| [5:1] | - | Reserved, write 0 to these bits. |
| 0 | CA8 | MSB of Column Address Register |

## DTR (A3-A0 Address 0100) Write Only

### Discharge Time Register

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| PD | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

| Bit Number | Bit Name | Function |
|---|---|---|
| 7 | PD | Power Down Chip.<br>PD=0, Chip in Normal Mode<br>PD=1, Chip in Low Power Mode |
| [6:0] | T[6:0] | Selects the count to be loaded into the Discharge Timer. Discharge time is selected in increments of the oscillator period. Discharge Time is defined as the period between the sampling and holding of the pre-charged sensor cell to the sampling and holding of the discharging sensor cell. The Discharge Time can be calculated from the following equation:<br><br>Discharge Time = T[6:0] * $t_{OSC}$ |

## DCR (A3-A0 Address 0101) Write Only

### Discharge Current Register

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| F2 | F1 | TRST | DC4 | DC3 | DC2 | DC1 | DC0 |

| Bit Number | Bit Name | Function |
|---|---|---|
| [7:6] | F2, F1 | These two bits tell the chip the frequency of the external oscillator or crystal that is connected to the chip.<br><br>F2 F1 XTAL Input<br>0 0 10-15 MHz<br>0 1 15-20 MHz<br>1 0 20-30 MHz<br>1 1 30-40 MHz |
| 5 | TRST | Timer Reset. Set this bit to halt and reset the Discharge Timer. Resetting the Discharge Timer is necessary to put the Discharge Timer in a known state after power-up or after returning to Normal mode from Low-power mode (See bit 7 of DTR).<br><br>TRST=0, Normal Timer Operation<br>TRST=1, Halt and Clear Discharge Timer (doesn't clear DTR) |
| [4:0] | DC[4:0] | Selects the Discharge Current source value. |

## RSR (A3-A0 Address 0110) Write Only

**Resistance Sensor Register**

RSR bits R[3:0] control the output of the current source of the Resistor Sensor. An external resistance between the RSENSE pin and ground can be measured by setting the R[3:0] bits to output a current so that a voltage between 0 and 1.2V will be developed across the external resistance and ground. Then the voltage at the RSENSE pin can be digitized by the internal A/D converter.

MSB LSB

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| OT | TB | - | - | R3 | R2 | R1 | R0 |

| Bit Number | Bit Name | Function |
|---|---|---|
| 7 | OT | Reserved. Write 0 to this bit. |
| 6 | TB | Reserved. Write 0 to this bit. |
| [4:5] | - | Reserved. Write 0 to these bits. |
| [3:0] | R[3:0] | These bits control the output of a current source that drives the RSENSE pin. The current output on RSENSE is calculated as follows: $I_{RSENSE} = (R3*100+R2*10+R1*1+R0*0.1) * I_{REFERENCE}$ where $I_{REFERENCE} = \frac{1.2V}{R_{SETCUR}}$ and $R_{SETCUR}$ is the value of the resistor between the SETCUR pin and ground. For example R[3:0] = 1000b sets the current source to 100 times the reference current. R[3:0] = 0100b sets the current source equal to 10 times the reference current. R[3:0] = 0001b sets the current source to 1/10th of the reference current. |

## Row Capture and A/D Conversion Timing

| F2 | F1 | XTAL Input Range | Row Capture Time in OSC Clock Periods | A/D Conversion Time in OSC Clock Periods |
|---|---|---|---|---|
| 0 | 0 | 10-15 MHz | 18+n | 13 |
| 0 | 1 | 15-20 MHz | 24+n | 15 |
| 1 | 0 | 20-30 MHz | 36+n | 23 |
| 1 | 1 | 30-40 MHz | 48+n | 30 |

NOTE: n is selected by bits T[6:0] of DTR.

## A/D Converter

The integrated 8-bit flash A/D converter is a buffered device. Each write to CAL causes: 1) the result of the previous conversion to be latched and made readable at CAL, and 2) the A/D converter to start digitizing its current input. Consequently, it takes 301 writes to CAL in order to digitize the 300 cells of a row. To digitize the output of the temperature or resistance sensor, CAL must be written twice—once to digitize the input and a second time to make the result readable at CAL.

## Specifications*

### Absolute Maximum Ratings

- Storage Temperature: -65° to +150° C
- DC Voltage Applied to any Pins: -0.5 V to +7.0 V
- Electrostatic Discharge Voltage: >2000 Volts
- Latch Up Current: >100 mA

### Operating Range

- Ambient Temperature: 0° C to 70° C
- $V_{DD}$ (Digital Supply Voltage): +4.3V to +5.5 V
- $V_{DDA}$ (Analog Supply Voltage): +3.0 V to +5.5 V
- Oscillator Frequency: 10 MHz to 40 MHz

### Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{DD}$=min, $I_{OH}$=-4mA | 2.4 | - | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$=min, $I_{OL}$=8mA | - | 0.4 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | | -0.5 | 0.8 | V |
| $I_{IX}$ | Input Current | GND< $V_{in}$ <$V_{CC}$ | -5.0 | 5.0 | µA |
| $I_{OZ}$ | Output Leakage Current | GND< $V_{out}$ <$V_{DD}$ | -5.0 | 5.0 | µA |
| $I_{CC}$ | Supply Current | $V_{DD}$=max | - | 20 | mA |
| $I_{CC}$pd (Power Down) | Supply Current | $V_{DD}$=max | - | 1 | mA |
| ADCM | ADC Monotonicity | | 8.0 | - | bits |
| $V_{temp}$ | Temperature measurement | | 0.5 | 1.5 | bits/C |

### Switching Characteristics

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| FIN | Frequency in, XTAL1 | 10 | 40 | MHz |

***Note**: All specifications in this document are preliminary and subject to change without notice.

## Read Cycle

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AAC}$ | Address valid to data valid. | - | 70 | ns |
| $t_{RC}$ | Read Cycle Time | 70 | - | ns |
| $t_{ACE1}$ | $\overline{CE1}$ low to data valid | - | 70 | ns |
| $t_{ACE2}$ | CE2 high to data valid | - | 70 | ns |
| $t_{DOE}$ | $\overline{RD}$ low to data valid | - | 35 | ns |
| $t_{LZOE}$ | $\overline{RD}$ low to low Z | 5 | - | ns |
| $t_{HZOE}$ | $\overline{RD}$ high to high Z | - | 30 | ns |
| $t_{LZCE}$ | $\overline{CE1}$ low and CE2 high to low Z | 5 | - | ns |
| $t_{HZCE}$ | $\overline{CE1}$ high to high Z or CE2 low to high Z | - | 30 | ns |
| $t_{LZWE}$ | $\overline{WR}$ high to low Z | 5 | - | ns |
| $t_{HZWE}$ | $\overline{WR}$ low to high Z | - | 30 | ns |

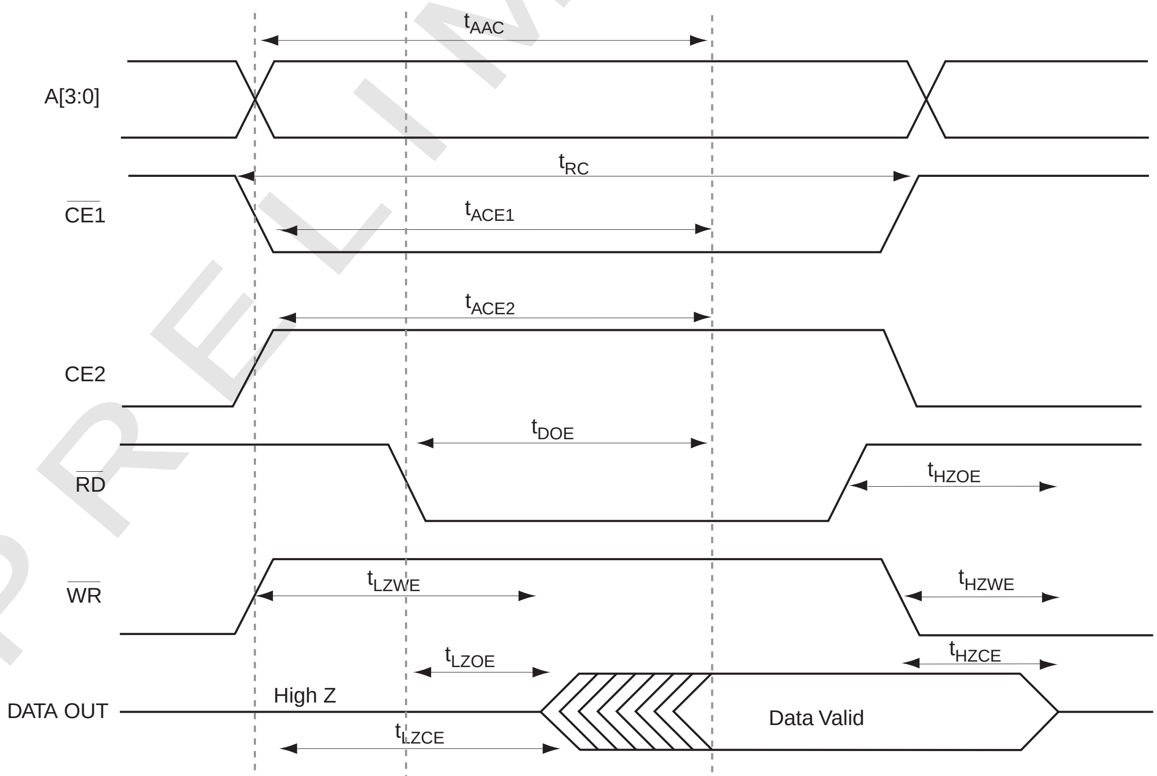



**Figure 2. Read Cycle Timing**

## Write Cycle

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle | 70 | - | ns |
| $t_{SCE1}$ | $\overline{CE1}$ low to write end | 60 | - | ns |
| $t_{SCE2}$ | CE2 high to write end | 60 | - | ns |
| $t_{AW}$ | Address setup to write end | 55 | - | ns |
| $t_{HA}$ | Address hold from write end | 0 | - | ns |
| $t_{SA}$ | Address set-up to write start | 0 | - | ns |
| $t_{PWE}$ | $\overline{WR}$ Pulse Width | 40 | - | ns |
| $t_{SD}$ | Data setup to write end | 35 | - | ns |
| $t_{HD}$ | Data hold from write end | 0 | - | ns |

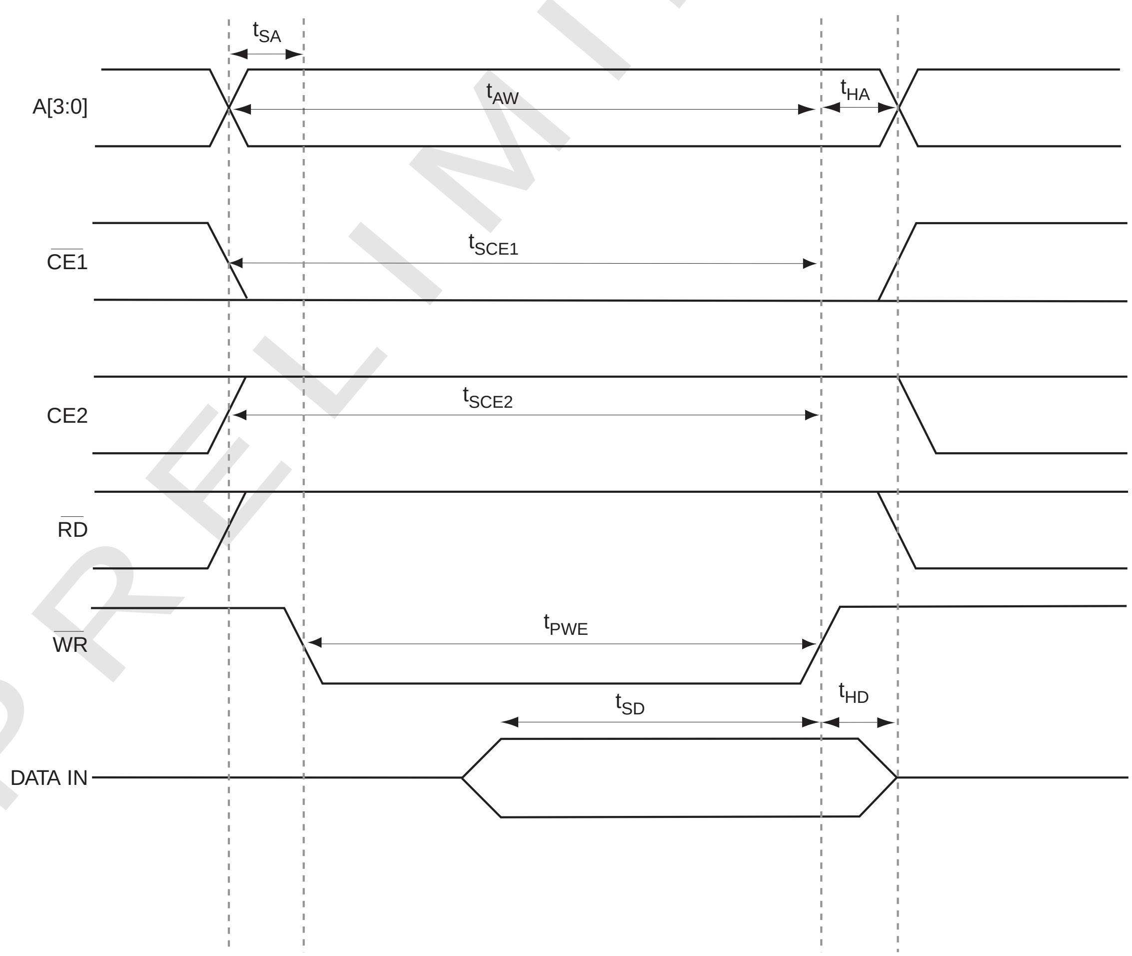
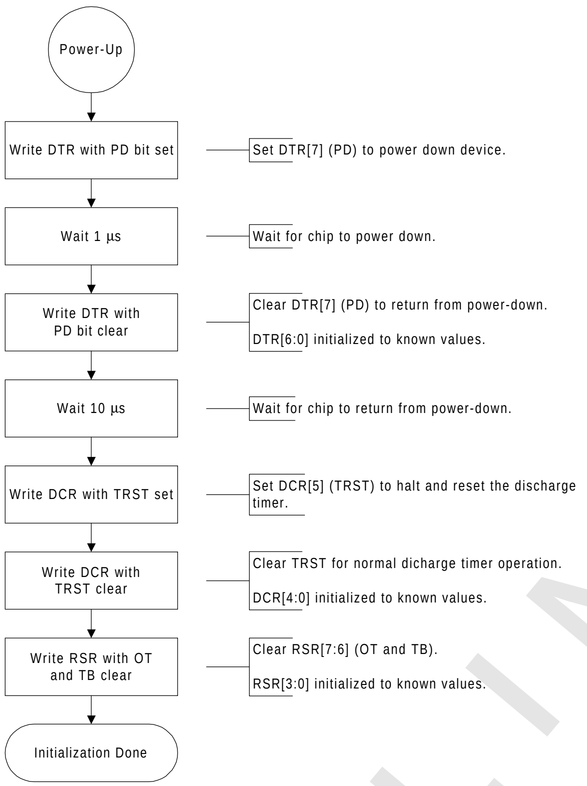
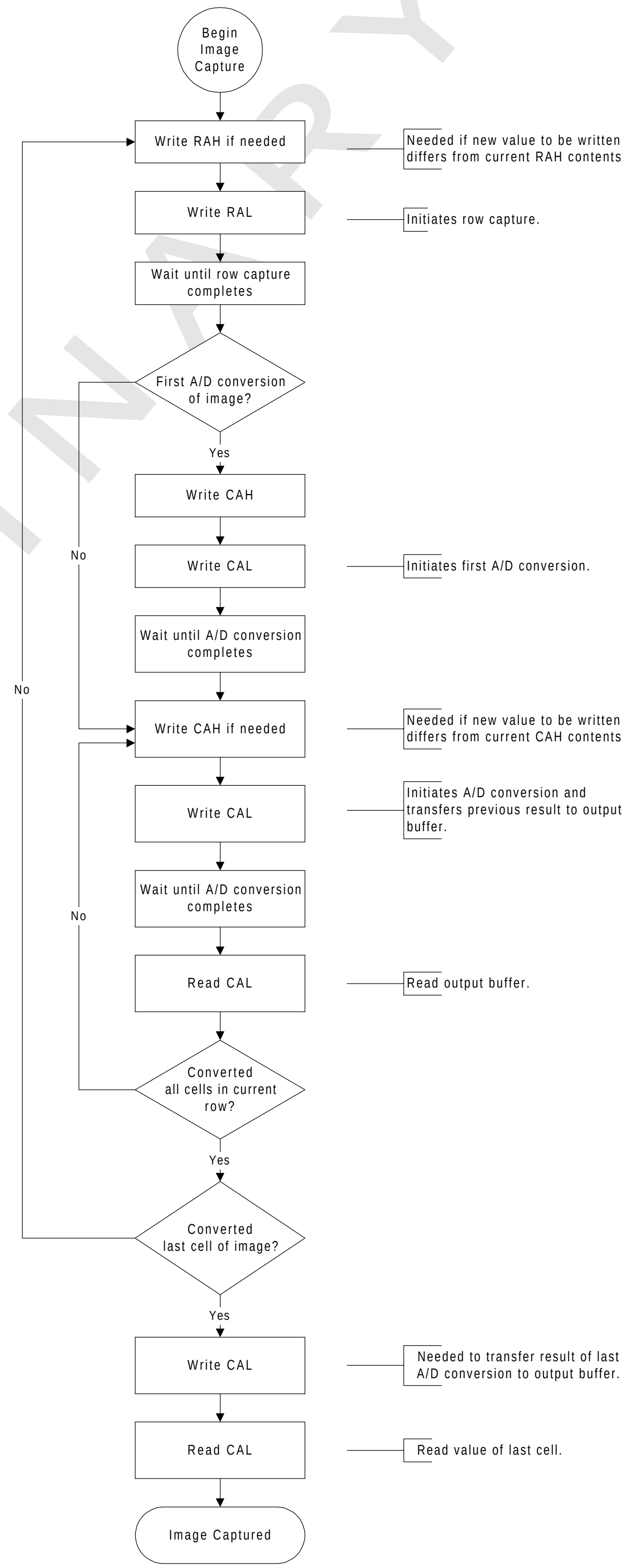



**Figure 3. Write Cycle Timing**

## Power Up and Initialization



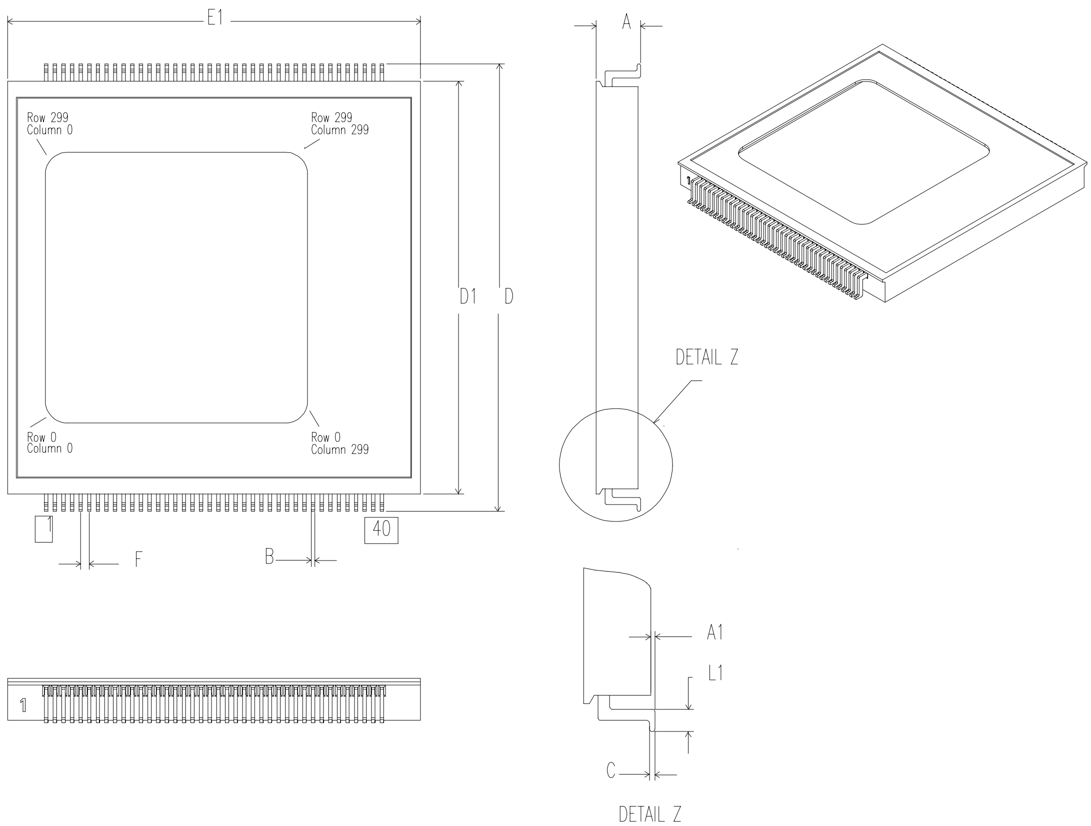

## Image Capture



## FPS100 Package

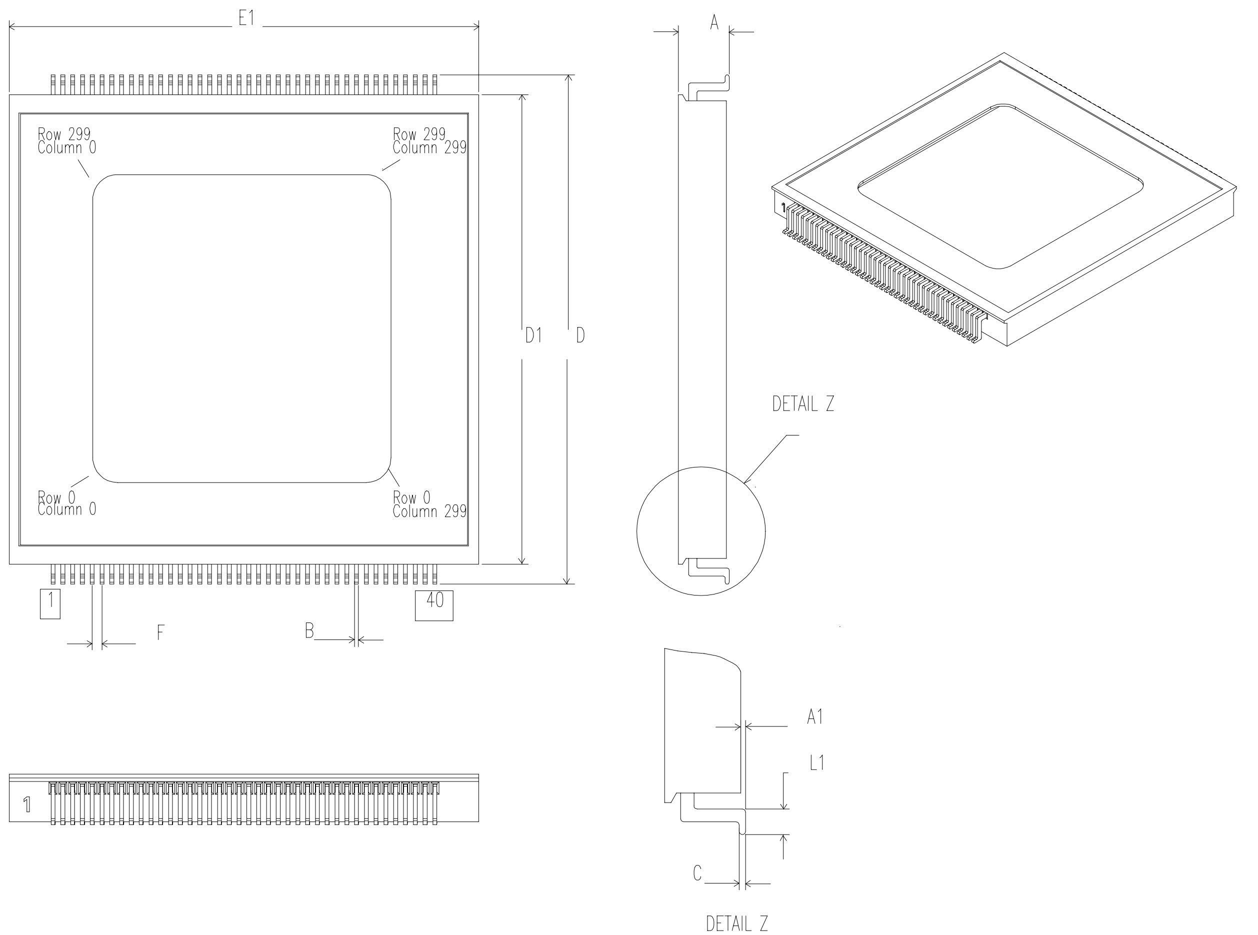
The FPS100 is shown below in two VSPA 80/1 packages: FPS100-P1, whose sensor window is offset in the package; and FPS100-P2, whose sensor window is centered in the package. The FPS100-P1 is currently available, but will be replaced in late 1998 by the FPS100-P2. Veridicom is also actively pursuing other packaging options. For more information, contact Veridicom.

### FPS100-P1 Assembly

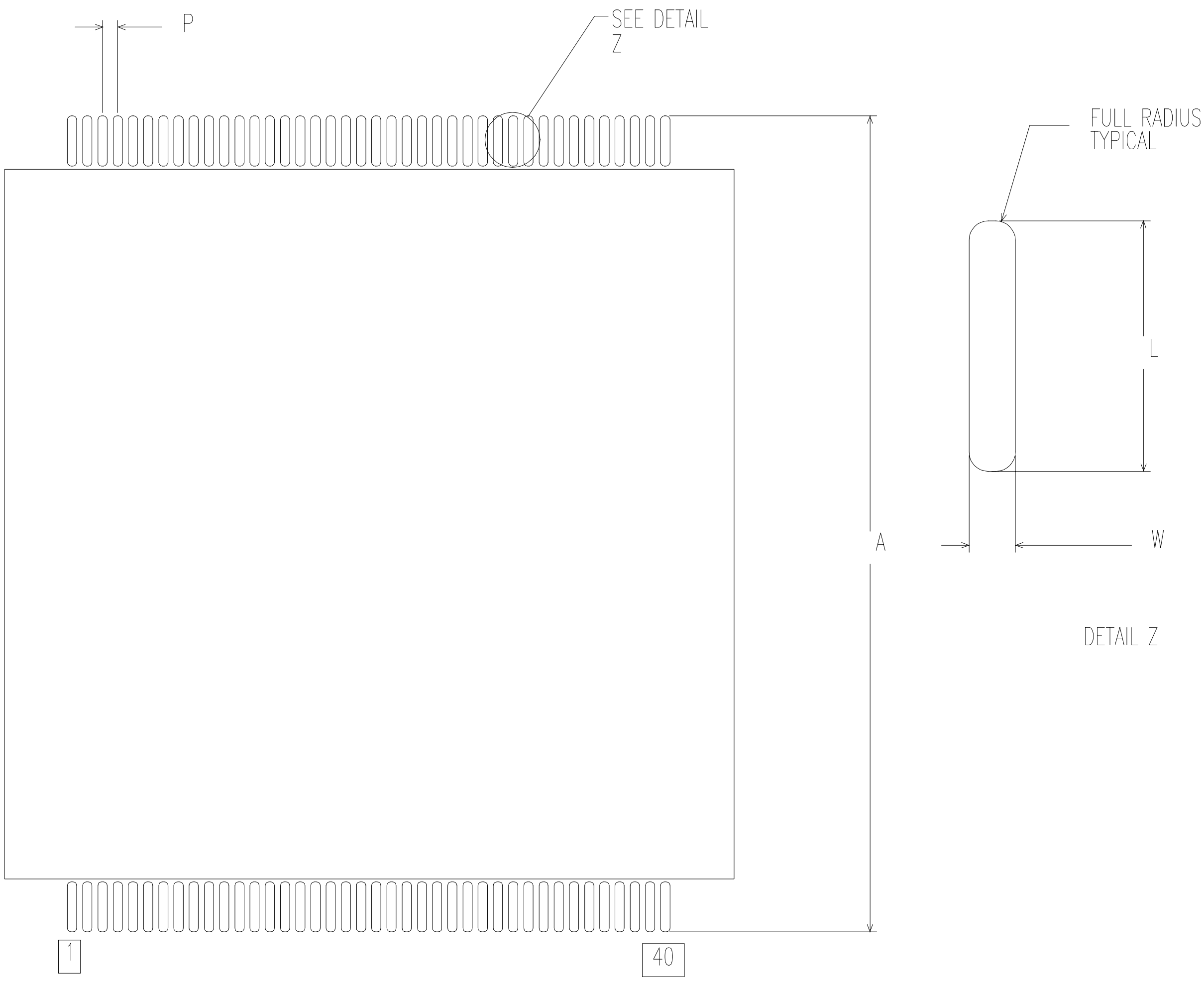



| FPS100-P1 and FPS100-P2 Dimensions | | | | |
|---|---|---|---|---|
| **Symbol** | **Description** | **Min** | **Nom** | **Max** |
| N | Pin Count | | 80 | |
| A | Overall Height | | .102 (2.60) | |
| A1 | Stand Off | | .006 (.15) | |
| B | Pin Width | | .008 (.20) | |
| C | Pin Thickness | | .008 (.20) | |
| D | Tip to tip Dimension | 1.016 (25.8) | 1.025 (26.0) | 1.032 (26.2) |
| D1 | Package Body | .941 (23.9) | .945 (24.0) | .949 (24.1) |
| E1 | Package Body | .941 (23.9) | .945 (24.0) | .949 (24.1) |
| F | Pin Pitch | .0187 (.47) | .0197 (.50) | .0207 (.53) |
| L1 | Foot length | | .032 (.81) | |
| Note: Dimensions are in inches (mm) | | | | |

## FPS100-P2 Assembly



## FPS100-P1 and FPS100-P2 Solder Pad Layout




| Symbol | Description | Dimension |
|---|---|---|
| N | Pin Count | 80 |
| A | Tip to Tip Dimension | 1.059 (26.9) |
| P | Pitch | .0197 (.50) |
| L | Pad Length | .065 (1.65) |
| W | Pad Width | .012 (.30) |
| Note: Dimensions are in inches (mm) | | |