OKI Semiconductor

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MSM7617

2-Channel Echo Canceler

GENERAL DESCRIPTION

The MSM7617 cancels echoes (acoustic or line echoes) generated in voice channels. It is a low-power CMOS LSI device with two channels.

MSM7617 echo canceling is performed by digital signal processing. It negates echoes by estimating the echo channel and then generating a pseudo-echo signal.

When used as an acoustic echo canceler, the MSM7617 can cancel acoustic echoes between speaker and microphone that occur during hands-free speaking with car phones, conferencing system phones, etc. When used as a line echo canceler, the MSM7617 can cancel line echoes returned by hybrid impedance mismatches.

By setting its mode for use as a single cross-connected channel, the MSM7617 can cancel both acoustic and line echoes.

Also, the MSM7617 can improve voice communication by using its howling detection, double-talk detection, attenuation, and gain control functions to prevent and suppress howling levels, and by using its center clipping function to suppress low level noise.

Furthermore, the MSM7617 can disable echo canceling during data communication with its 2100 Hz tone detector and 2100 Hz phase reversal detector. It also provides the ability to attenuate SIN levels, to amplify SOUT levels, and to adjust input/output levels.

An economical and highly efficient echo canceler unit can be constructed by using a 2-channel single-chip CODEC like the MSM7533 together with the MSM7617.

FEATURES

- Echo canceler has two channels, which can be used for acoustic and line echoes. Set as a single cross-connected channel, it can be used for both acoustic and line echoes.

- ITU-T G164/G165 standard tone disabler.

- PCM line level adjustment possible with SIN level attenuator (SA pin) and SOUT level amplifier (SG pin). Can also be used for ERL amplification with the SIN level attenuator (SA pin).

- RGC pin provides input/output adjustment mode (±6LR mode) that can prevent malfunction due to excessive inputs without changing the RIN-ROUT input/output levels.

- Cancelable echo delay time: 55 ms (max.)

- Echo attenuation: 30 dB (typ.)

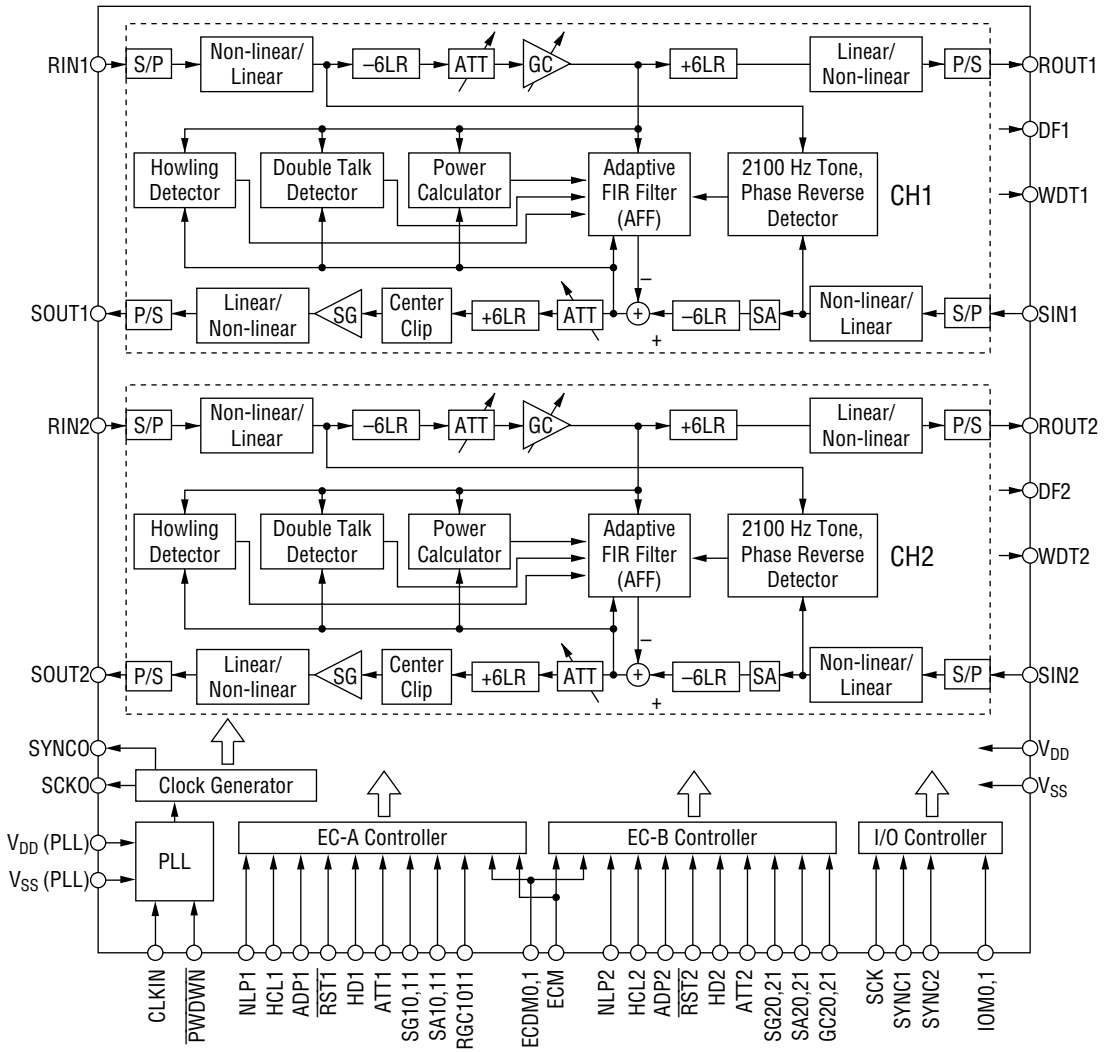
- Clock frequency: 18 to 20 MHz
  19.2 MHz if using internal clock signal

- Power supply voltage: 4.5 to 5.5 V

- Package: 64-pin plastic QFP (QFP64-P-1414-0.80-BK)

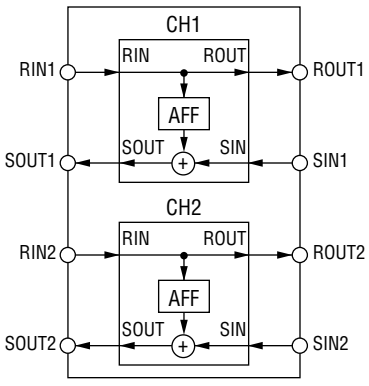
- Product name: MSM7617-001GS-BK (μ-law)

BLOCK DIAGRAM

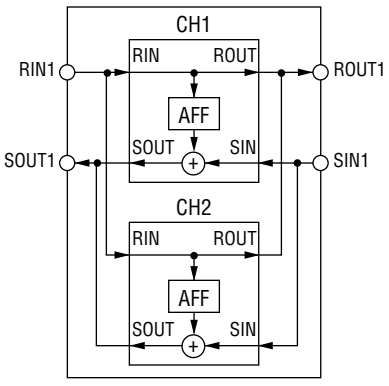


The above diagram shows internal connections for 2-channel parallel mode. The internal connections for 2-channel serial I/O mode and 1-channel cross-connected mode are shown below.

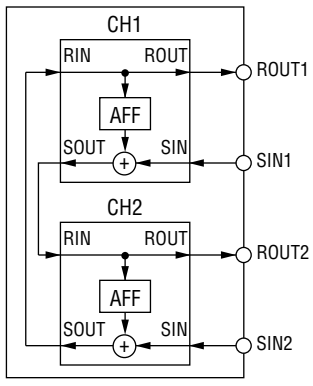
2-channel parallel I/O mode



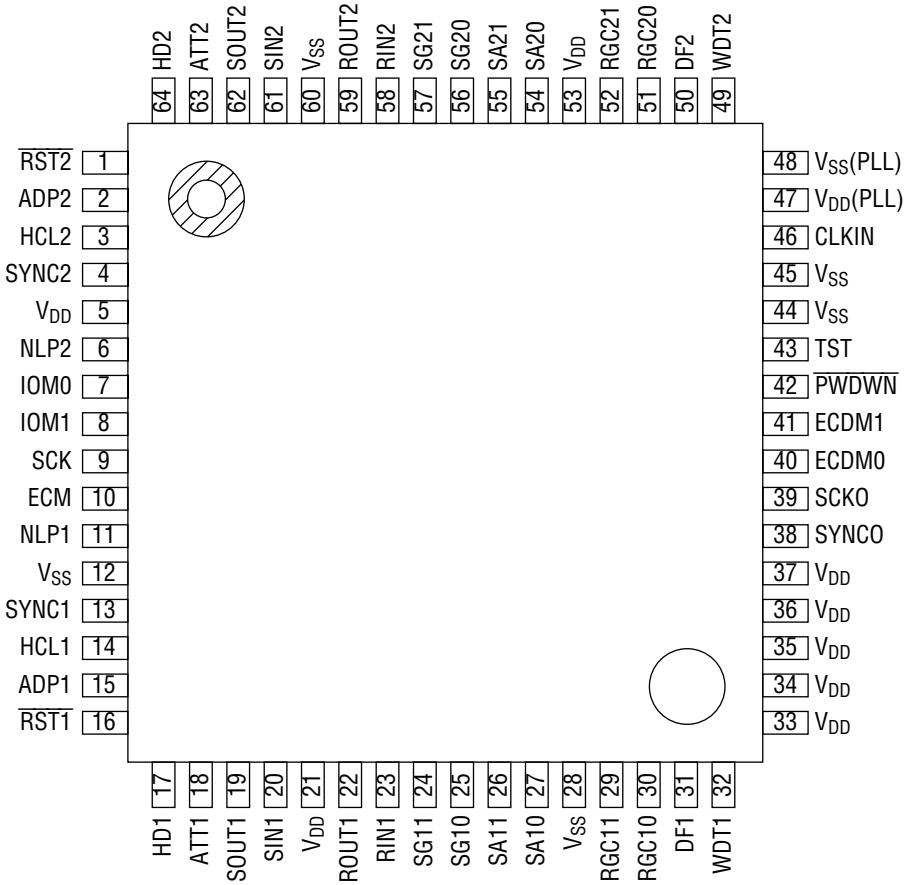
2-channel serial I/O mode



1-channel cross-connected mode



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	$\overline{RST2}$	I	Reset signal input pin for channel 2. "L": Reset "H": Normal operation Input signals are invalid for 100 μs after reset (after $\overline{RST}$ returns to "H" from "L") for setting initial values. Input the basic clock during reset. Output pins will be placed in the following states during reset. Hi-Z: ROUT2, SOUT2 No effect: SYNCO, SCKO, ROUT1, SOUT1, DF1, WDT1 Previous state: DF2, WDT2 After the power is turned on, initialize the LSI's internal registers by your execution of H→L sequence 1μs later than the master clock starts normal oscilation. This LSI starts a normal operation by releasing this pin to H after the H→L sequence above. Here, this pin must stay L for 1μs or longer.
2	ADP2	I	AFF coefficient control pin for channel 2. This pin stops coefficient variation of the adaptive FIR filter (AFF), fixing the coefficients. It allows once acquired AFF coefficients to be saved. "H": Fixed coefficient mode "L": Normal mode (variable coefficients)
3	HCL2	I	Echo canceler disable pin for channel 2. This pin disables the echo canceler and enables data from SIN to SOUT to be output in "through mode". The input and output levels of SIN and SOUT are changed by the setting of the SG and SA pins; therefore, to output data from SIN to SOUT in "through mode", set the SA and SG pins to "0 dB". It simultaneously clears the adaptive FIR filter coefficients. "H": Disable mode "L": Normal mode (echo canceller enabled)
4	SYNC2	I	Sync signal input pin for channel 2 transmit/receive PCM data while in parallel I/O mode. Input the transmit/receive sync signal (8 kHz) of the PCM CODEC connected to channel 2. Input "L" if not in parallel I/O mode.
6	NLP2	I	NLP control pin for channel 2. This pin controls center clipping, forcing SOUT2 output to the minimum positive value when it is below –54 dBm0. It is effective for reducing uncanceled echoes and low-level noise. "H": Center clipping on "L": Center clipping off

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>7
8</td><td>IOM0
IOM1</td><td>I</td><td>Sets I/O mode of PCM data.
<table>
<tr><th>IOM1</th><th>IOM0</th><th>Mode Setting</th></tr>
<tr><td>0</td><td>0</td><td>2-channel parallel I/O mode</td></tr>
<tr><td>0</td><td>1</td><td>2-channel serial I/O mode</td></tr>
<tr><td>1</td><td>0</td><td>1-channel cross-connected mode</td></tr>
<tr><td>1</td><td>1</td><td>Inhibited</td></tr>
</table></td></tr>
<tr><td>9</td><td>SCK</td><td>I</td><td>Common pin for channel 1 and channel 2. Clock input pin for PCM data transmission.
Input the same clock as the transmit/receive clock of the PCM CODEC.
Frequencies below 128 kHz cannot be used in serial mode.</td></tr>
<tr><td>10</td><td>ECM</td><td>I</td><td>Not used. Fix input to "H".</td></tr>
<tr><td>11</td><td>NLP1</td><td>I</td><td>NLP control pin for channel 1.
This pin controls center clipping, forcing SOUT1 output to the minimum positive value when it is below –54 dBm0. It is effective for reducing uncancelled echoes and low-level noise.
"H": Center clipping on
"L": Center clipping off</td></tr>
<tr><td>13</td><td>SYNC1</td><td>I</td><td>Sync signal input pin for channel 1 transmit/receive PCM data while in 2-channel parallel I/O mode, 2-channel serial I/O mode, or 1-channel cross-connected mode.
Input the transmit/receive sync signal (8 kHz) of the PCM CODEC.</td></tr>
<tr><td>14</td><td>HCL1</td><td>I</td><td>Echo canceler disable control pin for channel 1.
This pin disables the echo canceler and enables data from SIN to SOUT to be output in "through mode". The input and output levels of SIN and SOUT are changed by the setting of the SG and SA pins; therefore, to output data from SIN to SOUT in "through mode", set the SA and SG pins to "0 dB".
It simultaneously clears the adaptive FIR filter coefficients.
"H": Disable mode
"L": Normal mode (echo canceler enabled)</td></tr>
<tr><td>15</td><td>ADP1</td><td>I</td><td>AFF coefficient control pin for channel 1.
This pin stops coefficient variation of the adaptive FIR filter (AFF), fixing the coefficients. It allows once acquired AFF coefficients to be saved.
"H": Fixed coefficient mode
"L": Normal mode (variable coefficients)</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
16	$\overline{\text{RST1}}$	I	Reset signal input pin for channel 1. "L": Reset "H": Normal operation Input signals are invalid for 100 μs after reset (after $\overline{\text{RST}}$ returns to "H" from "L") for setting initial values. Input the base clock during reset. Output pins will be placed in the following states during reset. Hi-Z: ROUT1, SOUT1 No effect: SYNCO, SCKO, ROUT2, SOUT2, DF2, WDT2 Previous state: DF1, WDT1 After the power is turned on, initialize the LSI's internal registers by your execution of H→L sequence 1μs later than the master clock starts normal oscilation. This LSI starts a normal operation by releasing this pin to H after the H→L sequence above. Here, this pin must stay L for 1μs or longer.
17	HD1	I	Howling detection control pin for channel 1. This pin controls detection and canceling of howling generated by the acoustics of handsfree telephones. "L": Howling detector on "H": Howling detector off
18	ATT1	I	ATT control pin for channel 1. This pin controls the ATT function for preventing howling with the attenuators (ATT) provided on RIN and SOUT. When input is only on RIN, the SOUT attenuator is activated. When there is no input on RIN or there is input on both SIN and RIN, the RIN input attenuator is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. "H": Attenuator off "L": Attenuator on Because the attenuator is inserted opposite the speaker, it is effective for further reducing echo.
19	SOUT1	O	PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram). Data is always output on the rising edge of SCK. This pin is put in high impedance state while there is no data or during reset. In 2-channel parallel I/O mode, this pin becomes SOUT for channel 1 and outputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin outputs the SOUT signal as a multiplexed PCM signal of SOUT signal for channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin becomes high impedance.

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
20	SIN1	I	PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram). In 2-channel parallel I/O mode, this pin becomes SIN for channel 1 and inputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin sequentially inputs SIN as a multiplexed PCM signal from channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin becomes the cross-connected SIN pin for channel 1, and inputs the PCM signal synchronous with SYNC1. Data is captured on the falling edge of SCK.
22	ROUT1	O	PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram). Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data or during reset. In 2-channel parallel I/O mode, this pin becomes ROUT for channel 1 and outputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin outputs the ROUT signal as a multiplexed PCM signal of ROUT signals for channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin becomes the cross-connected ROUT pin for channel 1, and outputs the PCM signal synchronous with SYNC1.
23	RIN1	I	PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram). In 2-channel parallel I/O mode, this pin becomes RIN for channel 1 and inputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin sequentially inputs RIN as a multiplexed PCM signal from channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin is not used, and should be fixed at "L". Data is captured on the falling edge of SCK.

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th colspan="3">Description</th></tr>
<tr><td>24
25</td><td>SG11
SG10</td><td>I</td><td colspan="3">S output gain control pins for channel 1 (refer to the block diagram).
These pins amplify the output level of SOUT. The gain level can be set even during the echo canceler disable mode.</td></tr>
<tr><td></td><td></td><td></td><td>SG11</td><td>SG10</td><td>Gain Level</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>0 dB</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>+6 dB</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>+12 dB</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>Not used</td></tr>
<tr><td>26
27</td><td>SA11
SA10</td><td>I</td><td colspan="3">S input attenuator control pins for channel 1 (refer to the block diagram).
These pins attenuate the input level of SIN. Use them if ERL is large.
The attenuation level can be set even during the echo canceler disable mode.</td></tr>
<tr><td></td><td></td><td></td><td>SA11</td><td>SA10</td><td>Attenuation Level</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>0 dB</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>–6 dB</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>–12 dB</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>Not used</td></tr>
<tr><td>29
30</td><td>RGC11
RGC10</td><td>I</td><td colspan="3">R input level control pins for channel 1 (refer to the block diagram).
Excessive input (PCM level is at maximum value) causes a malfanction.
Use these pins when there is a possibility of excessive input.</td></tr>
<tr><td></td><td></td><td></td><td>RGC11</td><td>RGC10</td><td>Level Control Mode</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>Off</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>GC: On (control level = –20 dBm0)
By the R gain controller, levels from –20 to –11.5 dBm0 will be suppressed to –20 dBm0 and those above –11.5 dBm0 will always be attenuated by 8.5 dB. This is effective to prevent excessive input and howling for hands-free applications.</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>Inhibited</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>±6LR: On
Applies –6 dB to excessive inputs using the level adjuster provided on R and S I/O. Since +6 dB also is applied at the output, the total level will not change, making this effective against line echo.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>31</td><td>DF1</td><td>O</td><td>Tone disabler flag output pin for channel 1.
This pin outputs a disable flag when the ECDM pins are used for tone disabler mode.
"H": Echo canceler disabled
"L": Echo canceler enabled</td></tr>
<tr><td>32</td><td>WDT1</td><td>O</td><td>Not used. Leave this pin open.</td></tr>
<tr><td>38</td><td>SYNCO</td><td>O</td><td>Output pin for internal SYNC signal (8 kHz).
This pin is used as the transmit/receive synchronization signal for PCM signals. Connect it to the SYNC pin and PCM CODEC's synchronization signal pin. Leave this pin open if using an external SYNC.</td></tr>
<tr><td>39</td><td>SCKO</td><td>O</td><td>Output pin for internal SCK signal (256 kHz).
This pin is used for the transfer clock of PCM signals. Connect it to the PCM CODEC's synchronization signal pin. Leave open if using an external SYNC.</td></tr>
<tr><td>40
41</td><td>ECDM0
ECDM1</td><td>I</td><td>Tone disabler control pin common to channel 1 and channel 2.
These pins detect answer tones generated by modems (2100 Hz), and then disable the echo canceler.
<table>
<tr><th>ECDM1</th><th>ECDM0</th><th>Tone Disabler Mode</th></tr>
<tr><td>0</td><td>0</td><td>Off</td></tr>
<tr><td>0</td><td>1</td><td>2100 Hz tone detection: On</td></tr>
<tr><td>1</td><td>0</td><td>2100 Hz and phase reversal detection: On</td></tr>
<tr><td>1</td><td>1</td><td>Inhibited</td></tr>
</table></td></tr>
<tr><td>42</td><td>$\overline{\text{PWDWN}}$</td><td>I</td><td>Common pin for channel 1 and channel 2.
This pin controls the power-down mode to reduce current consumption when the device is not being used.
"L": Power down
"H": Normal operation
During power-down mode all input pins are invalid, and output pins will enter the following states.
Hi-Z: SOUT1, SOUT2, ROUT1, ROUT2
"L": SYNCO, SCKO
Previous state: DF1, WDT1, DF2, WDT2
Reset the device after power-down mode is released.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th colspan="3">Description</th></tr>
<tr><td>43</td><td>TST</td><td>O</td><td colspan="3">Not used. Leave this pin open.</td></tr>
<tr><td>46</td><td>CLKIN</td><td>I</td><td colspan="3">Basic clock input pin.
Input a clock 18 to 20 MHz. Use 19.2 MHz if using internal synchronization signals (SYNCO, SCKO).</td></tr>
<tr><td>47</td><td>V_{DD}
(PLL)</td><td>I</td><td colspan="3">Power supply for PLL circuit that uses the basic clock.
Insert a 0.1μF capacitor with excellent high frequency characteristics between V_{DD} (PLL) and V_{SS} (PLL).</td></tr>
<tr><td>48</td><td>V_{SS}
(PLL)</td><td>I</td><td colspan="3">Ground for PLL circuit that uses the basic clock.
Insert a 0.1μF capacitor with excellent high frequency characteristics between V_{DD} (PLL) and V_{SS} (PLL).</td></tr>
<tr><td>49</td><td>WDT2</td><td>O</td><td colspan="3">Not used. Leave this pin open.</td></tr>
<tr><td>50</td><td>DF2</td><td>O</td><td colspan="3">Tone disabler flag output pin for channel 2.
This pin outputs a disable flag when the ECDM pins are used for tone disabler.
"H": Echo canceler disabled
"L": Echo canceler enabled</td></tr>
<tr><td rowspan="6">51
52</td><td rowspan="6">RGC20
RGC21</td><td rowspan="6">I</td><td colspan="3">R input level control pins for channel 2 (refer to the block diagram).
Excessive input (PCM level is at maximum value) causes a malfunction.
Use these pins when there is a possibility of excessive input.</td></tr>
<tr><td>RGC21</td><td>RGC20</td><td>Level Control Mode</td></tr>
<tr><td>0</td><td>0</td><td>Off</td></tr>
<tr><td>0</td><td>1</td><td>GC: On (control level = –20 dBm0)
By the R gain controller, levels from –20 to –11.5 dBm0 will be suppressed to –20 dBm0 and those above –11.5 dBm0 will always be attenuated by 8.5 dB. This is effective to prevent excessive input and howling for hands-free applications.</td></tr>
<tr><td>1</td><td>0</td><td>Inhibited</td></tr>
<tr><td>1</td><td>1</td><td>±6LR: On
Apply –6 dB to excessive inputs using the level adjuster provided on R and S I/O. Since +6 dB also is applied at the output, the total level will not change, making this effective against line echo.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>54
55</td><td>SA20
SA21</td><td>I</td><td>S input attenuator control pins for channel 2 (refer to the block diagram).
These pins attenuate the input level of SIN. Use them if ERL is large.
The attenuation level can be set even during the echo canceler disable mode.
<table>
<tr><td>SA21</td><td>SG20</td><td>Attenuation Level</td></tr>
<tr><td>0</td><td>0</td><td>0 dB</td></tr>
<tr><td>0</td><td>1</td><td>–6 dB</td></tr>
<tr><td>1</td><td>0</td><td>–12 dB</td></tr>
<tr><td>1</td><td>1</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>56
57</td><td>SG20
SG21</td><td>I</td><td>S output gain control pins for channel 2 (refer to the block diagram).
These pins amplify the output level of SOUT. The gain level can be set even during the echo canceler disable mode.
<table>
<tr><td>SG21</td><td>SG20</td><td>Gain Level</td></tr>
<tr><td>0</td><td>0</td><td>0 dB</td></tr>
<tr><td>0</td><td>1</td><td>+6 dB</td></tr>
<tr><td>1</td><td>0</td><td>+12 dB</td></tr>
<tr><td>1</td><td>1</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>58</td><td>RIN2</td><td>I</td><td>PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram).
In 2-channel parallel I/O mode, this pin becomes RIN for channel 2 and inputs the PCM signal synchronous with SYNC2. Data is captured on the falling edge of SCK. In other modes, this pin is not used, and should be fixed at "L".</td></tr>
<tr><td>59</td><td>ROUT2</td><td>O</td><td>PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram).
Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data.
In 2-channel parallel I/O mode, this pin becomes ROUT for channel 2 and outputs the PCM signal synchronous with SYNC2. In 2-channel serial I/O mode, this pin is not used and should be left open. In 1-channel cross-connected mode, this pin becomes the cross-connected ROUT pin for channel 2, and outputs the PCM signal synchronous with SYNC1.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
61	SIN2	I	PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram). Data is captured on the falling edge of SCK. In 2-channel parallel I/O mode, this pin becomes SIN for channel 2 and inputs the PCM signal synchronous with SYNC2. In 2-channel serial I/O mode, this pin is not used and should be fixed at "L". In 1-channel cross-connected mode, this pin becomes the cross-connected SIN pin for channel 2, and inputs the PCM signal synchronous with SYNC1.
62	SOUT2	O	PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram). Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data. In 2-channel parallel I/O mode, this pin becomes SOUT for channel 2 and outputs the PCM signal synchronous with SYNC2. In other modes, this pin is not used and should be left open.
63	ATT2	I	ATT control pin for channel 2. This pin controls the ATT function for preventing howling with the attenuators (ATT) provided on RIN and SOUT. When input is only on RIN, the SOUT attenuator is activated. When there is no input on SIN or there is input on both SIN and RIN, the RIN input attenuator is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. "H": Attenuator off "L": Attenuator on Because the attenuator is activated opposite the speaker, it is effective for further reducing echo.
64	HD2	I	Howling detection control pin for channel 2. This pin controls detection and canceling of howling generated by the acoustics of handsfree telephones. "L": Howling detector on "H": Howling detector off

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to + 7	V
Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D		1	W
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.5	5	5.5	V
Power Supply Voltage	V_{SS}	—	—	0	—	V
High Level Input Voltage	V_{IH}	—	2.4	—	V_{DD}	V
Low Level Input Voltage	V_{IL}	—	0	—	0.8	V
Operating Temperature	Ta	—	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Output Voltage	V_{OH}	I_{OH} = 40 µA	4.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA	0	—	0.4	V
High Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.1	10	µA
Low Level Input Current	I_{IL}	$V_{IL} = V_{SS}$	–10	–0.1	—	µA
High Level Output Leakage Current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.1	10	µA
Low Level Output Leakage Current	I_{OZL}	$V_{OL} = V_{SS}$	–10	–0.1	—	µA
Power Supply Current (operation mode)	I_{DDO}	—	—	80	130	mA
Power Supply Current (power-down mode)	I_{DDS}	$\overline{PWDWN}$ = "L"	—	0.5	2	mA
Input Capacitance	C_I	—	—	—	15	pF
Output Load Capacitance	C_{LOAD}	—	—	—	20	pF

Echo Canceler Characteristics (refer to characteristics diagram)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Reduction (Common to Channel 1 and Channel 2)	L_{RES}	R_{IN} = –10 dBm0 (5 kHz white noise band) E. R. L. = 6 dB T_D = 50 ms ATT, GC, NLP: OFF	—	30	—	dB
Cancelable Echo Delay Time (Common to Channel 1 and Channel 2)	T_D	R_{IN} = –10 dBm0 (5 kHz white noise band) E. R. L. = 6 dB ATT, GC, NLP: OFF	—	—	55	ms

Tone Disabler Characteristics

Parameter		Min.	Typ.	Max.	Unit
Tone Detection	Detection frequency	2075	2100	2125	Hz
	Detection level	–32	—	—	dBm0
	Detection time	380	—	—	ms
Phase Reversal Detection	Detection condition	2100Hz. 180° out-of-phase detected before and after 450±25ms.			
	Detection frequency	2075	2100	2125	Hz
	Detection level	–32	—	—	dBm0
	Phase reversal	135	180	225	°
Release	Detection level	—	—	–32	dBm0
	Release time	—	250	—	ms

AC Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	f_C	—	19.2	—	MHz
If Used Without Internal Sync Signal		18	—	20	
Clock Cycle Time	t_{MCK}	—	52.08	—	ns
If Used Without Internal Sync Signal		50	—	55.56	
Clock Duty Cycle	t_{DMC}	40	—	60	%
Clock High Level Pulse Width	t_{MCH}	$t_{MCK} \times 0.4$	—	$t_{MCK} \times 0.6$	ns
Clock Low Level Pulse Width	t_{MCL}	$t_{MCK} \times 0.4$	—	$t_{MCK} \times 0.6$	ns
Clock Rise Time	t_r	—	—	5	ns
Clock Fall Time	t_f	—	—	5	ns
Internal Sync Clock Output Time	t_{DCM}	—	—	40	ns
Internal Sync Clock Frequency	f_{CO}	—	256	—	kHz
Internal Sync Clock Cycle Time	t_{CO}	—	3.9	—	µs
Internal Sync Clock Duty Cycle	t_{DCO}	—	50	—	%
Internal Sync Signal Output Time	t_{DCC}	—	—	5	ns
Internal Sync Signal Period	t_{CYO}	—	125	—	µs
Internal Sync Signal Pulse Width	t_{WSO}	—	t_{CO}	—	µs
Transmit/Receive Sync Clock Frequency	f_{SCK}	64	—	2048	kHz
In Serial I/O Mode		128	—	2048	
Transmit/Receive Sync Clock Cycle Time	t_{SCK}	0.488	—	15.62	µs
In Serial I/O Mode		0.488	—	7.81	
Transmit/Receive Sync Clock Duty Cycle	t_{DSC}	40	50	60	%
Transmit/Receive Sync Signal Period	t_{CYC}	—	125	—	µs
Sync Timing	t_{XS}	45	—	—	ns
	t_{SX}	45	—	—	ns
Sync Signal Width	t_{WSY}	t_{SCK}	—	$t_{CYC}–t_{SCK}$	µs
Receive Signal Setup Time	t_{DS}	45	—	—	ns
Receive Signal Hold Time	t_{DH}	45	—	—	ns
Receive Signal Input Time	t_{ID}	—	$7t_{SCK}$	—	µs
In 2-Channel Serial Mode	t_{ID2}	—	$15t_{SCK}$	—	µs

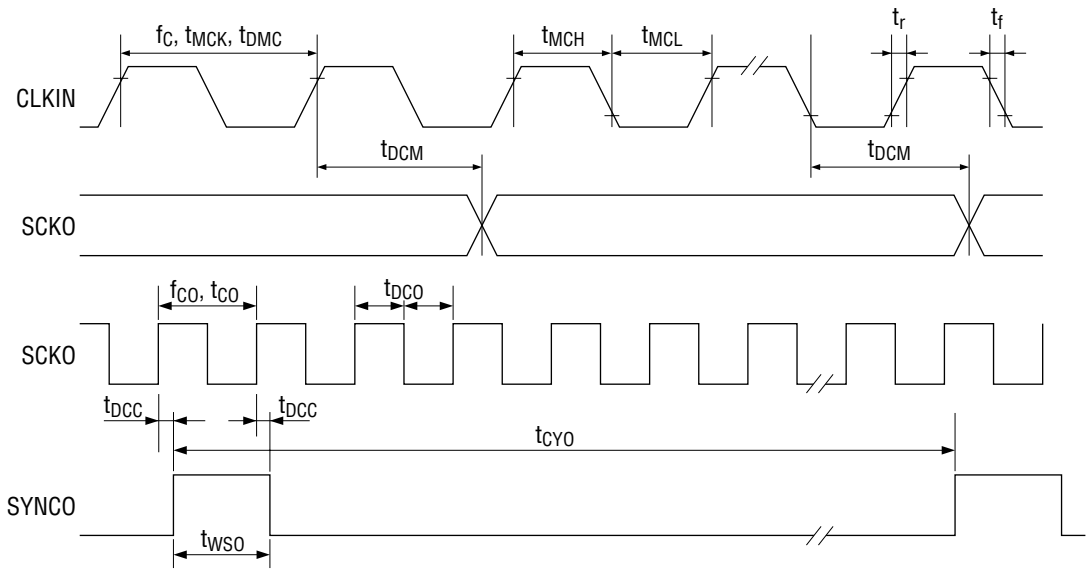
AC Characteristics (Continued)

(V_{DD} = 4.5 V to 5.5 V, Ta = –40°C to +85°C)

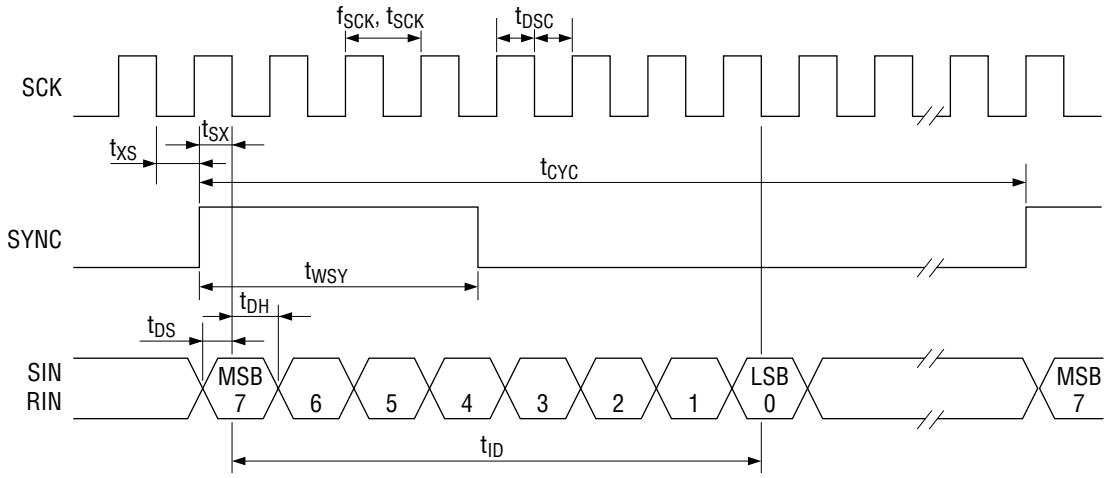
Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial Output Delay Time	t_{SD}	—	—	90	ns
	t_{XD}	—	—	90	ns
Reset Signal Input Width	t_{WR}	1	—	—	µs
Reset Start Time	t_{DRS}	5	—	—	ns
Reset End Time	t_{DRE}	—	—	52	ns
Process Operation Start Time	t_{DIT}	100	—	—	µs
Power-Down Start Time	t_{DPS}	—	—	111	ns
Power-Down End Time	t_{DPE}	—	—	15	ns
RST Width After Power-Down	t_{WPR}	10	—	—	µs
$\overline{RST}$ Control Pin Setup Time	t_{DSR}	20	—	—	ns
$\overline{RST}$ Control Pin Hold Time	t_{DHR}	20	—	—	ns
SCK Control Pin Setup Time	t_{DCS}	120	—	—	ns
SCK Control Pin Hold Time	t_{DCH}	120	—	—	ns

TIMING DIAGRAMS

Clock Timing

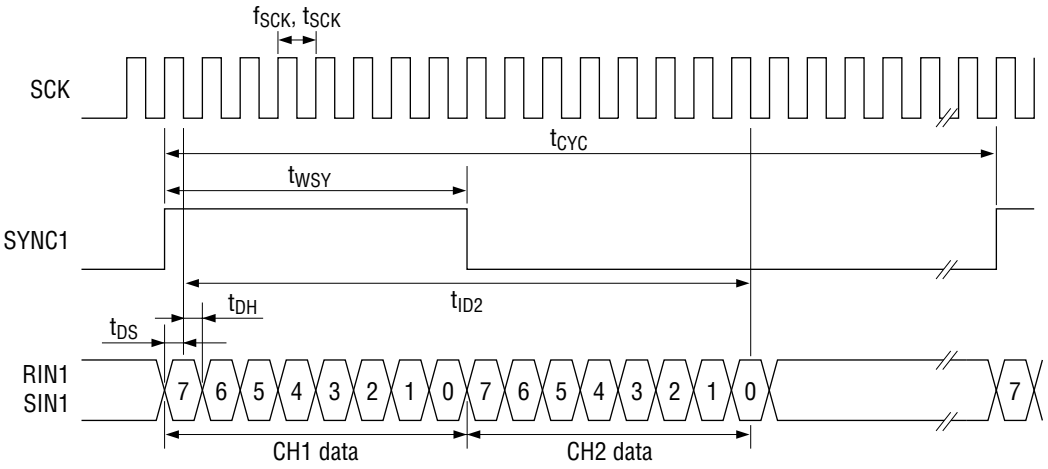


Serial Data Input Timing (Parallel Mode, FTF Mode)

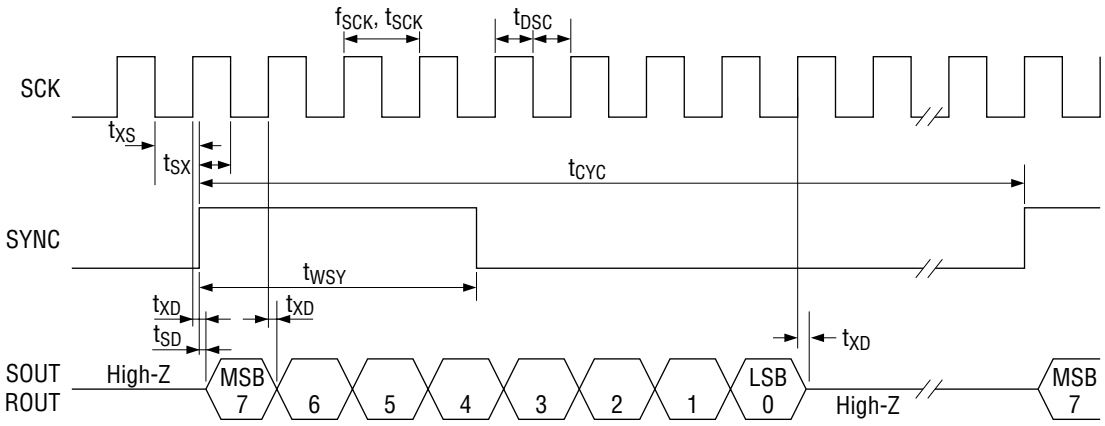


Serial Data Input Timing (Serial Mode)

Note: Refer to parallel mode for detailed timing

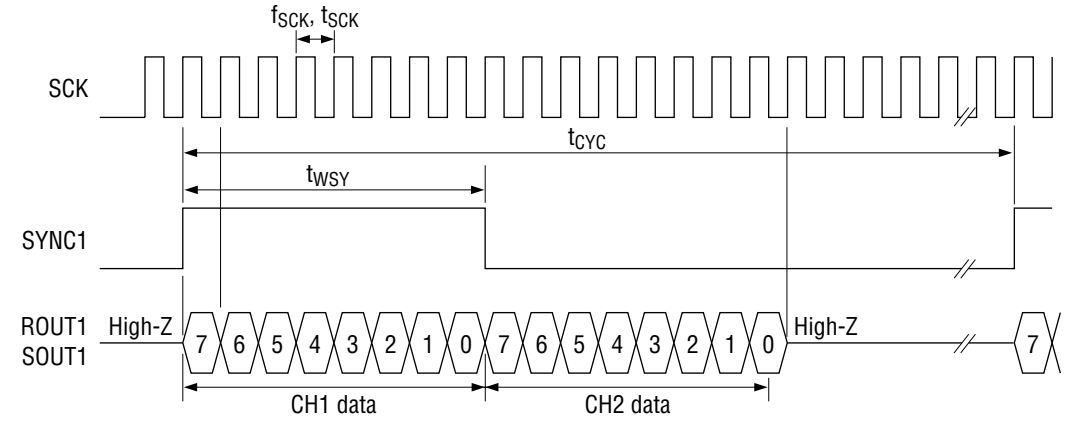


Serial Data Output Timing (Parallel Mode, FTF Mode)

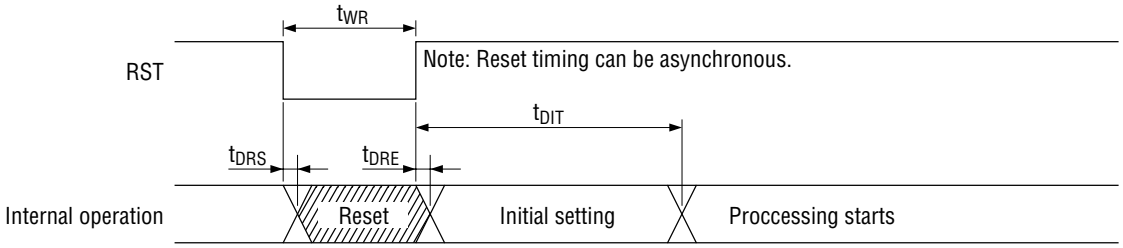


Serial Data Output Timing (Serial Mode)

Note: Refer to parallel mode for detailed timing

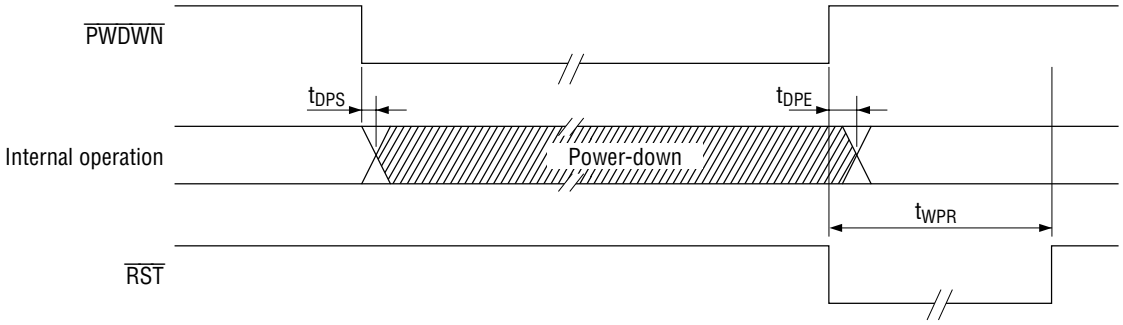


Operation Timing After Reset



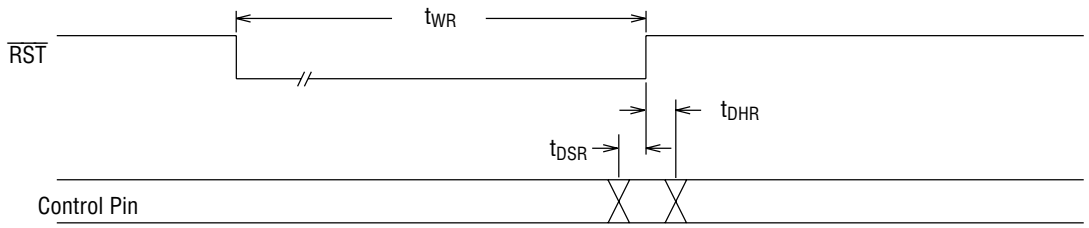
Power-Down Timing

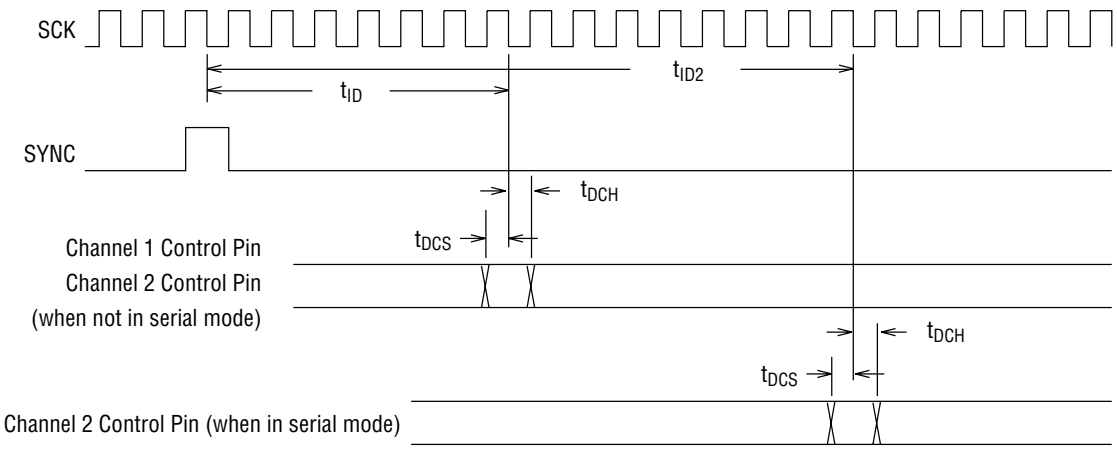
Note: All inputs are invalid during power-down. Always reset the device after power-down.



Capture Timing of Control Pins

Control pin states are captured during reset and during each period's serial data capture.



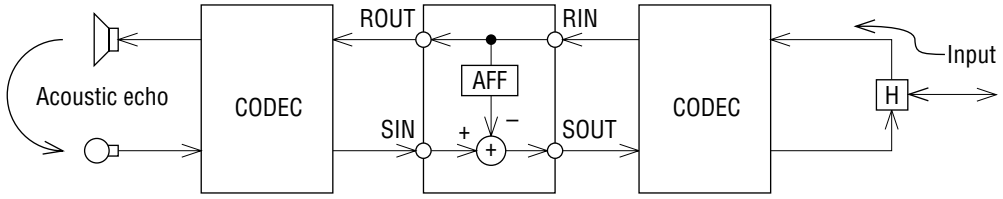


HOW TO USE THE MSM7617

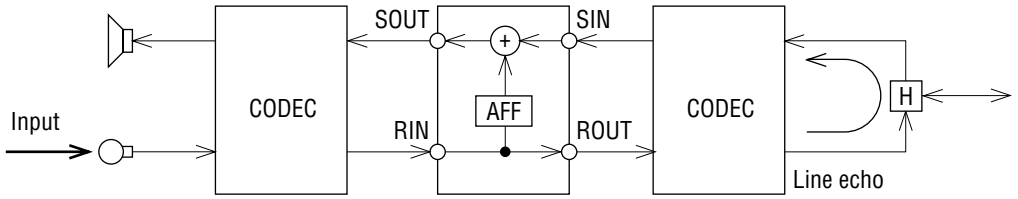
The echo canceler cancels the echo on the RIN signal as returned by SIN. Connect the original signal to the R side, and the signal generating the echo to the S side.

Connection Methods According to Echoes

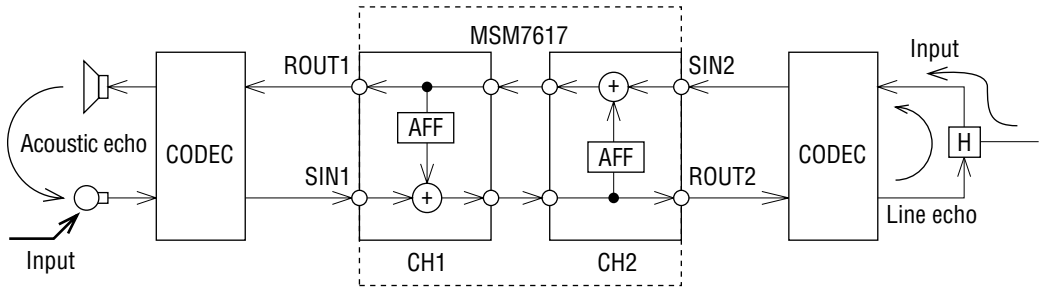
Example 1. Cancel Acoustic Echo (applies to acoustic echo from line input)



Example 2. Cancel Line Echo (applies to line echo from microphone input)

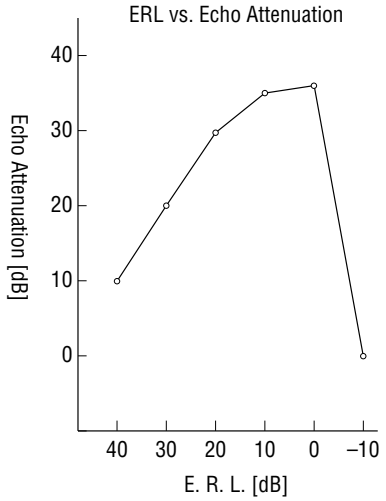


Example 3. Cancel Both Acoustic Echo And Line Echo

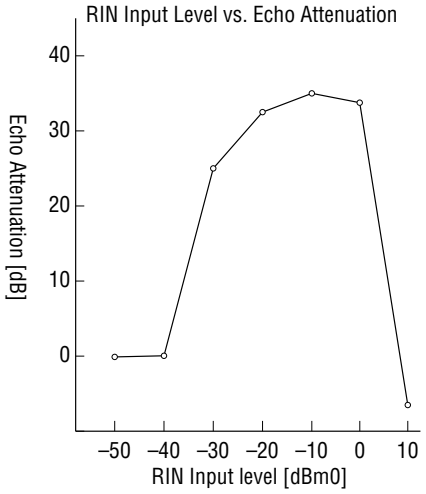


ECHO CANCELER CHARACTERISTICS DIAGRAM

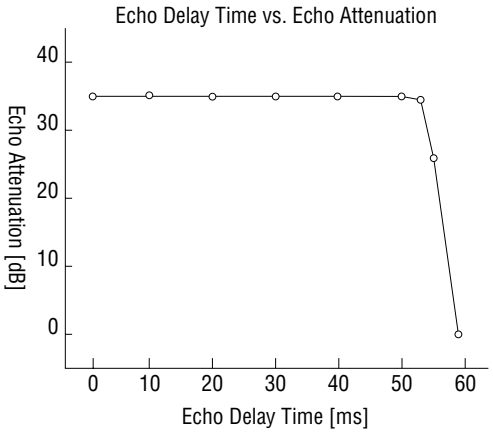
Characteristics of μ-law and A-law are identical. (Characteristic graphs below are reference data.)



Measuring Conditions:
RIN input level = –10 dBm0 white noise
Echo delay time = 50 ms
ATT, GC, NLP, LR all off



Measuring Conditions:
RIN input = white noise
Echo delay time = 50 ms
E.R.L. = 6 [dB]
ATT, GC, NLP, LR all off



Measuring Conditions:
RIN input level = –10 dBm0 white noise
Echo delay time = 50 ms
E.R.L = 6 dB
ATT, GC, NLP, LR all off

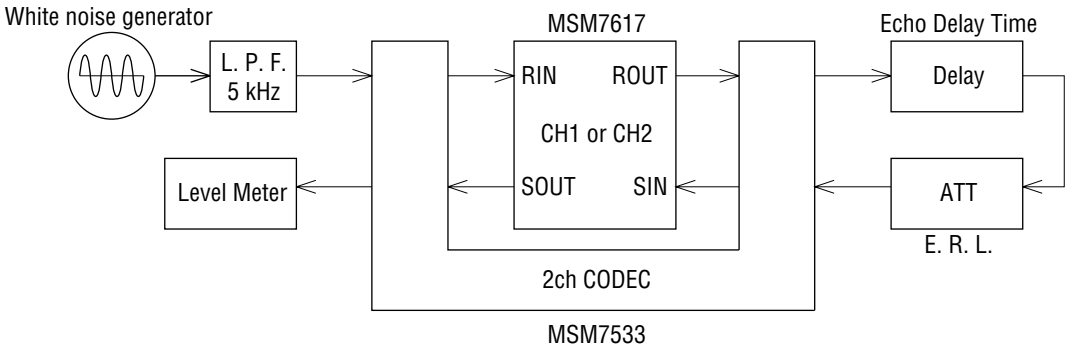
Note: regarding dBm0:

The "dBm0" unit used in the characteristic graphs is a unit that expresses PCM CODEC digital values. Therefore, be aware that the same value 0 [dBm0] might correspond to different analog input levels depending on the PCM CODEC being used. Please check the data sheet of the PCM CODEC being used.

Example MSM7533 0 [dBm0] = 0.85 [Vrms] = 2.4 [Vp-p] = 0.8 [dBm] 600 Ω
–10 [dBm0] = 0.27 [Vrms] = 0.76 [Vp-p] = –9.2 [dBm] 600 Ω

MSM7543 0 [dBm0] = 0.6007 [Vrms] = 1.7 [Vp-p] = –2.2 [dBm] 600 Ω
–10 [dBm0] = 0.19 [Vrms] = 0.54 [Vp-p] = –12.2 [dBm] 600 Ω

Measurement System Block Diagram



NOTES ON USE

1. Set echo return loss (E. R. L) to be attenuated. If the echo return loss is set to be amplified, the echo cannot be canceled. (Refer to the "E. R. L vs Echo Attenuation" characteristic graph.)

   When the echo return loss is amplified, adjust the input level to be attenuated by setting the mode with the SA pin. If the level from the SA pin is too low by setting the mode with the SA pin, then amplify the output level by setting the mode with the SG pin.

2. Set RIN input so that there is not excessive input (above 0 dBm0) from the PCM CODEC. Echo cancellation is not possible with excessive input. (Refer to the "RIN vs Echo Attenuation" characteristic graph.)

   Recommended input levels are –10 to –20 dBm0. If there is a possibility of excessive input, then set GC mode or 6LR mode with the RGC pins.

3. Applying the tone signals to this echo canceler will decrease echo attenuation.

4. For changes in the echo path (retransmit, circuit switching during transmission, and so on), convergence may be difficult.
   Perform a reset to make it converge.
   If the state of the echo path changes after a reset, convergence may again be difficult.
   In cases such as a change in the echo path, perform a reset each time.

5. If a clock is not input after power is applied, then the internal circuits will not stabilize, possibly damaging the device.

   When power is applied, set the $\overline{\text{PWDWN}}$ pin to "H" and input the basic clock.

   If the device is put into $\overline{\text{PWDWN}}$ immediately after power has been applied, be sure to input 10 or more clocks of the basic clock before setting to the power down mode.

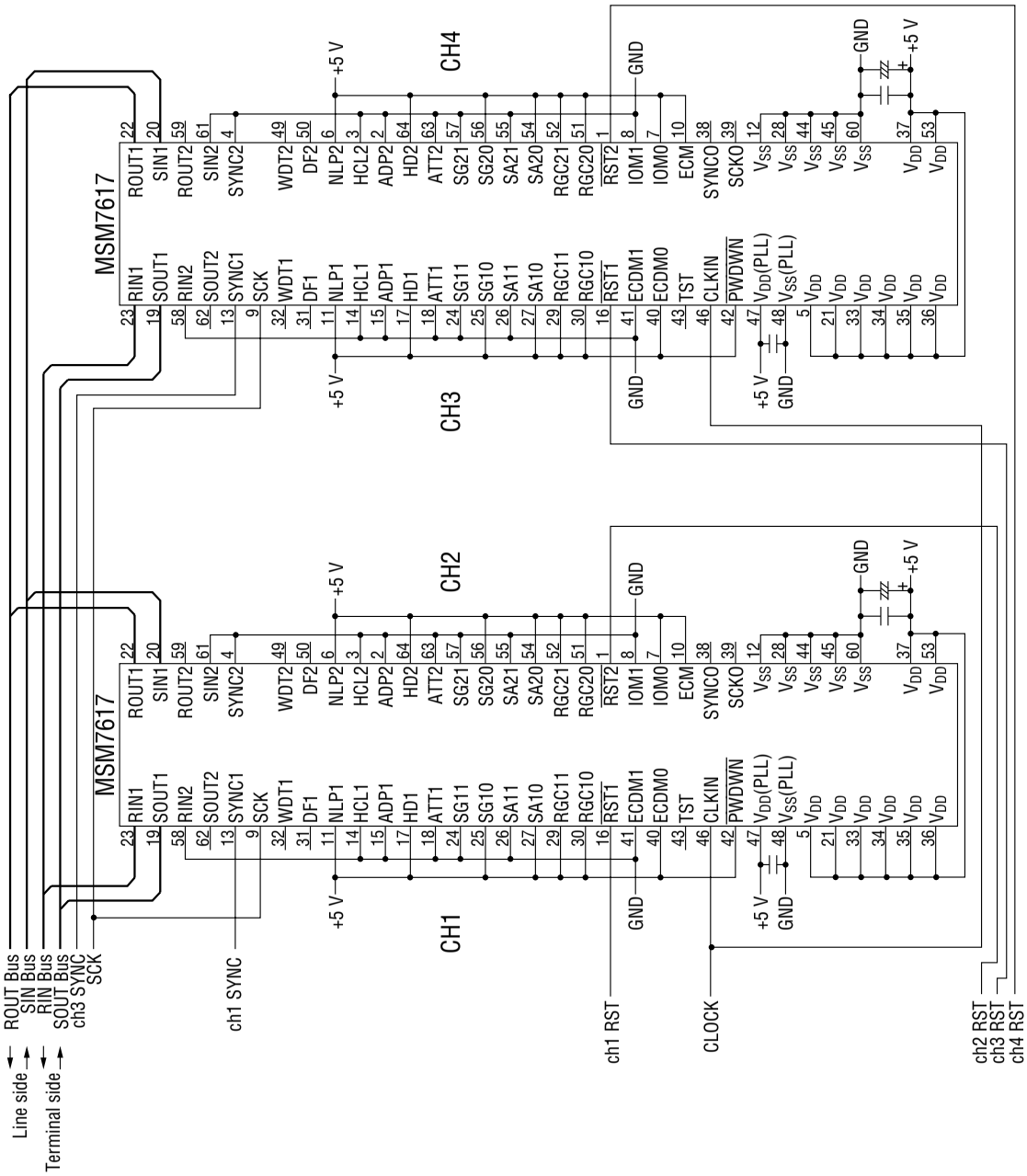
6. Always reset after power is applied or power-down is released.
   For power-on reset operation, an external oscillator may require a certain setting time after powered on. Allow 10 µs for a reset time after the oscillator has settled.

7. When the device is used as an acoustic echo canceler, equipment noise and environment noise from the microphone amp may be amplified, and echo attenuation may be below 30 dB.

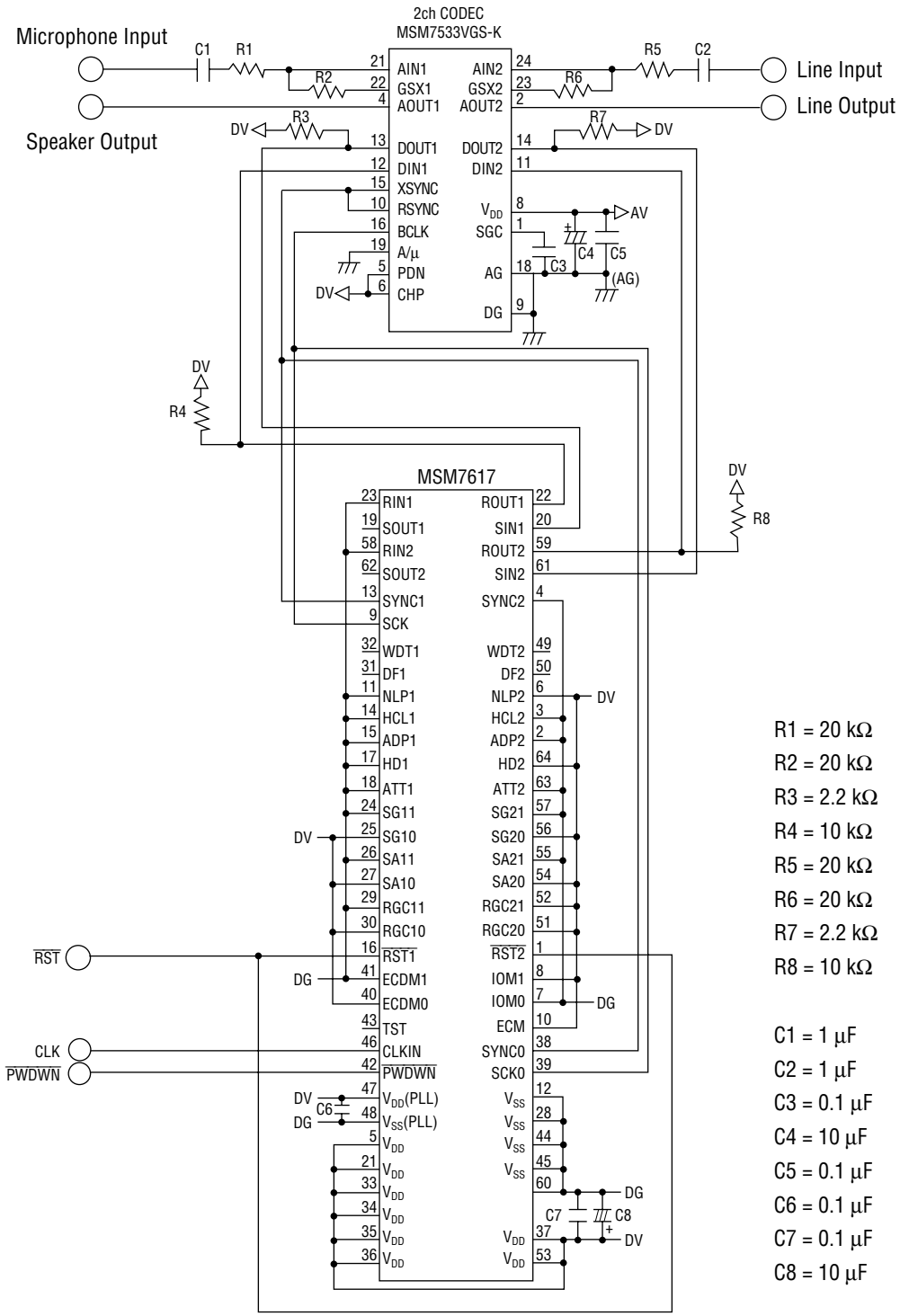
APPLICATION CIRCUITS

4-Channel Serial Interface

Line Echo Canceler Example



Cross-Connection Example



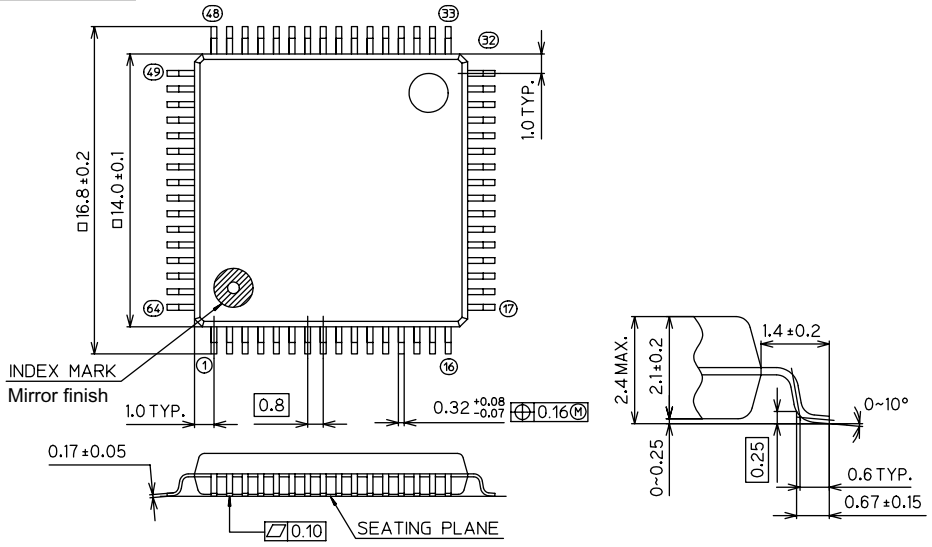
R1 = 20 kΩ
R2 = 20 kΩ
R3 = 2.2 kΩ
R4 = 10 kΩ
R5 = 20 kΩ
R6 = 20 kΩ
R7 = 2.2 kΩ
R8 = 10 kΩ

C1 = 1 μF
C2 = 1 μF
C3 = 0.1 μF
C4 = 10 μF
C5 = 0.1 μF
C6 = 0.1 μF
C7 = 0.1 μF
C8 = 10 μF

PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.87 TYP.
Rev. No./Last Revised	6/Feb. 23, 2001

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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