OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM6981-01

32 kbps ADPCM TRANSCODER

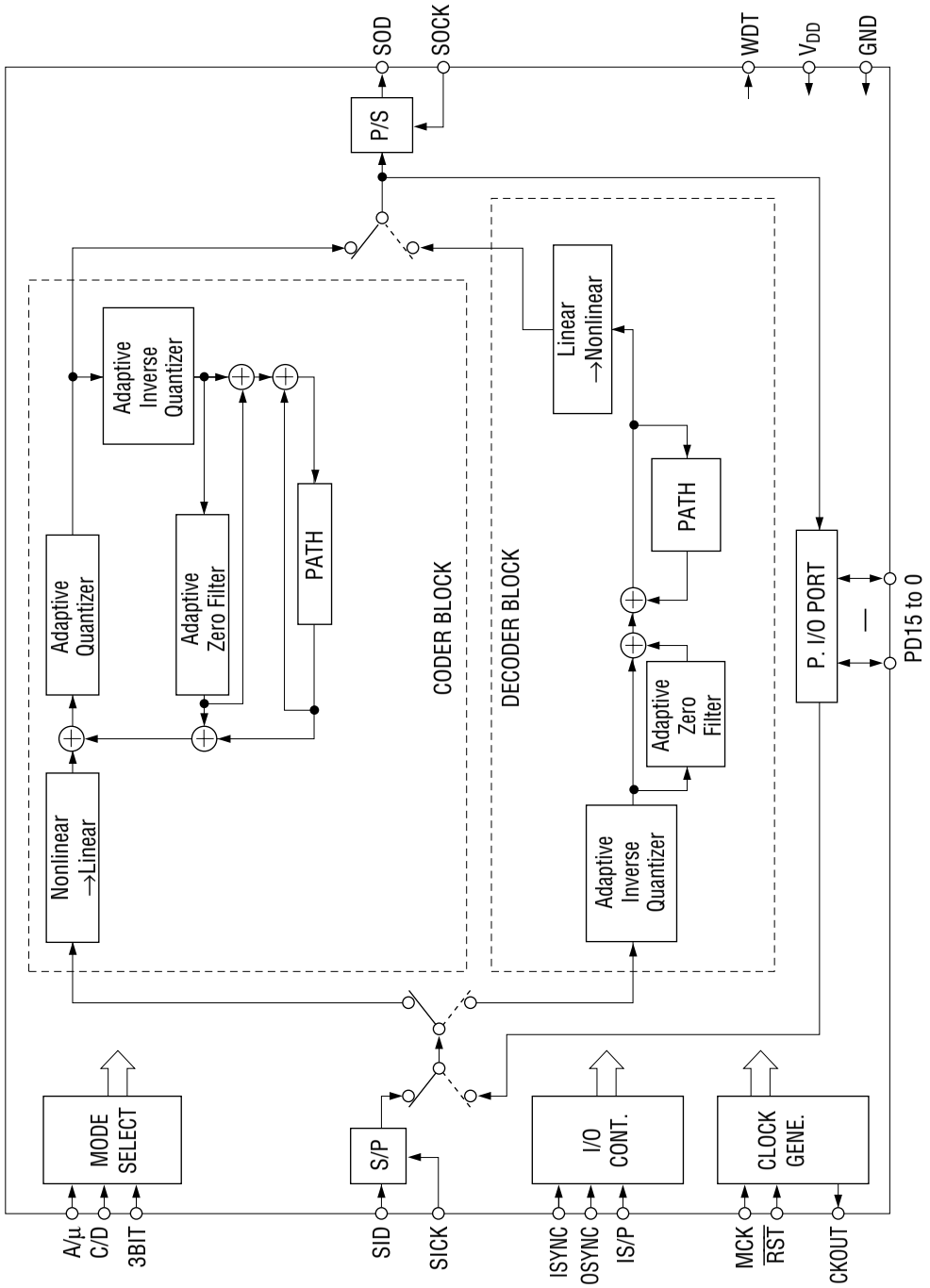
GENERAL DESCRIPTION

The MSM6981-01 is for performing high-efficiency compression to code an A/D converted audio-band PCM signal into an ADPCM signal with a transmission rate of 32 kbps, or conversely for converting an ADPCM signal to a PCM signal.
With digital-digital conversion in particular, if this device is used as a PCM-ADPCM mutual converter (transcoder) between existing PCMs and CODECs, efficiency can be doubled with respect to conventional transmission lines without loss of call quality.
This device may be used in high-speed digital dedicated line multiplexors, digital circuit multiplexors and digital PBX's, or in audio band signal coders/decoders for this kind of equipment.
The MSM6981-01 cannot transfer data to and from the MSM6980-03 (MSM6980 family).

FEATURES

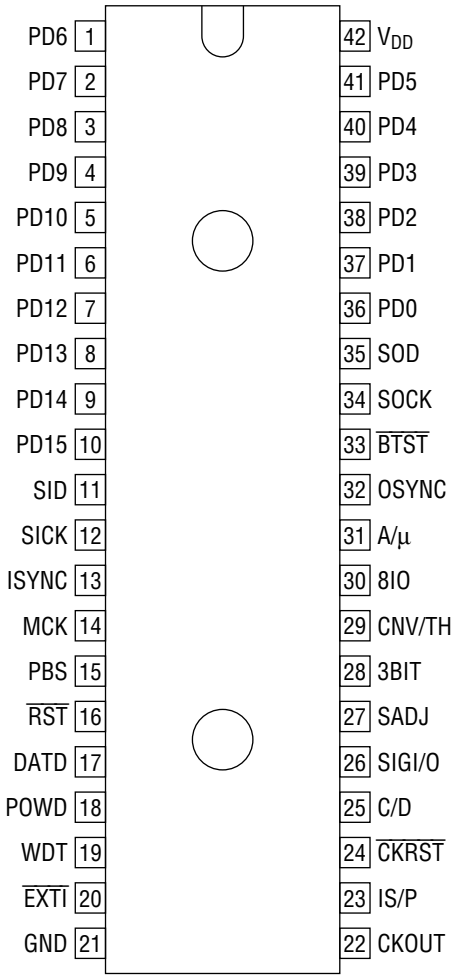
- Provides 9600 bps modem signal (conformed with ITU-T V.29) transmission capability
- High quality transmission characteristics equal to or better than ITU-T G.721 (ADPCM specification) for voice signals and tone signals
- Provides 24 kbps ADPCM transmission capability for voice signals
- Can be interfaced with μ-law or A-law PCM CODECs
- Can operate as ADPCM encoder or decoder (selection of operation mode)
- Asynchronous data input and output
- Serial or parallel data interface
- Usable clock rate of 32 kbps to 2048 kbps for serial input or output
- Selectable 3 bit or 4 bit data conversion
- Low power consumption: +5 V, 70 mW (Typ.)
- Package:
  42-pin plastic DIP (DIP42-P-600-2.54) (Product name : MSM6981-01RS)

BLOCK DIAGRAM



PATH: Prediction filter controlled by Advanced Tchebycheff equation and Hurwitz stability

PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

PIN DESCRIPTION

Pin	Symbol	Description
1 to 10 36 to 41	PD0 to PD15	Bidirectional bus interface. PD15 is the MSB pin. Refer to Tables 1 and 2 for the specifications and Figures 1 and 3 for the timings. When $\overline{RST}$ or OSYNC is a logic "0", all of outputs PD0 to PD15 are "1"s with an impedance of 100 kΩ or more. A logic "0" means low level input/output voltage and a logic "1" high level input/output voltage.
11	SID	Serial data input. The bit length is 4 or 8. Refer to Fig.2.
12	SICK	Clock signal input for serial input data. The maximum clock rate is 2048 kbps. The input clock count should be longer than the serial data bit length. Refter to Fig.2.
13	ISYNC	Synchronous pulse signal input. For taking in the serial or parallel data.
14	MCK	Main clock input. 20 MHz clock input.
15	PBS	Chip test input. Input a logic "0" to this pin.
16	$\overline{RST}$	Reset signal input. Input a logic "0" while the main clock (MCK) is input. Provide the timing indicated in Fig.6 to make the first output data effective. While a logic "0" is input to $\overline{RST}$, PD0 to PD15 output a logic "1" with a high output impedance of 100 kΩ or more, and SOD is in a high impedance state.
17	DATD	Chip test output.
18	POWD	Chip test output.
19	WDT	Chip test output. Also available for the internal observation signal. When the device is operating normally, the signal synchronized with ISYNC is output from WDT. Refter to Fig.5.
20	$\overline{EXTI}$	Chip test input. Normally input a logic "1" to this pin.
21	GND	Ground. 0 V.
22	CKOUT	Chip test output. Normally 1/4 main clock (MCK) frequency is output (5 MHz).
23	IS/P	Serial/Parallel data input select signal. Logic "1": Serial data input. Logic "0": Parallel data input. Refer to Table 1.
24	$\overline{CKRST}$	Chip test input. Normally pull this pin to a logic "1".
25	C/D	Operating mode select input. Logic "1": Coding mode. Logic "0": Decoding mode. Refer to Table 1.

Pin	Symbol	Description
26	SIGI/O	Chip test input and output. Normally remain this pin open.
27	SADJ	Chip test input. Normally pull this pin to a logic "0".
28	3BIT	ADPCM data bit length select signal. Logic "1": 3 bits Logic "0": 4 bits Refer to Table 2.
29	CNV/TH	Chip test input. Normally pull this pin to either a logic "1" or "0".
30	8IO	Chip test input. Normally pull this pin to a logic "0".
31	A/μ	PCM coding law select input. Logic "1": A-law Logic "0": μ-law
32	OSYNC	Parallel or serial output control. Refer to Fig.3 and Fig.4.
33	$\overline{\text{BTST}}$	Chip test input. Pull this pin to a logic "1".
34	SOCK	Clock input for serial data output control. The maximum output data rate is 2048 kbps. Refer to Fig.4.
35	SOD	Serial data output. The data bit length is 4 or 8. After the determined number of bits has been sent from SOD, SOD is in a high impedance state. The fourth bit is a logic "0" when the bit length is three. Refer to Fig.4.
42	V_{DD}	+5 V power supply.

Input/Output Setting Table

Table-1

Operating Mode	Input		Output		Control Pin	
	Bit Length	P/S	Bit Length	P/S	C/D	IS/P
Coder	8	P	4 (3)	Note: P, S	1	0
		S				1
Decoder	4 (3)	P	8	Note: P, S	0	0
		S				1

P: Parallel format
S: Serial format

Note: Output in serial or Parallel

Table to Indicate the Parallel I/O Pins

Table-2

I/O	Input			Output		
	Coder	Decoder		Coder		Decoder
		4-bit	3-bit	4-bit	3-bit	
PD15 to 12				MSB … LSB	MSB … LSB	MSB …
PD11 to 8						… LSB
PD7 to 4	MSB …					
PD3 to 0	… LSB	MSB … LSB	MSB … LSB			

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	
Power Dissipation	P_D		1	W
Storage Temperature	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature	Ta	—	0	25	70	°C
Power Supply Voltage	V_{DD}	—	4.75	5	5.25	V
Master Clock Frequency	F_C	—	19.998	20	25	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics (In range of Recommended Operating Condition)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Stand-by Power Supply Current	I_{DD1}	Master clock is not input	—	1.0	2.0	mA
Operating Power Supply Current	I_{DD2}	F_C = 20 MHz	—	14	20	mA
Input Low Voltage	V_{IL}	—	0	—	0.8	V
Input High Voltage	V_{IH1}	MCK, SICK, SOCK	2.4	—	V_{DD}	V
	V_{IH2}	Other input pins	2.0	—	V_{DD}	
Output Low Voltage	V_{OL1}	SOD, I_{OL} = 6.0 mA	0	—	0.4	V
	V_{OL2}	Other output pins, I_{OL} = 1.6 mA	0	—	0.4	
Outpu High Voltage	V_{OH}	I_{OH} = 40 µA	4.2	—	V_{DD}	V
Input Leakage Current	I_I	V_{IN} = V_{DD}, GND	–10	—	+10	µA
Input Capacitance	C_I	—	—	—	10	pF
Output Load Capacitance	C_L	—	—	—	100	pF

TIMING DIAGRAM

Parallel Data Input

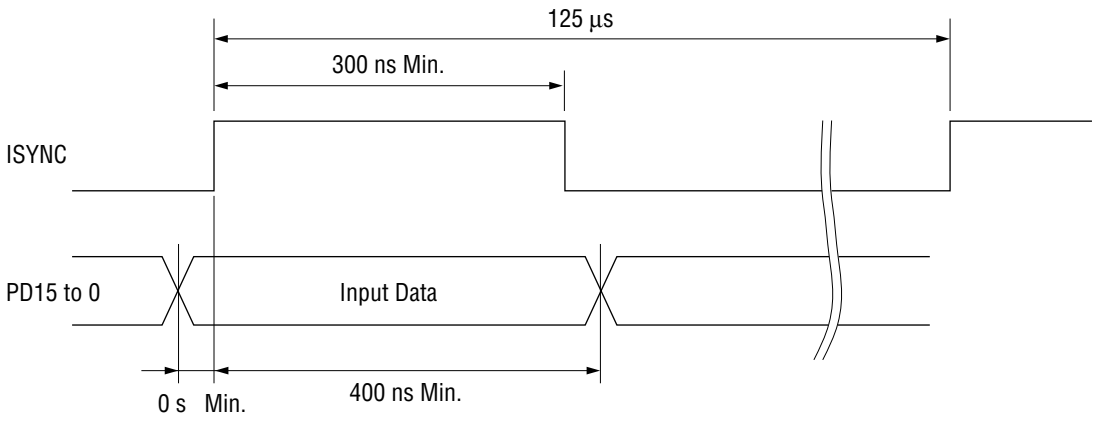
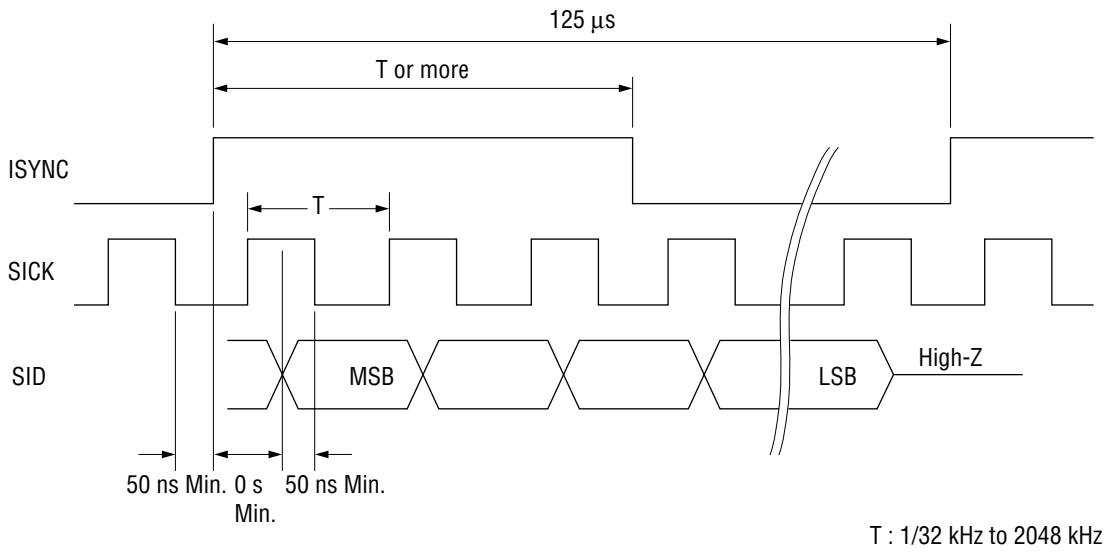


Figure 1

Serial Data Input



T : 1/32 kHz to 2048 kHz

Figure 2

Parallel Data Output

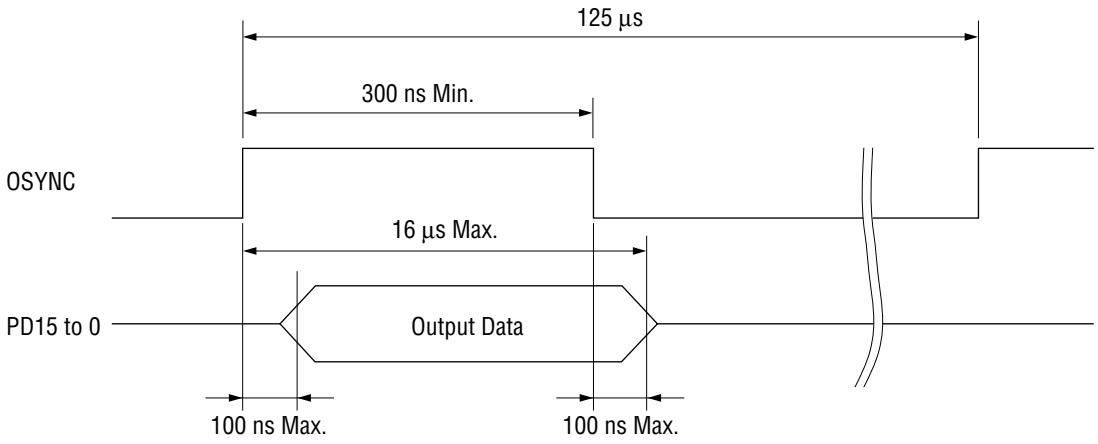


Figure 3

Serial Data Output

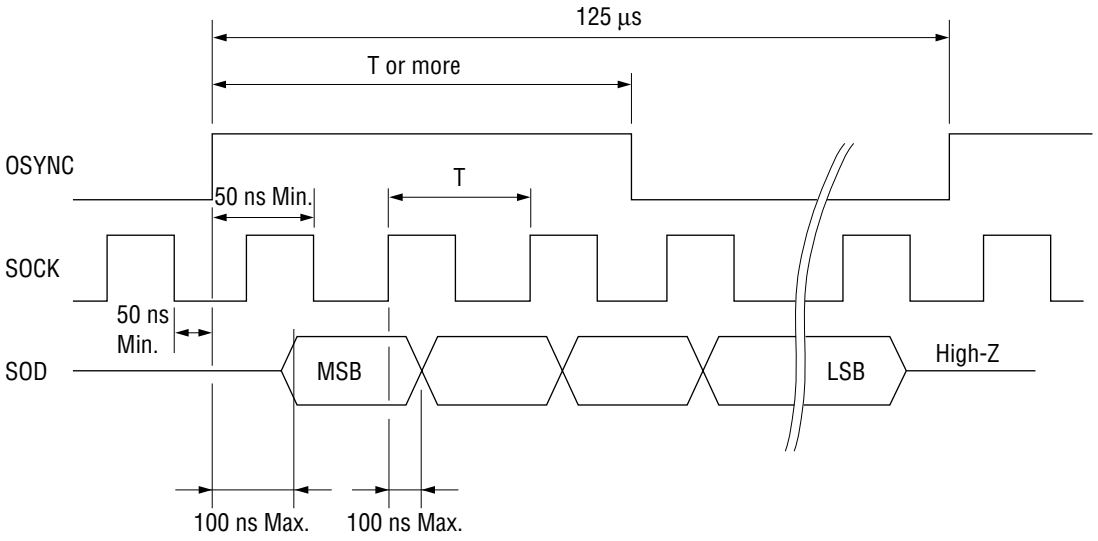
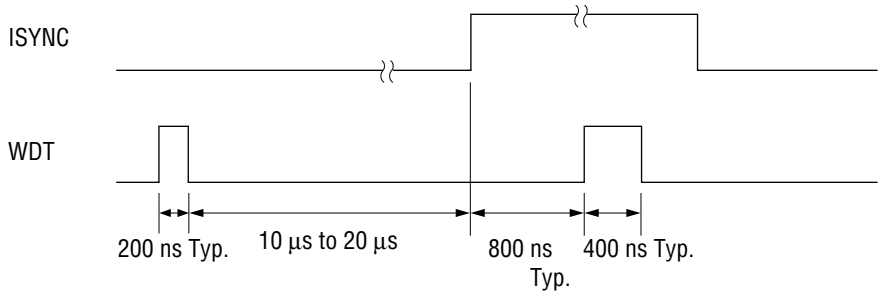


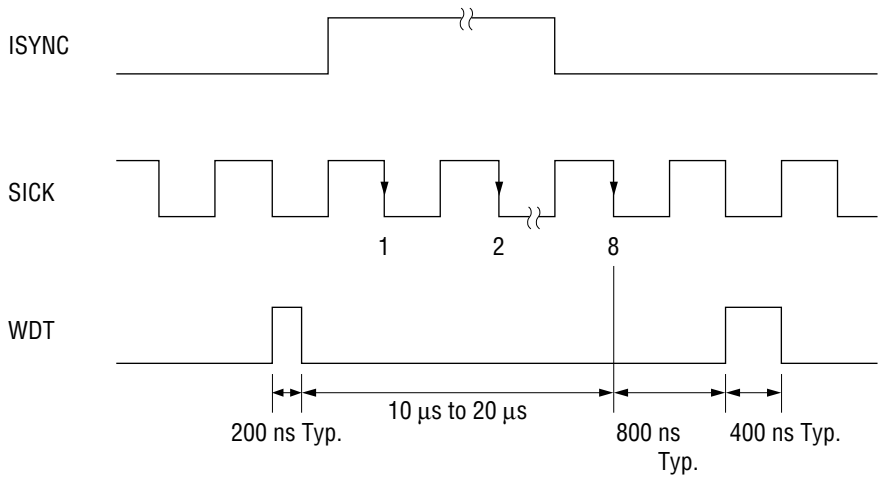
Figure 4

WDT

(1) Parallel data input



(2) Serial data input during coding function



(3) Serial data input during decoding function

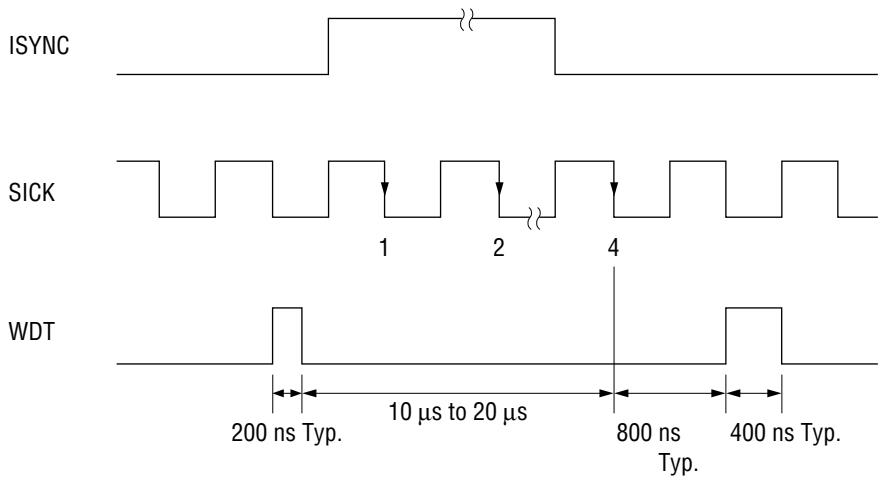


Figure 5

RST

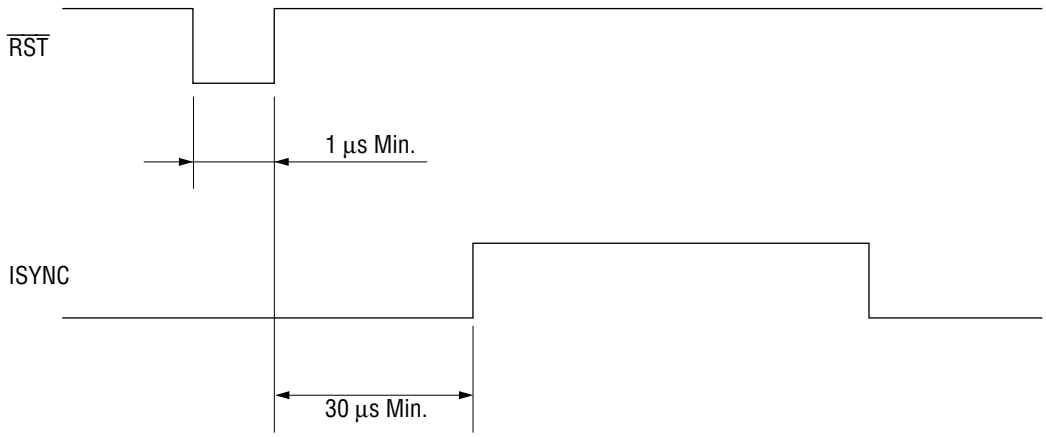
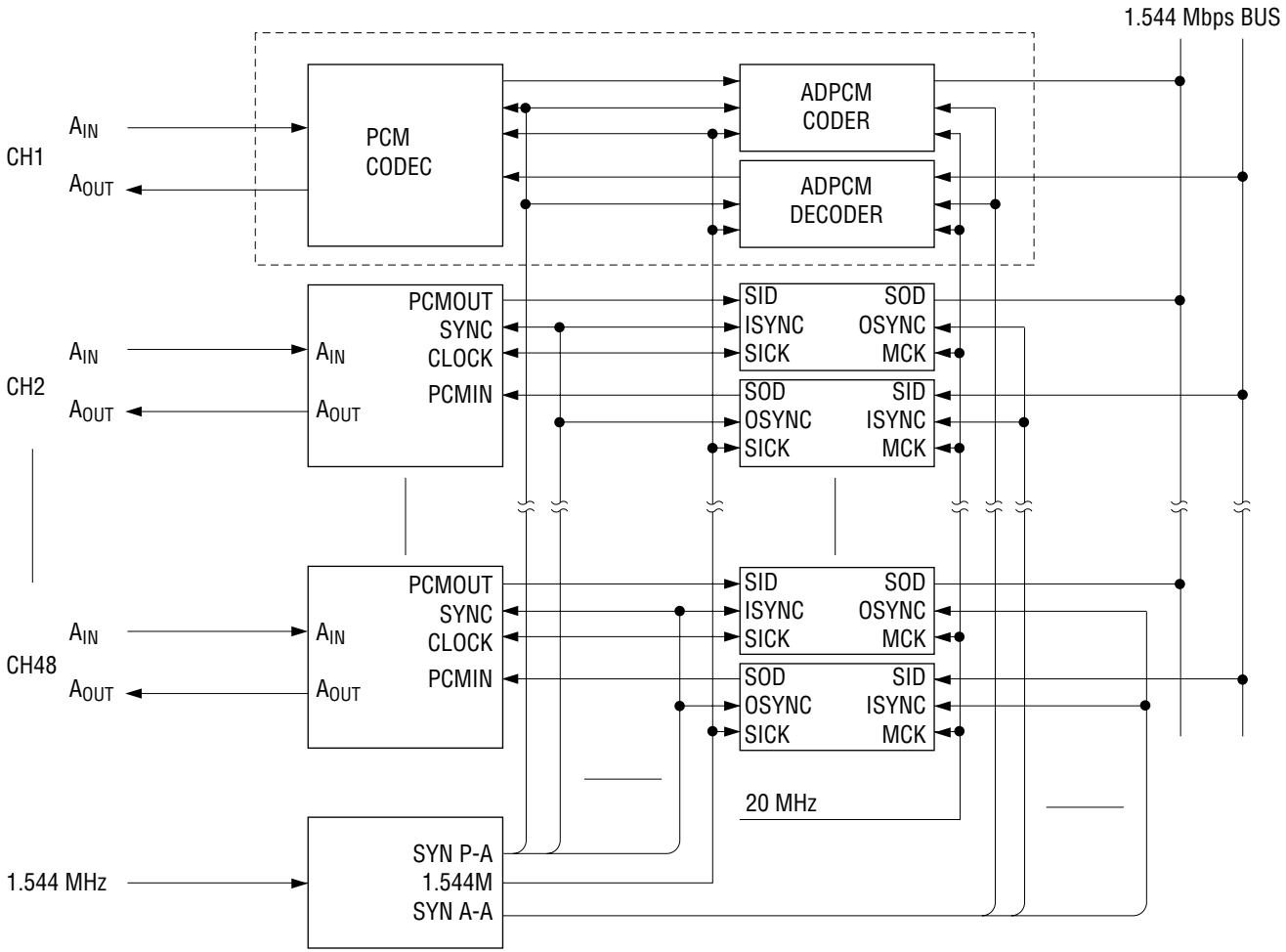
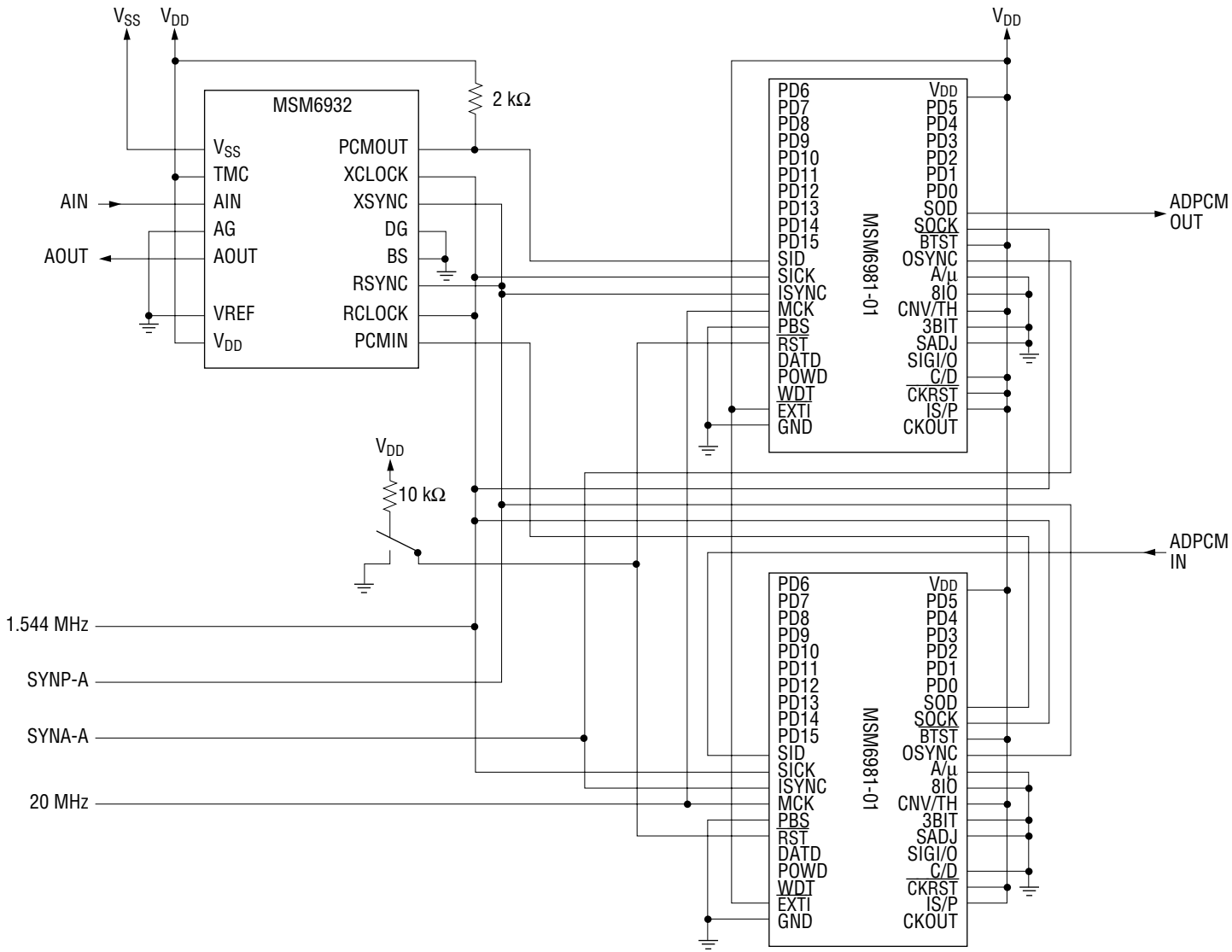


Figure 6

APPLICATION CIRCUIT





RECOMMENDATIONS FOR ACTUAL DESIGN

Countermeasures for malfunctions caused by instantaneous power supply failures

The MSM6981-01 is a digital signal processor (DSP) operated by a built-in program ROM. If the sequence program of device operation runs away, or the stored data in internal memory or in registers is destroyed due to instantaneous power supply failure, the device output becomes abnormal and cannot be recovered automatically unless the external reset signal ($\overline{RST}$) is applied.

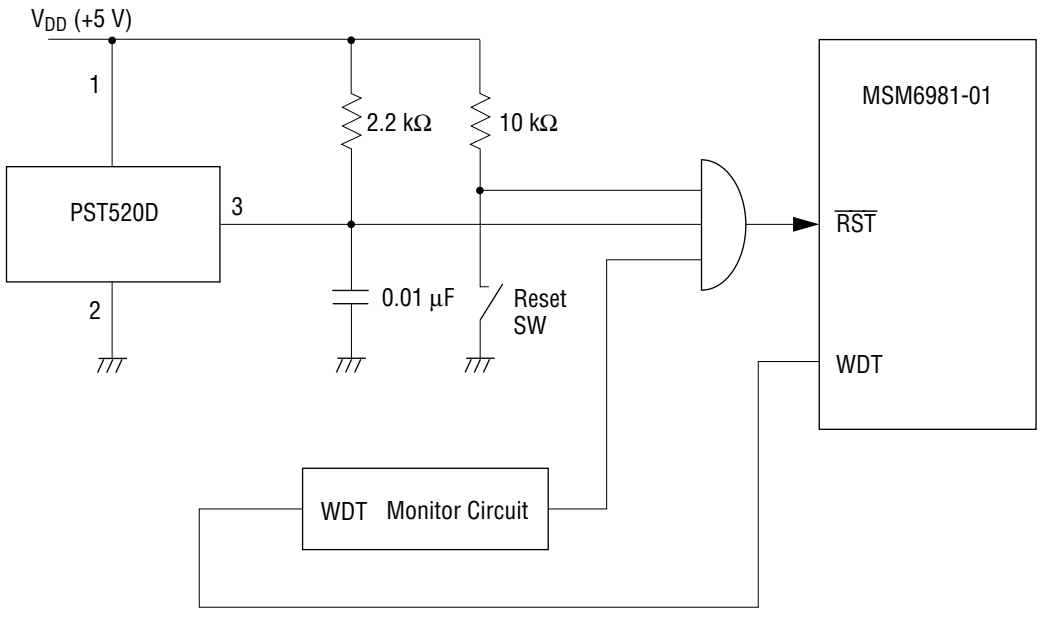
The duration of the instantaneous power supply failure or power voltage drop, and the voltage drop level, which cause malfunctions are specified according to the impedance of the power supply circuit including additional capacitances and inductances, and the pulse waveform at the time of instantaneous power failure.
Experimentally, when the duration is about 1 ms or less and the voltage drop level is about 2 V, device malfunctions may occur.
To prevent malfunctions due to instantaneous power supply failures, the following actions are recommended.

(1) A capacitor (20 µF to 50 µF) and inductance (100 µH to 500 µH) should be inserted closest to the power supply pin of the printed circuit board.

(2) A capacitor (0.1 µF to 1.0 µF) should be inserted between the power supply pin and ground pin of the MSM6981-01.

(3) A power supply reset signal generation IC should be used.
(See the figure below)

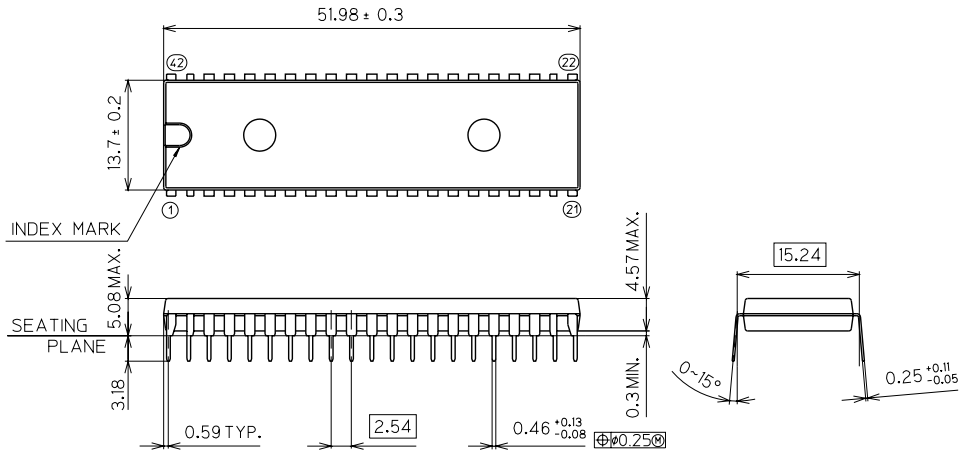
(4) A WDT monitor circuit should be used.



PACKAGE DIMENSIONS

(Unit : mm)

DIP42-P-600-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.20 TYP.