MSM6782-01

REAL TIME CLOCK

GENERAL DESCRIPTION

The MSM6782 - 01 is a CMOS Serial Interface Real Time Clock/Calendar.
The serial interface that can be controlled by mere 3 signal lines has minimized the number of CPU terminals required .

The MSM6782 - 01 provides 30-second adjustment, oscillation stop detection, and periodic flag setting and signal output in 4 diferent cycle periods.
The clock ranges are seconds, minutes, hours, days, months, years, and days of the week.

The interface supply voltage is 2.7V to 5.5V and the clock supply voltage is 2.0V to 5.5V.

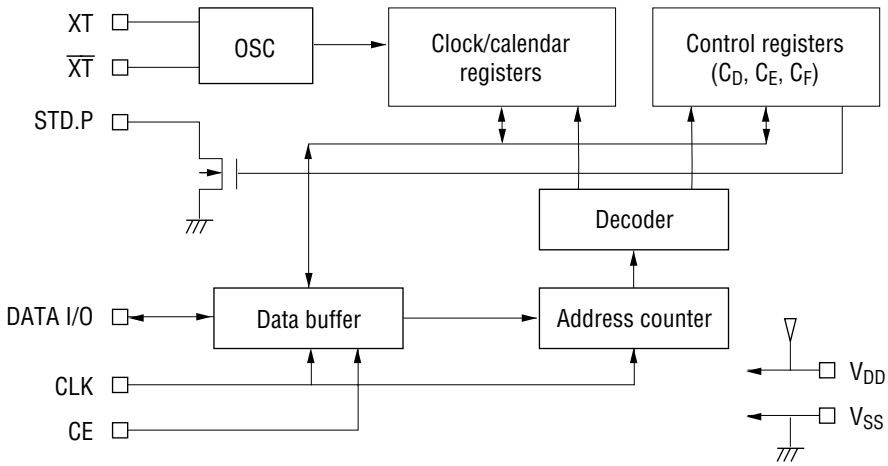
The MSM6782 - 01 comes in an 8-pin DIP package or an 8-pin SOP package.

The MSM6782 - 01 is highly integrated and is suitable for use in a variety of portable applications.

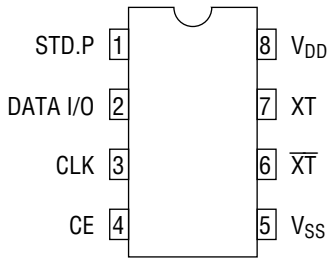
FEATURES

- Real time clock providing seconds, minutes, hours, days, months, and days of the week.
- Serial interface controlled by 3 signal lines
- A periodic interrupt output in 4 different cycle periods (or periodic waveform output)
- Automatic leap year calendar
- 30-second adjustment controlled by software
- Stop and restart of clock
- Wide range of interface power supply: 2.7V to 5.5V
- Wide range of clock power supply: 2.0V to 5.5V
- 32.768kHz external quart crystal
- Low current consumption
- 8-pin plastic DIP (DIP8-P-300) (MSM6782-01RS)
- 8-pin plastic SOP (SOP8-P-250-K) (MSM6782-01MS-K)

BLOCK DIAGRAM

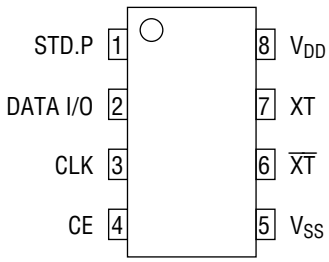


PIN CONFIGURATION



8-Pin Plastic DIP

Note : The actual type name is displayed as 6782-01.



8-Pin Plastic SOP

Note : The actual type name is displayed as 82-01.

PIN DESCRIPTION

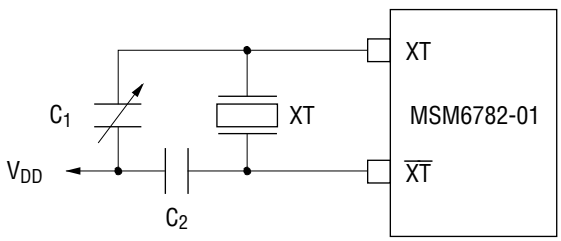
- STD.P (Pin No. 1)
  Periodic output of N-CH OPEN DRAIN type or interrupt signal output of N-CH OPEN DRAIN type for the CPU. The periodic output is used to check the reference signal and oscillation frequency.
  This pin is set as periodic output or interrupt signal output by writing "1" or "0" to the INT/STND bit.
  This output is not inhibited by CE. For more information, see "FUNCTIONAL DESCRIPTION OF REGISTERS".

- DATA I/O (Pin No.2)
  Input/output pin for setting of WRITE mode or READ mode, writing of addresses, or writing/reading of data.
  This pin is used as an input or output pin in high impedance state depending on whether WRITE mode or READ mode is selected in the first 8-bit data cycle after the rising of the CE input pulse.

- CLK (Pin No. 3)
  Shift clock input pin. Data is taken in on the rising edge of a shift clock pulse when in WRITE mode and data is output when in READ mode.

- CE (Pin No. 4)
  Chip enable input pin. "H" level on this pin means "enable".
  When this pin is low, the DATA I/O pin goes into high impedance state, and DATA I/O and CLK are disabled inside the LSI and current stops flowing through those pins.
  "L" level on this pin forces the TEST and REST bits of the C_F registers and the fr flag to be set to "0".
  When turning the power ON, set this pin to "L" level.

- XT, $\overline{XT}$ (Pin Nos. 7 and 6)
  32.768kHz crystal is to be connected to these pins.



  When an external clock is used, it is to be input from XT, while $\overline{XT}$ should be left open.
  The oscillation crystal and capacitors should be placed as close to the IC as possible.
  The oscillation circuit and other signal lines on any side of the LSI should be distant from each other.

- V_{DD}, V_{SS} (Pin No.5)
  Power supply pins. V_{DD} is used for positive supply and V_{SS} is for negative supply.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to 7.0	V
Input voltage	V_I		V_{ss}–0.3 to V_{DD}+0.3	
Output voltage	V_O		V_{ss}–0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	—	2.7 to 5.5	V
Clock power supply	V_{CLK}	—	2.0 to 5.5	V
Crystal frequency	f_X	—	32.768	kHz
Operating temperature	T_{OP}	—	–40 to +85	°C

(Note) Clock power supply : Crystal oscillation and clock must be assured

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5.V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		MIN	TYP	MAX	Unit	Applicable terminal
"H" Input Voltage	V_{IH}	—		0.8V_{DD}	—	—	V	All input pins except XT
"L" Input Voltage	V_{IL}	—		—	—	0.2V_{DD}	V	
"H" Input Current (1)	I_{IH1}	V_I=V_{DD}		—	—	1	µA	CE, CLK
"L" Input Current (1)	I_{IL1}	V_I=V_{SS}		—	—	–1	µA	CE, CLK
"H" Input Current (2)	I_{IH2}	V_I=V_{DD}		—	—	10	µA	DATA I/O
"L" Input Current (2)	I_{IL2}	V_I=V_{SS}		—	—	–10	µA	DATA I/O
"L" Output Current (1)	V_{OL1}	I_O=1.0mA		—	—	0.2V_{DD}	V	DATA I/O
"H" Output Current	V_{OH}	I_O=–400µA		0.8V_{DD}	—	—	V	DATA I/O
"L" Output Current (2)	V_{OL2}	I_O=1.0mA		—	—	0.2V_{DD}	V	STD.P
OFF Leak Current	V_{OFLK}	V_O=V_{DD}		—	—	10.0	µA	STD.P
Current Consumption(1)	V_{DD1}	f_X=32.768kHz V_I(CE)=0V	V_{DD}=5V	—	—	20.0	µA	V_{DD}
Current Consumption(2)	V_{DD2}		V_{DD}=2V	—	—	2.5	µA	V_{DD}

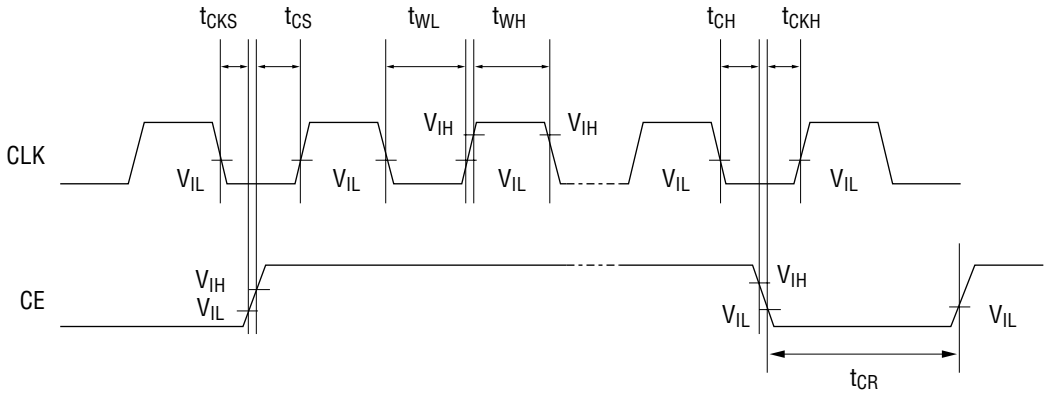
- **AC Characteristics**

(V_{DD} = 2.7 to 5.5V, Ta = –40 to +85°C)

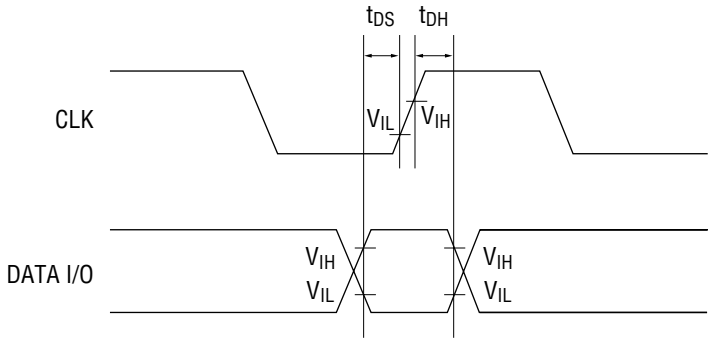
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
CLK "H" Pulse Width	t_{WH}	—	300	—	—	ns
CLK "L" Pulse Width	t_{WL}	—	300	—	—	ns
CE Setup Time	t_{CS}	—	150	—	—	ns
CE Hold Time	t_{CH}	—	200	—	—	ns
CE Recovery Time	t_{CR}	—	300	—	—	ns
CLK Setup Time	t_{CKS}	—	20	—	—	ns
CLK Hold Time	t_{CKH}	—	20	—	—	ns
WRITE Data Setup Time	t_{DS}	—	50	—	—	ns
WRITE Data Hold Time	t_{DH}	—	50	—	—	ns
READ Data Delay Time	t_{RD}	C_L = 50pF	—	—	250	ns
Output Disable Delay Time	t_{RZ}	—	—	—	100	ns
Input Rise, Fall Time	t_{RF}	—	—	—	20	ns

(Note) See Timing Chart.

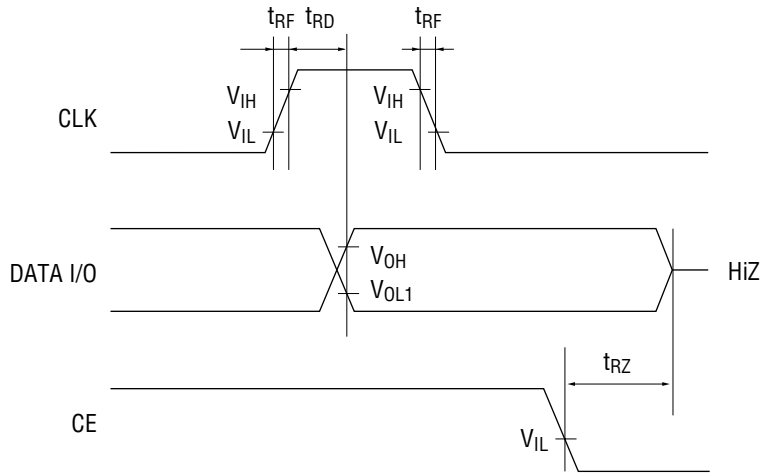
TIMING CHART



WRITE mode



READ mode



FUNCTIONAL DESCRIPTION

REGISTER TABLE

HEX	A3A2A1A0	Register name	D3 (MSB)	D2	D1	D0 (LSB)	Count range	Note
0	0 0 0 0	S_1	s_8	s_4	s_2	s_1	0 to 9	1-second digit register
1	0 0 0 1	S_{10}	f_0	s_{40}	s_{20}	s_{10}	0 to 5	10-second digit register
2	0 0 1 0	MI_1	mi_8	mi_4	mi_2	mi_1	0 to 9	1-minute digit register
3	0 0 1 1	MI_{10}	f_r	mi_{40}	mi_{20}	mi_{10}	0 to 5	10-minute digit register
4	0 1 0 0	H_1	h_8	h_4	h_2	h_1	0 to 9	1-hour digit register
5	0 1 0 1	H_{10}	f_r	PM/AM	h_{20}	h_{10}	0 to 1, 2	10-hour digit register
6	0 1 1 0	D_1	d_8	d_4	d_2	d_1	0 to 9	1-day digit register
7	0 1 1 1	D_{10}	f_r	*	d_{20}	d_{10}	0 to 3	10-day digit register
8	1 0 0 0	MO_1	mo_8	mo_4	mo_2	mo_1	0 to 9	1-month digit register
9	1 0 0 1	MO_{10}	f_r	*	*	mo_{10}	0 to 1	10-month digit register
A	1 0 1 0	Y_1	y_8	y_4	y_2	y_1	0 to 9	1-year digit register
B	1 0 1 1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 to 9	10-year digit register
C	1 1 0 0	W	f_r	w_4	w_2	w_1	0 to 6	Week digit register
D	1 1 0 1	C_D	30-secADJ	IRQ-F	CAL/HW	HOLD	—	Control register D
E	1 1 1 0	C_E	t_1	t_0	INT/STND	MASK	—	Control register E
F	1 1 1 1	C_F	TEST	24/12	STOP	REST	—	Control register F

- The relation between the register's bit 0 and bit 1 is logically positive as 0="L" and 1="H".
- The counted values are in BCD notation.
  For example, with 1-year register (Y_1), (y_8, y_4, y_2, y_1) = (0, 0, 1, 0) means the last digit ("2") of "1992".
- Bit * also can be used as RAM.
- It is unexecutable to write data into the IRQ-F bit.
  The IRQ-F bit is set to "1" when a specified carry determined by the combination of t_1 and t_0 is executed.
  The IRQ-F bit holds "1" until the reading of C_D is complete and is reset to "0" automatically after the reading of C_D is complete .
- The bit fo (OSC FLAG) memorizes that oscillation stops.
  This bit is used to monitor the battery.
  This bit is cleared by writing a "0". (A "1" also can be written into this bit.)
- The bit f_r (READ FLAG) goes "0" when the CE pin is set at "L" level and goes "1" when a carry occurs for 1-second digit while the CE input is at "H" level.
  Thus, it is possible to judge whether a carry occurs for 1-second digit during the reading of the clock register (CE input = "H").
  If the bit f_r is set at "1", it is required to read the clock register once more.
- The "1" of the PM/AM bit indicates PM and its "0" indicates AM.

FUNCTIONAL DESCRIPTION OF REGISTERS

Registers S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, MO_1, MO_{10}, Y_1, Y_{10}, W

- These are abbreviations for $Second_1$, $Second_{10}$, $MInute_1$, $MInute_{10}$, $Hour_1$, $Hour_{10}$, Day_1, Day_{10}, $MOnth_1$, $MOnth_{10}$, $Year_1$, $Year_{10}$, Week.
  These values are in BCD notation.

- Refer to the REGISTER TABLE for more detalied information.
  All registers are logically positive.
  For example, (S_8, S_4, S_2, S_1) = 1001 means 9 seconds.
  The * bit in the register table is writable/readable and can be used as RAM.

- Writing non-existant data may cause a clocking error.

- PM/AM, h_{20}, h_{10}
  a) In 12-hour mode
     The existant time is AM 12:00 through AM 11:00 and PM 12:00 through PM 11:00.
     It is impossble to write data into the h_{20} bit which is fixed to "0" unconditionally. The h_{20} bit is not set by clocking.
  b) In 24-hour mode
     The existant time is 0:00 clock through 23:00 clock.
     The PM/AM bit written is ignored and read out as "0" unconditionally.

- Registers Y_1, Y_{10}, and Leap Year
  When using the Christian Era calendar, Y_1 and Y_{10} are assigned to the last 2 digits of the year of Christian Era.
  The MSM6782 - 01 is capable of automatically identifying a leap year when the last 2-digit number of the year can be divided by four. The last 2-digit number 99 changes to 00 next year.

- Register W
  The count range of the register W is 0 ~ 6. The following table shows a possible bit data definition.

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

- f_o Flag
  The f_o flag bit memorizes that oscillation stops and is used to monitor the output of the battery. The "1" of this bit indicates stop of oscillation. This bit is cleared by writing "0". It is not permitted to write "1" into this bit.

- f_r Flag
  The f_r flag bit indicates a carry when the CE input is at "H" level.
  This bit is checked when the clock/calendar registers are read out. If this bit is set to "1", it is possible to read out these registers without using the HOLD bit.
  This bit is cleared by setting the CE input to "L" level.

C_D REGISTER (Control D Register)

- 30-sec ADJ (30-second adjustment bit)
  When writing to this bit, if the second digits are smaller than 30, the second digits are reset to 00, and if it is larger than 30, the second digits are reset to 00 and a carry into the minute digit is executed. Data can not be written into the S_1 ~ W registers and a "1" can not be written into the REST bit of the C_F register 125µs after writing into this bit because internal processing is being executed. This bit holds "1" 125µs after writing, and returns to "0" automatically. Therefore, data should be written into the S_1 ~ W registers after checking that this bit has returned to "0".

- IRQ - F
  This bit is set to "1" and the STD.P output goes low in the cycle period specified by the combination of bit t_1 and bit t_0 of the C_E register. If INT/STND = "1", the bit status "1" and output level "L" are kept until reading of the C_D register is complete.
  After the C_D register is read out, the IRQ - F bit returns to "0" and the STD.P output goes into high impedance automatically.
  If INT/STD = "0", the IRQ -F bit returns to "0" about 7.8 ms later or immediately after the C_D register is read out, and the STD.P returns to "high impedance" about 7.8 ms later.

- CAL/HW (Clock range switching bit)
  CAL/HW = "1" : Seconds, minutes, hours, days, month, year, day of week
  CAL/HW = "0" : Seconds, minutes, hours, day of week
  If this bit is "0", the D_1, D_{10}, MO_1, MO_{10}, Y_1, Y_{10} registers can be used as 4-bit data RAM and the * bits and f_r bits of the D_{10} and MO_{10} registers also can be used as independent RAM, because these registers stop clock operation.

- HOLD

  "1" of this bit inhibits a carry into 1-second digit.
  Clock operation continues before reaching a second.
  During Hold = "1", if a carry occurs, the S1 counter is incremented by 1 second after Hold = "0".
  This bit is cleared to zero by writing "0".

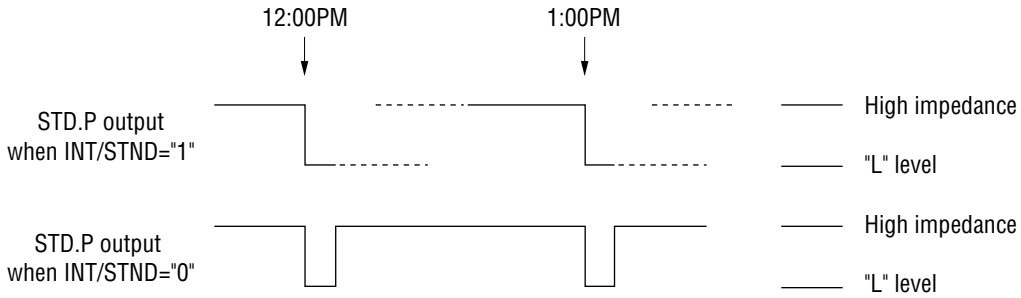
C_E REGISTER (Control E Register)

- t_1, t_0
  INT/STND bit = "1" : Setting of interrupt period
  INT/STND bit = "0" : Setting of periodic waveform

t_1	t_0	Period
0	0	1/64 second
0	1	1 second
1	0	1 minute
1	1	1 hour

The duration that the periodic waveform output is at "L" level is about 7.8ms.
t_1 and t_0 determine the output timing of the STD.P output.

e.g.) When t_1="1", t_0="1", MASK="0"



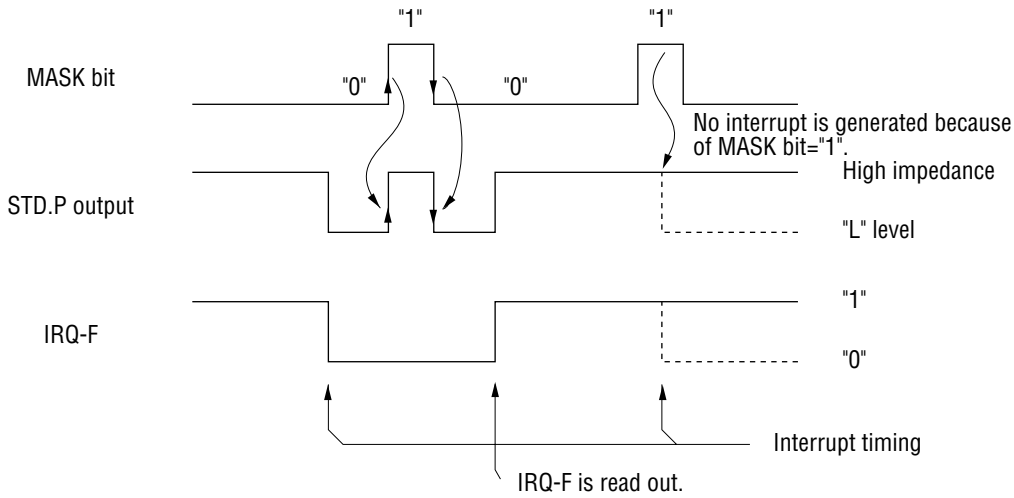
When writing into the 30-sec ADJ bit, a carry can occur.
Therfore, if (t_1, t_0) = (1, 0), (1, 1), the STD.P output may sometime be at "L" level. When INT/STND="0", this "L" level is kept for a maximum of 9.8ms after under-second digits in 30-sec ADJ is cleared (the 30-sec ADJ flag returns to "0").
If the selected interrupt period is 1 second, 1 minute, or 1 hour, and if a carry occurs during the time the S_1, S_{10}, MI_1, MI_{10} registers are overwritten using the HOLD bit, and if data written in these registers determines the interrupt timing set by the carry, the STD.P output will go to "L" level after HOLD="0". (IRQ-F will is set to "1")

In other cases, writing to the S_1, S_{10}, MI_1, MI_{10}, H_1 registers do not change the STD.P output.

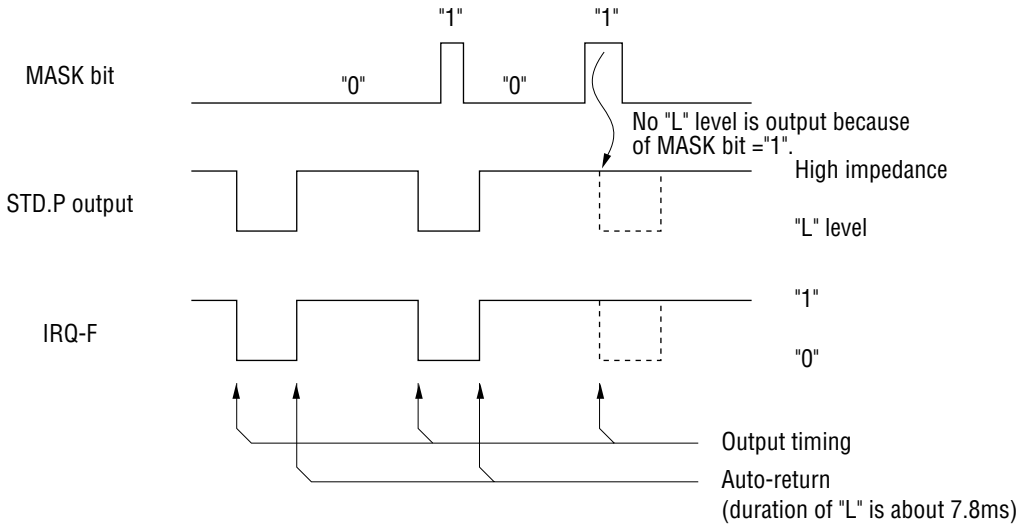
- INT/STND (interrupt-to-Standard waveform switching bit)
  INT/STND = "1" : "1" of the IRQ-F bit and "L" level on the STD.P output are kept until IRQ-F (C_D register) is read out.
  INT/STND = "0" : "1" of the IRQ-F bit returns to "0" after a certain time elapses (after about 7.8ms) or when IRQ-F is read out.
  "L" level on the STD.P output returns to high impedance after a certain time elapses.

- MASK
  "1" of the MASK bit inhibits the setting of "1" to the IRQ-F flag and sets the STD.P output to the high impedance state.

  Interrupt mode (INT/STND="1")



  Periodic timing waveform output mode (INT/STND="0")



  When the IRQ-F bit is read out before auto-return, the IRQ-F bit goes to "0", and the STD.P output keeps "L" level for about 7.8ms, then goes into the high impedance state.

C_F REGISTER (Control F Register)

- TEST
  The TEST bit is used for testing by OKI and should be set to "0".
  This bit can be cleared to "0" by setting the CE pin to "L" level.

- 24/12
  This bit is used to switch between 24-hour system and 12-hour system.
  24/12 = "1" : 24-hour system without PM/AM
  24/12 = "0" : 12-hour system with PM/AM
  When the 24/12 bit is overwritten, data in the H_1 ~ W registers may become undefined. Therefore, it is required to newly set those registers again.

- STOP
  "1" of this bit stops clocking and "0" restarts clocking.

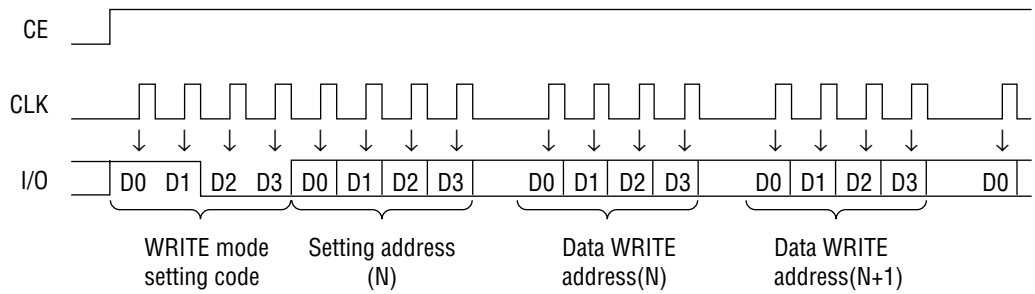
- REST
  "1" of this bit clears under-second-time to zero and at the same time stops clocking. "0" of this bit restarts clocking.
  Take care not to set the TEST bit to "1" when writing "0" into the REST bit.

Usage

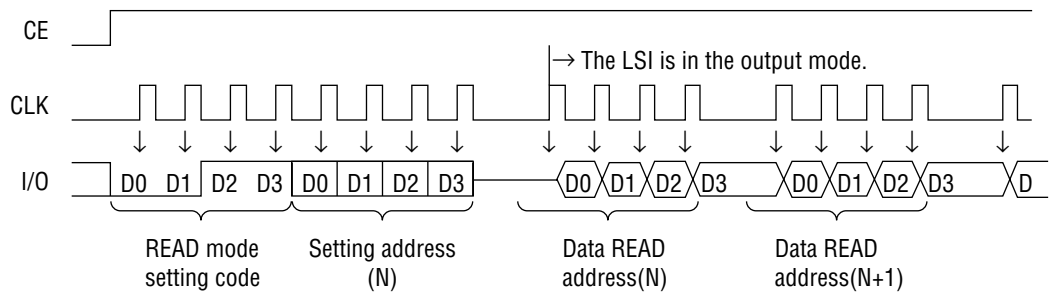
Functional Description

Writing and reading are executed in units of 4 bits after the CE input goes high. If the CE input goes low before 4-bit data input is complete, the 4-bit data written when the CE input goes low is ignored. (Data written before the CE input goes low is valid)
Writing and reading are executed starting from the LSB.

(WRITE)
1) The first 4 bits that are input after the CE input goes high are specified as "3" indicating the WRITE mode. The address to be written is set into the second 4 bits.
2) The third 4 bits are written into the previously-set address.
   The following 4-bit data are sequentially written into automatically-incremented addresses.
3) The address is automatically incremented in a loop way where address F is followed by address 0.

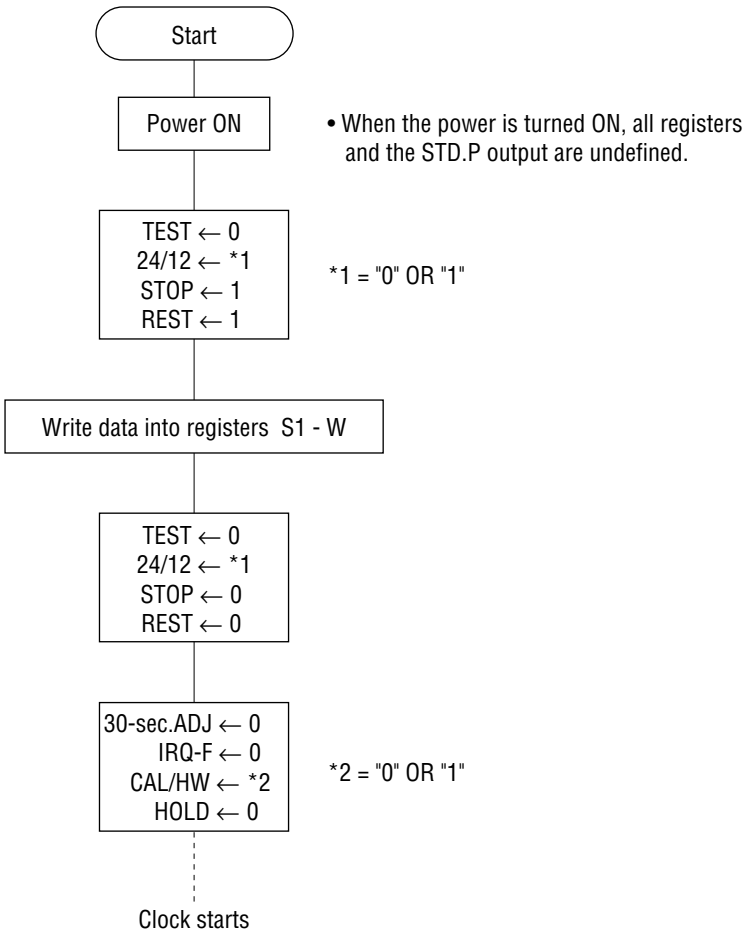


(READ)
1) The first 4 bits that are input after the CE input goes high are specified as "C" indicating the READ mode.
   The address to be read is set into the second 4 bits.
2) The third 4-bit data is read from the previously-set address.
   The following 4-bit data are sequentially read from automatically incremented addresses.
3) The address is automatically incremented in a loop way where address F is followed by address 0.

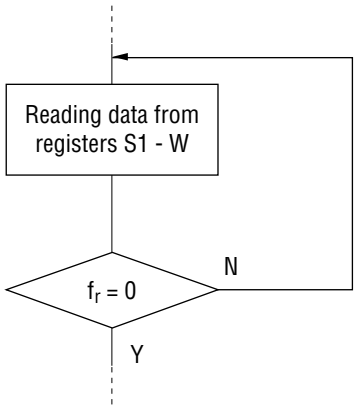


If a character other than "C" or "3" is specified to the mode setting code, the following data is ignored and the DATA I/O pin keeps the input state.

Power Supply



Reading of registers S_1 ~ W

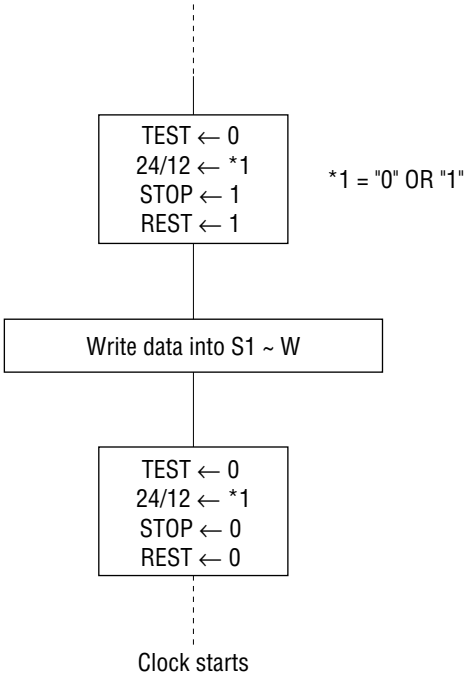


Note 1) Data in registers C_D, C_E, C_F, or registers S1 to W which are used as RAM can be read out without using fr.

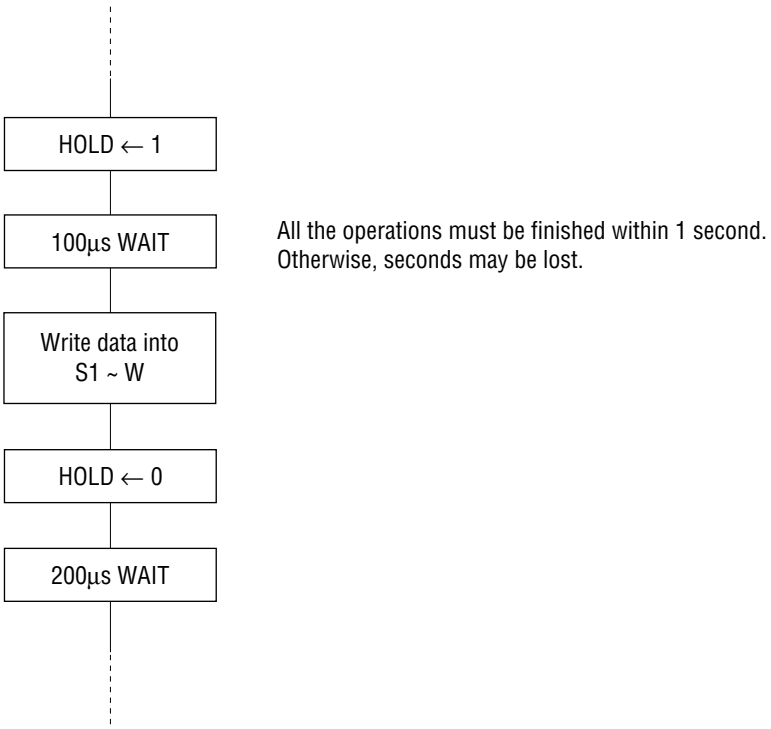
Note 2) Checking fr is complete by checking only the last digit of fr which has been read out.

Writing data to S_1 - W

Method 1 : When under-second data is not stored

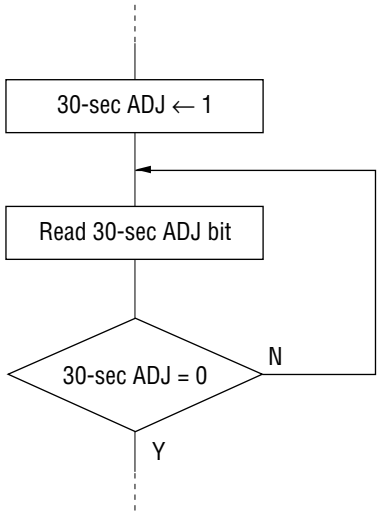


Method 2 : When under-second data is stored (This method is used for switching summer time).

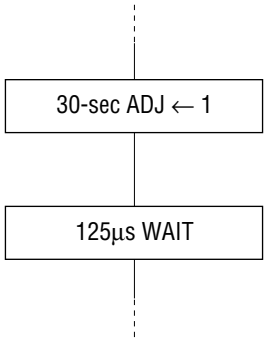


Writing 30-sec ADJ bit

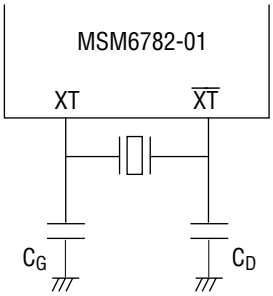
Method 1



Method 2



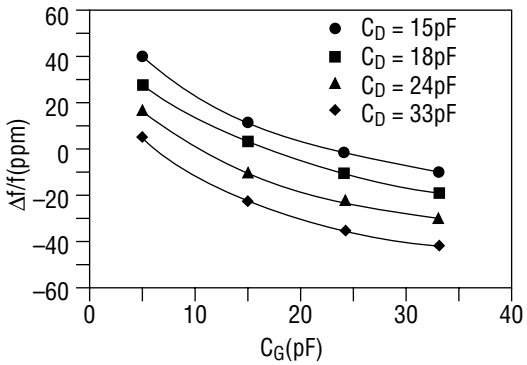
REFERENCE DATA



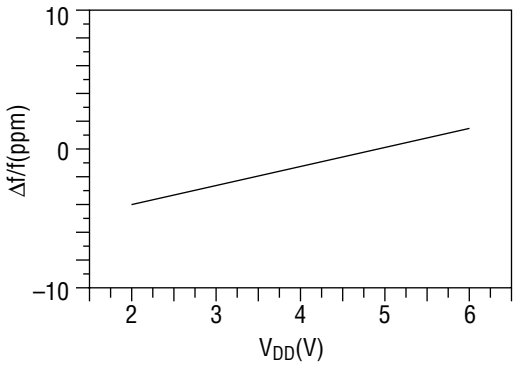
Crystal quartz : Citizen-made CFS-308

C_G = 18pF
C_D = 18pF

Capacitance dependency of oscillation frequency



Supply voltage dependency of oscillation frequency



Supply voltage dependency of I_{DD}