OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM66562/66P563

High-speed High-performance 16-Bit Microcontroller for Compact System

GENERAL DESCRIPTION

The MSM66562/66P563 is a high-speed, high-performance 16-bit microcontroller that employs OKI original nX-8/500S CPU core.
The MSM66562/66P563 includes a 16-bit CPU, ROM, RAM, a 8-bit A/D converter, serial ports, capture/compare timers, and I/O ports.

FEATURES

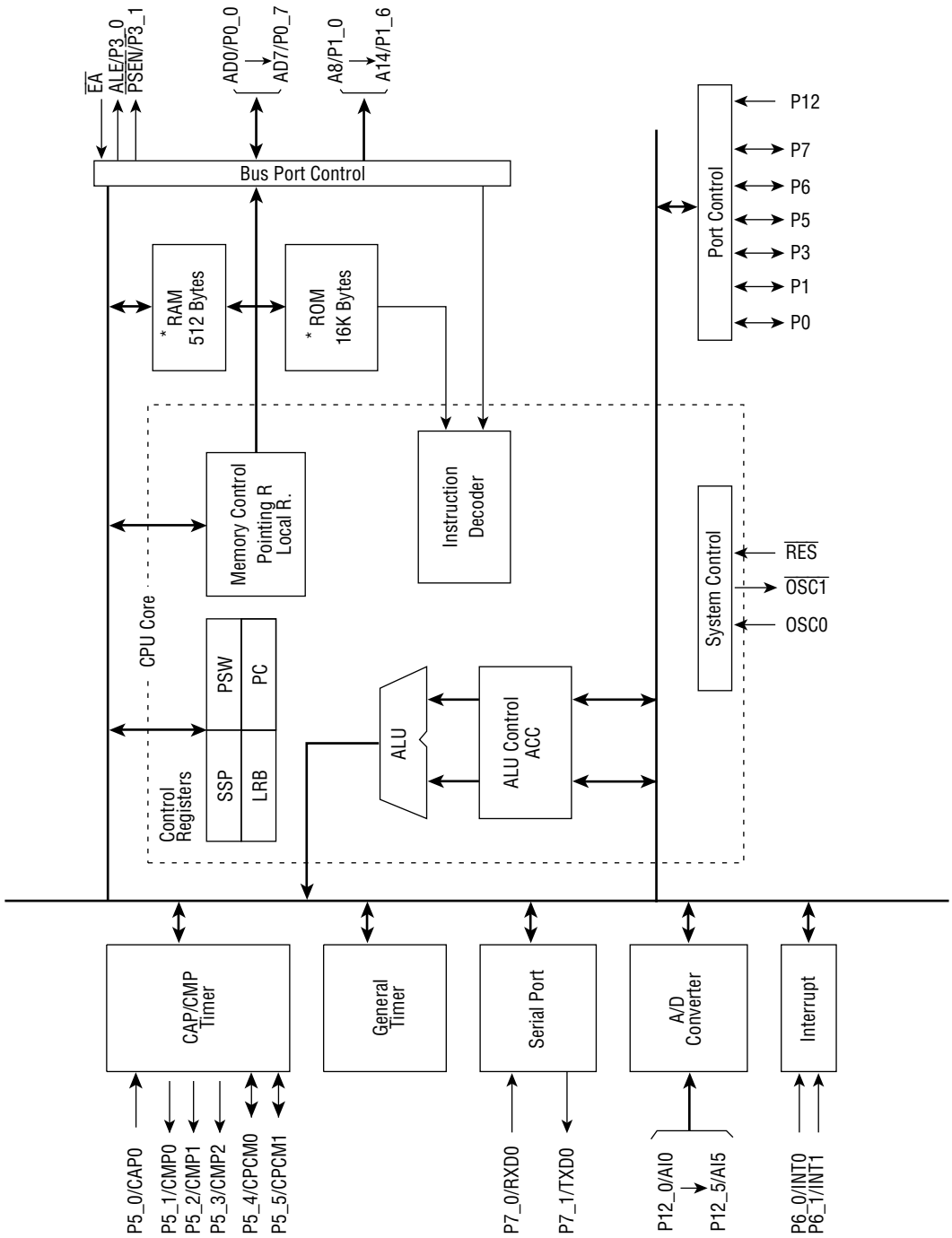
- Program memory space : 32K bytes
  Internal ROM : 16K bytes (MSM66562), 32K bytes (66P563)
- Data memory space : Internal RAM only
  Internal RAM : 0.5K bytes (MSM66562), 1K bytes (MSM66P563)
- High-speed execution
  Minimum instruction execution time : 100 nsec (@ 20 MHz)
- Rich instruction set : Instruction set superior in orthogonal matrix
  8/16-bit data transfer instructions
  8/16-bit arithmetic instructions
  Multiplication and division operation instructions
  Bit manipulation instructions
  Bit logic instructions
  ROM table reference instructions
- Abundant addressing modes : Register addressing
  Page addressing
  Pointing register indirect addressing
  Stack addressing
  Immediate addressing
- I/O port
  Input ports (or analog input ports) : 6 channels
  Input-output ports : 27 bits
  (Each bit can be configured to be an input or output)
- Capture (CAP)/Compare (CMP) timers
  Free run counters : 16 bits × 1
  16-bit CAP : 1
  16-bit CMP : 3
  16-bit CAP/CMP : 2
- 16-bit general timer (also usable for 2ch × 8 bits) : 1
  8-bit geneal counter (or baud rate generator) : 1
- 8-bit serial ports
  UART mode : 1
- 8-bit A/D converter : 6 channels
- Interrupts
  Maskable : Internal 12/external 2
  (2-level priority can be set)
- ROM window function

- Standby modes
  HALT mode
  STOP mode
- Package:

42-pin plastic Shrink DIP (SDIP42-P-600-1.78)	(Product name: MSM66562-×××RS)
	(Product name: MSM66P563-×××RS)
64-pin plastic QFP (QFP64-P-1414-0.80-BK)	(Product name: MSM66562-×××GS-BK)
	(Product name: MSM66P563-×××GS-BK

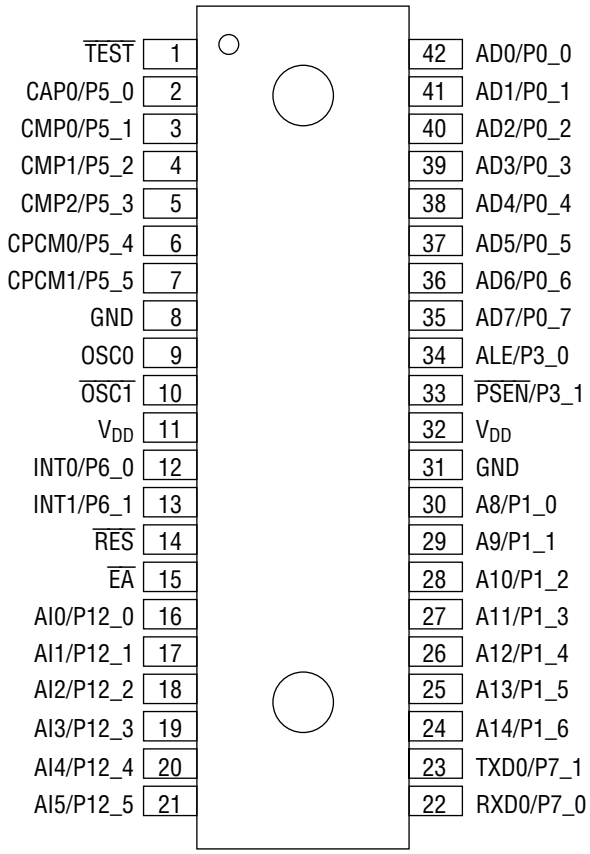
××× indicates a code number.

BLOCK DIAGRAM



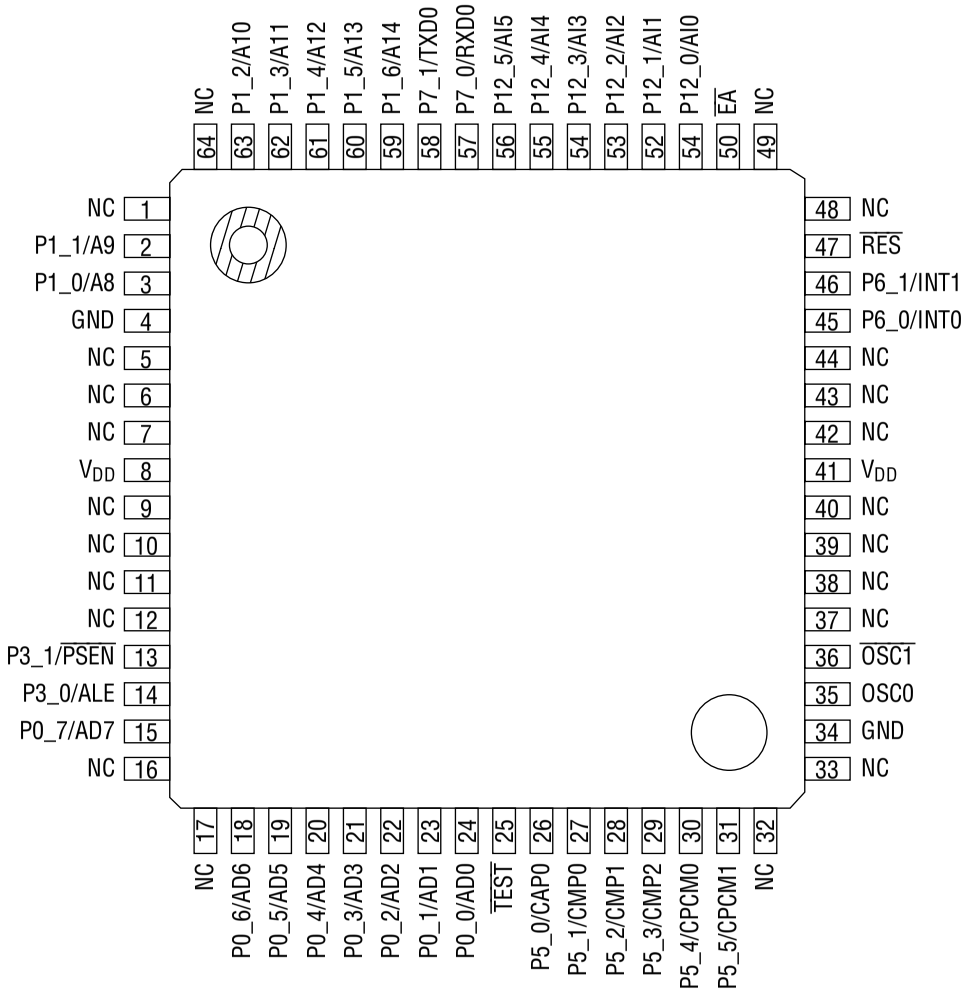
* MSM66P563 (OTP version) contains 32K bytes ROM and 1K bytes RAM.

PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC : No connection pin

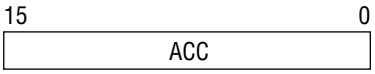
64-Pin Plastic QFP

PIN DESCRIPTION

Symbol	Type	Description
P0_0-P0_7/ AD0-AD7	I/O	P0: 8-bit input-output port. Each bit can be assigned to be an input or an output. AD: When an external memory is used, these pins output the lower 8 bits of the address. These pins also input or output the data.
P1_0-P1_6/ A8-A14	I/O	P1: 7-bit input-output port. Each bit can be assigned to input or output. A: When an external memory is used, these pins output the upper 8 bits of the address.
P5_0/CAP0 P5_1-P5_3/ CMP0-CMP2 P5_4-P5_5/ CPCM0-CPCM1	I/O	P5: 6-bit input-output port. Each bit can be assigned to input or output. CAP : Capture input pin CMP: Compare output pin CPCM: Capture input pin or compare output pin
P6_0/INT0 P6_1/INT1	I/O	P6: 2-bit input-output port. Each bit can be assigned to input or output. INT0/1: External interrupt request input pin
P3_0/$\overline{\text{PSEN}}$ P3_1/ALE	I/O	P3: 2-bit input-output port. Each bit can be assigned to input or output. $\overline{\text{PSEN}}$: Strobe pulse output pin to fetch to external program memory ALE: Timing pulse output pin to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory
P7_0/RXD0 P7_1/TXD0	I/O	P7: 2-bit input-output port. Each bit can be assigned to input or output. RXD0 : SCI0 Receiver data input pin TXD0 : SCI0 Transmitter data output pin
P12_0-P12_5	I	P12: 6-bit input port
AI0-AI15	I	Analog signal input pin for A/D converter
OSC0	I	Basic clock oscillation pin
$\overline{\text{OSC1}}$	0	
$\overline{\text{RES}}$	I	Low-active RESET input pin
$\overline{\text{EA}}$	I	Normally set to "H" level. If set to "L" level, the program memory goes into external access mode and accesses external program memory
V_{DD}	I	Power supply pin
GND	I	Ground pin
$\overline{\text{TEST}}$	I	Be sure to connect this pin to V_{DD}. Test pin for outgoing inspection.

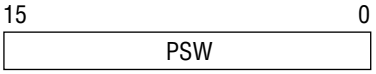
REGISTERS

Accumulator



Control Register (CR)

Program Status Word

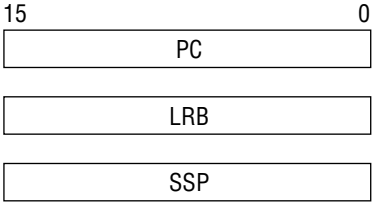


Bit 15 : Carry flag (CY)
Bit 14 : Zero flag (ZF)
Bit 13 : Half carry flag (HC)
Bit 12 : Data descriptor (DD)
Bit 11 : Sign flag (S)
Bit 10 : User flag (F2)
Bit 9 : Overflow flag (OV)
Bit 8 : Master interrupt enable flag (MIE)
Bit 7 : Multiply and accumulate operation bank flag (MAB)*
Bit 6 : User flag (F1)
Bit 5 : Bank common base (BCB1)*
Bit 4 : Bank common base (BCB0)*
Bit 3 : User flag (F0)
Bit 2-0 : System control base 2-0 (SCB2-0)
* Bit 7 (MAB), Bit 5 (BCB1), and Bit 4 (BCB0) can be used as the User flag.

Program Counter

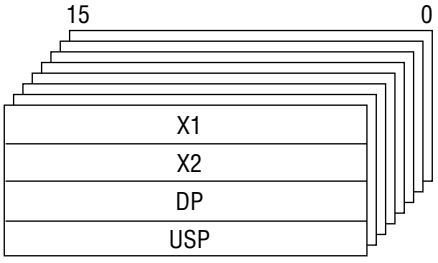
Local Register Base

System Stack Pointer

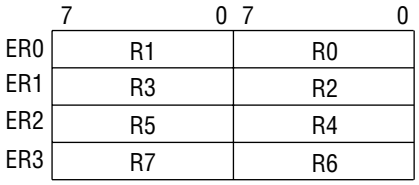


Pointing Register (PR)

Index Register 1
Index Register 2
Data pointer
User Stack Pointer



Local Register



SFR

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0000	System Stack Pointer	—	SSP	R/W	16	FFFF
0001						
0002	Local Register Base	LRBL	LRB		8/16	Undefined
0003		LRBH				
0004	Program Status Word	PSWL	PSW			0000
0005		PSWH				0000
0006	Accumulator	ACCL	ACC			0000
0007		ACCH				0000
0008☆						
0009						
000A						
000B	ROM Window Register	ROMWIN	—	R/W	8	00
000C☆	ROM Ready Control Register	ROMRDY	—			8B
000D						
000E	Stop Code Acceptor	STPACP	—	W		"0"
000F☆	Standby Control Register	SBYCON	—	R/W		C8
0010						
0011						
0012						
0013						
0014						
0015						
0016						
0017						
0018	Port 0 Data Register	P0	—	R/W	8	00
0019☆	Port 1 Data Register	P1				00
001A						
001B	Port 3 Data Register	P3	—	R/W	8	00
001C						
001D☆	Port 5 Data Register	P5	—	R/W	8	C0
001E☆	Port 6 Data Register	P6				00
001F☆	Port 7 Data Register	P7				00
0020	Port 0 Mode Register	P0IO	—	R/W	8	00
0021☆	Port 1 Mode Register	P1IO				00
0022						
0023☆	Port 3 Mode Register	P3IO	—	R/W	8	00
0024						
0025☆	Port 5 Mode Register	P5IO	—	R/W	8	00
0026☆	Port 6 Mode Register	P6IO	—			00
0027☆	Port 7 Mode Register	P7IO	—			00

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0028	Port 1 Secondary Function Control Register	P0SF	—	R/W	8	00
0029☆	Port 2 Secondary Function Control Register	P1SF				00
002A						
002B☆	Port 3 Secondary Function Control Register	P3SF	—	R/W	8	00
002C						
002D☆	Port 5 Secondary Function Control Register	P5SF	—	R/W	8	00
002E☆	Port 6 Secondary Function Control Register	P6SF				00
002F☆	Port 7 Secondary Function Control Register	P7SF				00
0030	Interrupt Request Register 0	IRQ0	—	R/W	8	00
0031☆	Interrupt Request Register 1	IRQ2	—			00
0032						
0033☆	Interrupt Request Register 3	IRQ3	—	R/W	8	00
0034	Interrupt Enable Register 0	IE0	—	R/W	8	00
0035☆	Interrupt Enable Register 1	IE1	—			00
0036						
0037	Interrupt Enable Register 3	IE3	—	R/W	8	00
0038☆	Interrupt Priority Control Register 0	IP0	—	R/W	8	F0
0039☆	Interrupt Priority Control Register 1	IP1	—			00
003A☆	Interrupt Priority Control Register 2	IP2	—			00
003B☆	Interrupt Priority Control Register 3	IP3	—			00
003C						
003D						
003E						
003F☆	Interrupt Priority Control Register 7	IP7	—	R/W	8	00
0040	Free Run Counter	—	FRC	R/W	16	0000
0041						
0042	Capture Register 0	—	CAPR0	R		Undifined
0043						
0044	Compare Out Register 0	—	CMPR0	R/W		0000
0045						
0046	Compare Out Register 1	—	CMPR1			0000
0047						
0048	Compare Out Register 2	—	CMPR2			0000
0049						
004A	Capture Compare Register 0	—	CPCMR0			0000
004B						
004C	Capture Compare Register 1	—	CPCMR1			0000
004D						
004E						
004F						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0050☆	Free Run Counter Control Register	FRCON	—	R/W	8	C0
0051☆	Capture Control Register	CAPCON	—	R/W	8	C0
0052☆	Compare Out Control Register 0	CMPCON0	—	R/W	8	FC
0053☆	Compare Out Control Register 1	CMPCON1	—	R/W	8	FC
0054☆	Compare Out Control Register 2	CMPCON2	—	R/W	8	FC
0055☆	Capture Compare Control Register 0	CPCMCON0	—	R/W	8	FC
0056☆	Capture Compare Control Register 1	CPCMCON1	—	R/W	8	FC
0057						
0058☆	External Interrupt Control Register 0	EXI0CON	—	R/W	8	00
0059						
005A☆	External Interrupt Control Register 1	EXI2CON	—	R/W	8	4C
005B						
005C						
005D						
005E						
005F						
0060☆	TBC Clock Dividing Counter	TBCKDVR	TBCKDV	R/W	8/16	F0
0061☆	TBC Clock Dividing Register	—		R	16	F0
0062						
0063						
0064						
0065						
0066						
0067						
0068	8-bit General Timer 1 Counter	TM1C	TBCKDV	R/W	8/16	Undifined
0069	8-bit General Timer 2 Counter	TM2C				
006A	8-bit General Timer 1 Register	TM1R	TBCKDV			Undifined
006B	8-bit General Timer 2 Register	TM2R				
006C☆	8-bit General Timer 1 Control	TM1CON	—	R/W	8	70
006D☆	8-bit General Timer 2 Control	TM2CON	—			40
006E						
006F						
0070						
0071	8-bit General Timer 3 Counter	TM3C	—	R/W	8	Undifined
0072☆	8-bit General Timer 3 Register	TM3R	—			Undifined
0073	8-bit General Timer 3 Control	TM3CON	—			70
0074						
0075						
0076						
0077						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
0078						
0079						
007A						
007B						
007C						
007D						
007E						
007F						
0080☆	SIO0 Transmit Control Register	ST0CON	—	R/W	8	05
0081☆	SIO0 Receive Control Register	SR0CON	—			09
0082	SIO0 Transmit/Receive Buffer Register	SI0BUF	—			Undifined
0083☆	SIO0 Status Register	S0STAT	—			C0
0084						
0085						
0086						
0087						
0088						
0089						
008A						
008B						
008C						
008D						
008E						
008F						
0090						
0091						
0092						
0093						
0094						
0095						
0096						
0097						
0098						
0099						
009A						
009B						
009C						
009D						
009E						
009F						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
00C8						
00C9						
00CA						
00CB						
00CC						
00CD						
00CE						
00CF						
00D0						
00D1						
00D2						
00D3						
00D4						
00D5						
00D6						
00D7						
00D8						
00D9						
00DA						
00DB						
00DC						
00DD						
00DE						
00DF						
00E0						
00E1						
00E2						
00E3						
00E4						
00E5						
00E6						
00E7						
00E8						
00E9						
00EA						
00EB						
00EC						
00ED						
00EE						
00EF						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

SFR (Continued)

Address [H]	Name	Abbreviated Name (BYTE)	Abbreviated Name (WORD)	R/W	8/16 Operation	Reset Status
00F0						
00F1						
00F2						
00F3						
00F4						
00F5						
00F6						
00F7						
00F8						
00F9						
00FA						
00FB						
00FC	Emulator Use Area					
00FD	(Do not access this area.)					
00FE						
00FF						

☆ mark in the address column indicates that there is a nonexistent bit in its register.

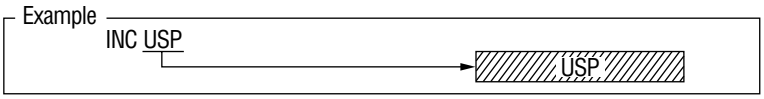
Notes: 1. Do not write a read-only SFR.
2. Do not read a write-only SFR.
3. Do not provide 16-bit manipulation to 8-bit manipulation only SFR.
4. Do not provide 8-bit/1-bit manipulation of to 16-bit manipulation only SFR.
5. Do not access the addresses which are not allocated with a register.
6. Do not access the emulator application area.

ADDRESSING MODES

The MSM66562/66P563 provides independent 0.5K-byte data (1K bytes for MSM65P63) and 32K-byte program spaces with various types of addressing modes. These modes are shown below for both RAM (for data space) and ROM (for program space).

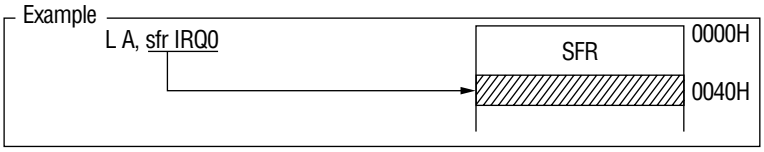
RAM Addressing Mode (for data space)

- **Register addressing**

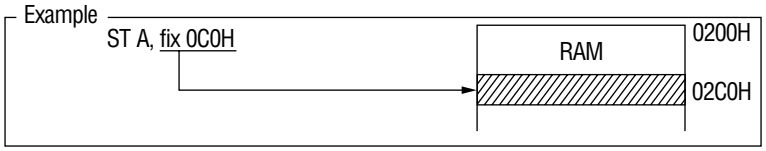


- **Page addressing**

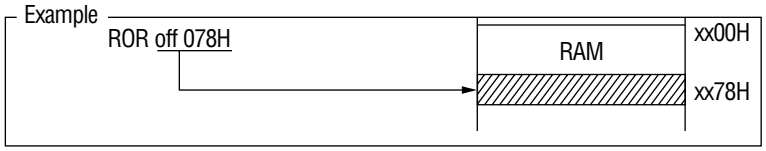
a) sfr page



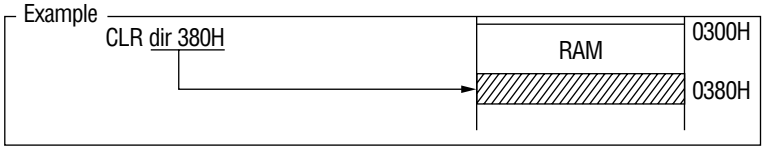
b) Fixed page



c) Current page

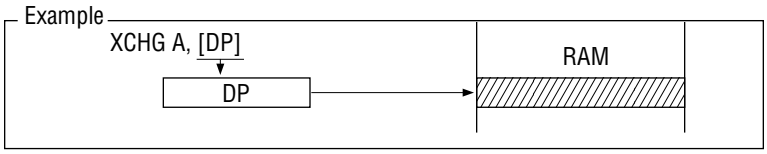


- **Direct data addressing**

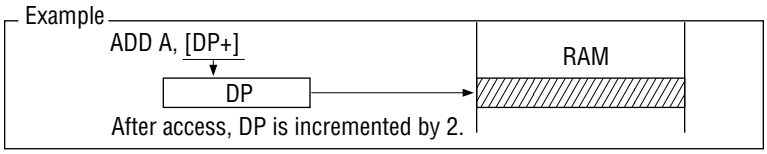


- **Pointing register indirect addressing**

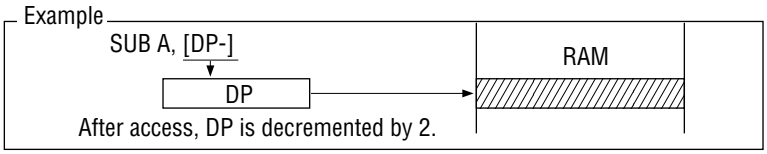
a) DP/X1 indirect



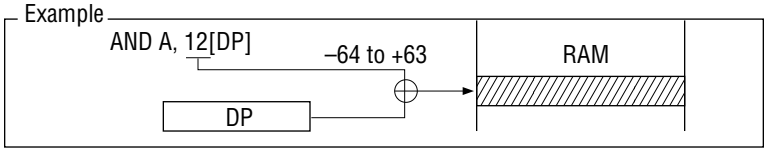
b) Post increment DP indirect



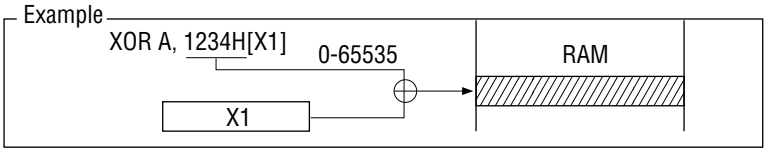
c) Post decrement DP indirect



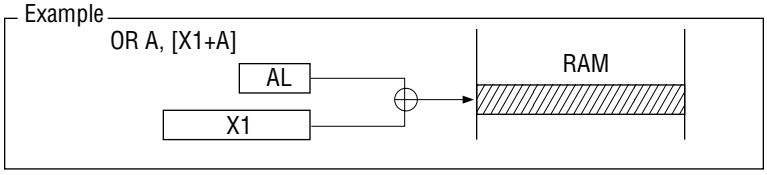
d) DP/USP indirect with 7-bit displacement



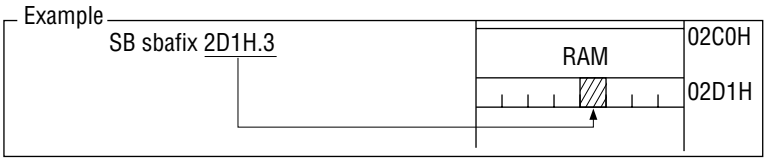
e) X1/X2 indirect with 16-bit base



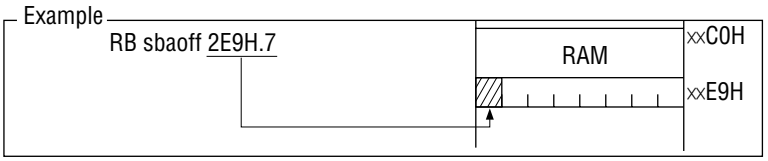
f) X1 indirect with 8-bit register (A, R0) displacement



- **Special bit area addressing**
  a) Fixed page SBA area (02C0H to 02FFH)

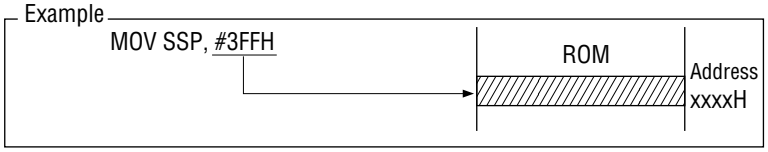


  b) Current page SBA area (××C0H to ××FFH)

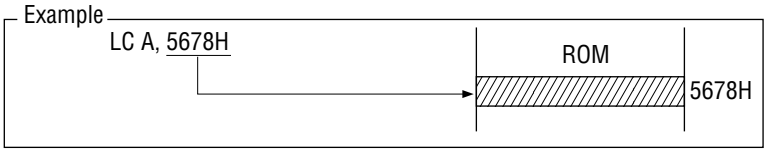


ROM Addressing Mode (for program space)

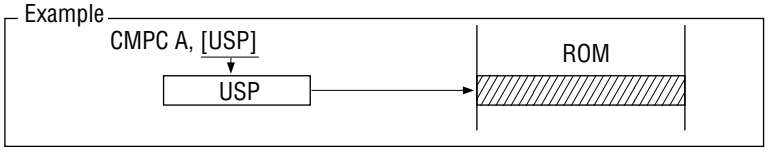
- **Immediate addressing**



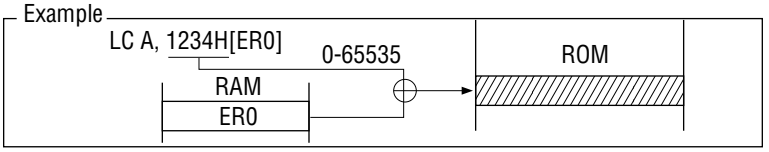
- **Table data addressing**
  TSR specifies the address segment.
  a) Direct



  b) RAM addressing indirect

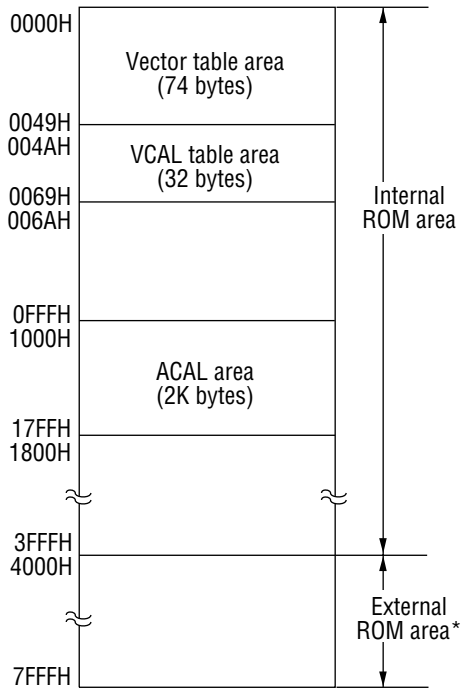


  c) RAM addressing indirect with 16-bit base



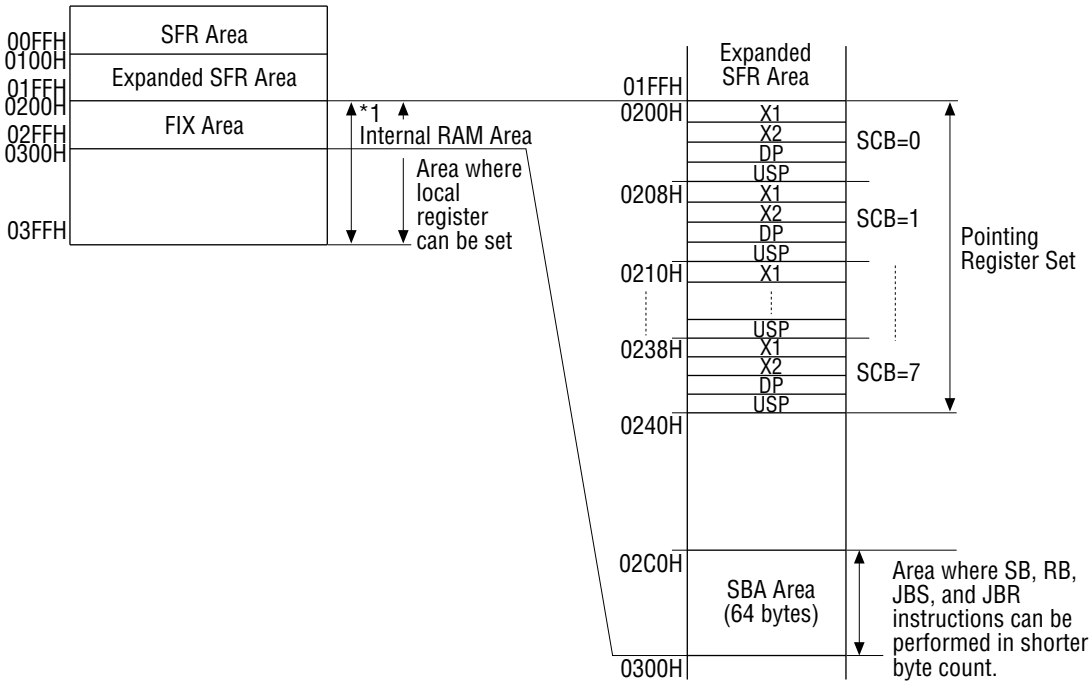
MEMORY MAP

Program Memory Space



* For MSM66P563 (OTP version), 4000H to 7FFFFH are in the internal ROM area.

Data Memory Space *2



*1 For MSM66P563 (OTP version), 200H to 5FFH are in the internal RAM area.

*2 1000H to 7FFFH inthe data space (also can be used as a ROM window area.

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

Parameter	Symbol	Condition		Rating	Unit
Power Supply Voltage	V_{DD}	GND=0 V Ta = 25°C		–0.3 to 7.0	V
Input Voltage	V_I			–0.3 to V_{DD}+0.3	
Output Voltage	V_O			–0.3 to V_{DD}+0.3	
Analog Input Voltage	V_{AI}			–0.3 to V_{DD}	
Power Dissipation	P_D	Ta=85°C	Per package	—	mW
			Per output	50	
Storage Temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Digital Power Supply Voltage	V_{DD}	f_{OSC}≤20 MHz		4.5 to 5.5	V
Analog Input Voltage	V_{AI}	—		GND to V_{DD}	
Memory Hold Voltage	V_{DDH}	f_{OSC}=0 Hz		2.0 to 5.5	
Operating Frequency	f_{OSC}	V_{DD}=5 V±10%		0 to 20	MHz
Ambient Temperature	Ta	—		–40 to +85	°C
Fan Out	N	MOS load		20	—
		TTL load	P0, P3_0, P3_1	2	
			P1, P5, P6, P7	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics (Preliminary)

(V_{DD}=5 V±10%, Ta=–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H Level Input Voltage 1	V_{IH}	—	2.2	—	V_{DD}+0.3	V
H Level Input Voltage 2, 4, 5, 6, 7			0.80V_{DD}	—	V_{DD}+0.3	
L Level Input Voltage 1	V_{IL}	—	–0.3	—	0.8	
L Level Input Voltage 2, 4, 5, 6, 7			–0.3	—	0.2V_{DD}	
H Level Output Voltage 1, 4	V_{OH}	I_{OH}=–400 µA	V_{DD}–0.4	—	—	
H Level Output Voltage 2		I_{OH}=–200 µA	V_{DD}–0.4	—	—	
L Level Output Voltage 1, 4	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	
L Level Output Voltage 2		I_{OL}=1.6 mA	—	—	0.4	
Input Leakage Current 3, 6	I_{IH}/I_{IL}	V_I=V_{DD}/0 V	—	—	1/–1	µA
Input Current 5			—	—	1/–250	
Input Current 7			—	—	15/–15	
H Level Output Current 1, 4	I_{OH}	V_O=2.4 V	–2	—	—	mA
H Level Output Current 2			–1	—	—	
L Level Output Current 1, 4	I_{OL}		10	—	—	
L Level Output Current 2			5	—	—	
Output Leakage Current 1, 2, 4	I_{LO}	V_O=V_{DD}/0 V	—	—	±2	µA
Input Capacitance	C_I	f=1 MHz, Ta=25°C	—	5	—	pF
Output Capacitance	C_O		—	7	—	
Current Consumption (in STOP mode)	I_{DDS}	V_{DD}=2 V, Ta=25°C*	—	0.2	10	µA
		*1	—	1	100	
Current Consumption *2 (in HALT mode)	I_{DDH}	f_{OSC}=20 MHz No load	—			mA
Current Consumption *2	I_{DD}		—			

1. Applied to P0
2. Applied to P1 to P7 (except P3_0/ALE, P3_1/$\overline{PSEN}$, P7_0/$\overline{WR}$, P7_1/$\overline{RD}$)
3. Applied to A_{IN}
4. Applied to P3_0/ALE, P3_1/$\overline{PSEN}$, P7_0/$\overline{WR}$, P7_1/$\overline{RD}$
5. Applied to $\overline{RES}$
6. Applied to $\overline{EA}$
7. Applied to OSC0

*1 Ports for input pins are V_{DD} or GND, otherwise no load.

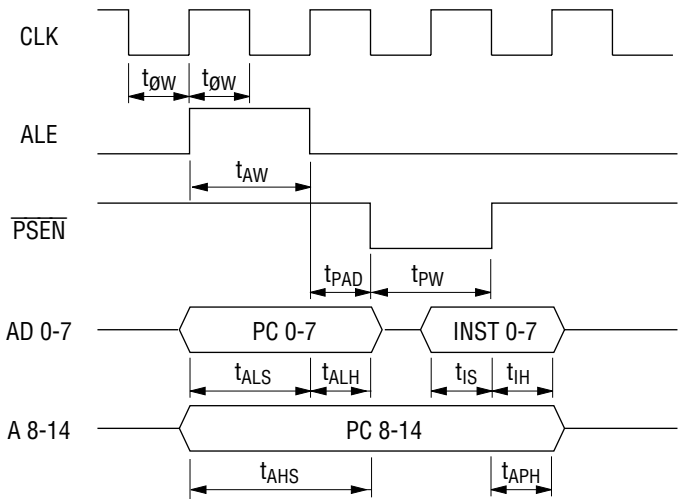
*2 Indicates the current consumption when A/D converter is not operating.
When A/D convertion is operating current is consumed max. 2 mA more than that when it is not operating.

AC Characteristics (Preliminary)

- **External program memory control**

(V_{DD}=5 V±10%, Ta=–40 to +85°C)

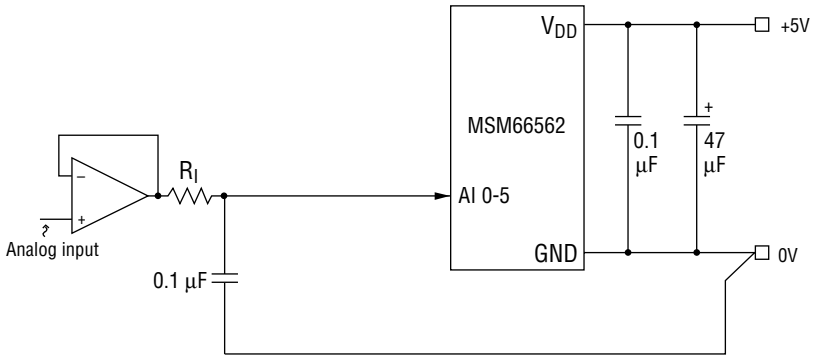
Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) pulse width	$t_{øW}$	—	25	—	nsec
ALE pulse width	t_{AW}	C_L=50 pF	$2t_{øW}$–10	—	
$\overline{PSEN}$ pulse width	t_{PW}		$2t_{øW}$–10	—	
$\overline{PSEN}$ pulse delay time	t_{PAD}		$t_{øW}$–10	$t_{øW}$+10	
Low-order address set-up time	t_{ALS}		$2t_{øW}$–10	$2t_{øW}$+10	
Low-order address hold time	t_{ALH}		$t_{øW}$–10	$t_{øW}$+10	
High-order address set-up time	t_{AHS}		$3t_{øW}$–10	$3t_{øW}$+10	
High-order address hold time	t_{APH}			$t_{øW}$+10	
Instruction set-up time	t_{IS}			—	
Instruction hold time	t_{IH}			$t_{øW}$–10	



A/D CONVERTER CHARACTERISTICS (Preliminary)

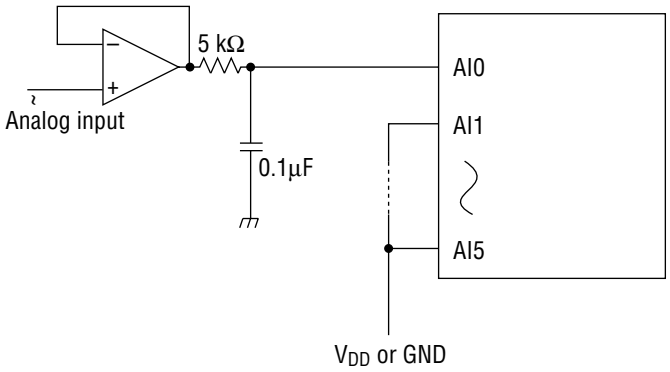
(Ta=–40 to +85°C, V_{DD}=5 V±10%, GND=0 V, f_{OSC}=20 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit. Analog input source impedance $R_I \leq 5$ kΩ t_{CONV}=19.2 µsec	—	—	8	Bit
Linearity Error	E_L		—	—		LSB
Differential Linearity Error	E_D		—	—		
Zero Scale Error	E_{ZS}			—		
Full Scale Error	E_{FS}		—	—		
Crosstalk	E_{CT}	Refer to the measuring circuit.	—	—		
Conversion Time	t_{CONV}	by ADTM set data	6.4	–	19.2	µs/CH



R_I (Analog input source impedance) ≤ 5 kΩ

Recommended Circuit



Crosstalk is defined as the difference between the A/D conversion result when applying the identical analog input to AI0 to AI5 and the A/D conversion result in the circuit in the left figure.

Crosstalk Measuring Circuit

Definitions of Terms

Resolution
The minimum distinguishable analog input value. For 8 bits, 2^8=256, i.e. (V_{DD}–GND) ÷ 256.

Linearity error
The variance between the ideal conversion characteristics as a 8-bit A/D converter and the actual conversion characteristics. (Quantized error is therefore not included.)
In the ideal conversion, a voltage between V_{DD} and GND is divided into 256 equal steps.

Differential linearity error
The smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB=(V_{DD}–GND) ÷ 256 ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.

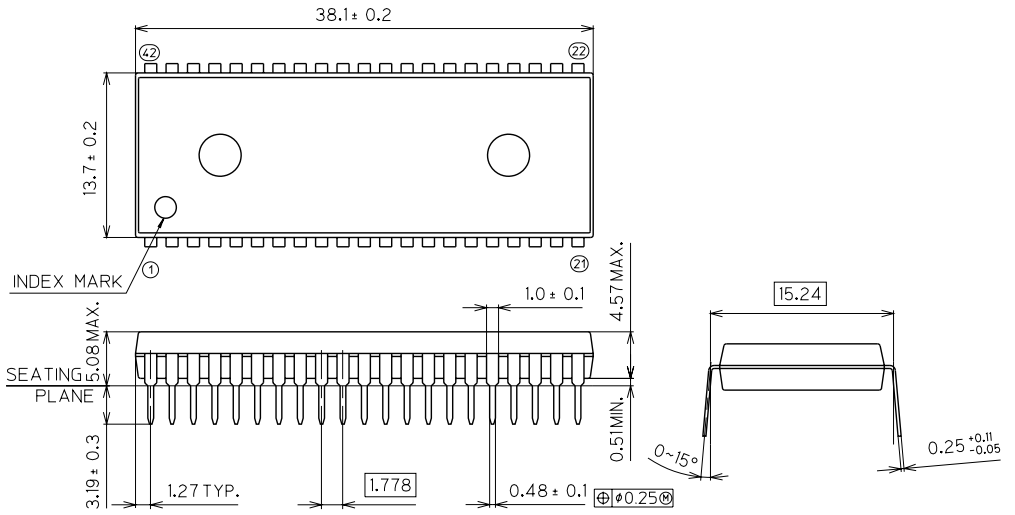
Zero scale error
The variance between the ideal conversion characteristics at the switching point of digital output "00H to 01H" and actual conversion characteristics.

Full scale error
The variance between the ideal conversion characteristics at the switching point of digital output "0FEH to 0FFH" and actual conversion characteristics.

PACKAGE DIMENSIONS

(Unit : mm)

SDIP42-P-600-1.78



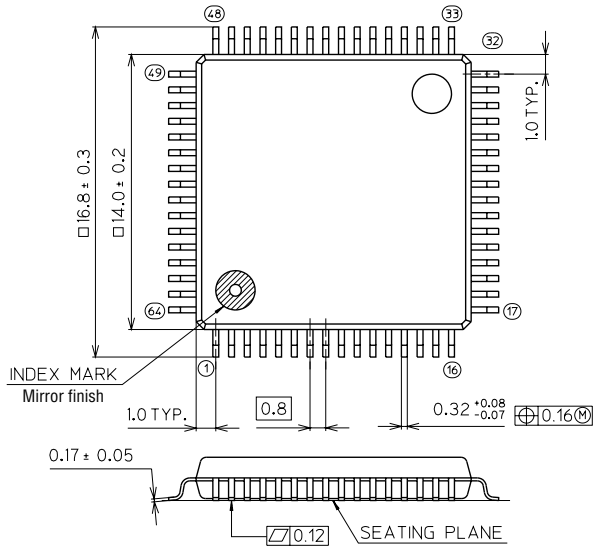
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.52 TYP.

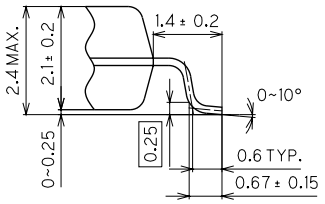
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP64-P-1414-0.80-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

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