OKI Semiconductor

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MSM6555B-xx

DOT MATRIX LCD CONTROLLER WITH 17-DOT COMMON DRIVER AND 80-DOT SEGMENT DRIVER

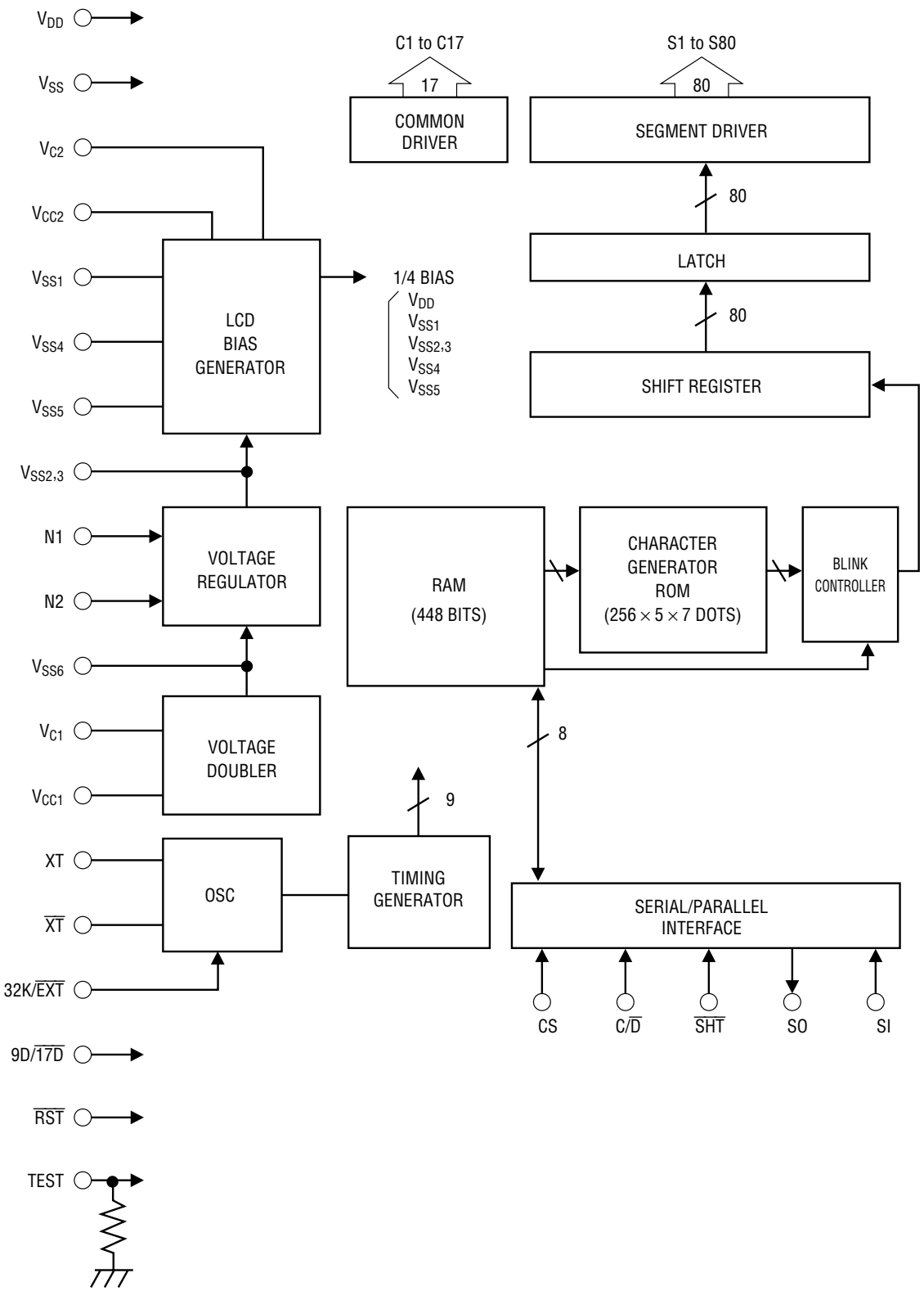
GENERAL DESCRIPTION

The MSM6555B-xx is a dot matrix LCD controller with 17-dot common driver and 80-dot segment driver comprising a display RAM, character generation ROM, LCD bias generation circuit and control circuit.
The LCD driving bias generation circuit incorporated in the MSM6555B-xx allows LCD bias voltage to be obtained merely by providing a specified capacitance externally.
The MSM6555B-xx can display the arbitrator (arbitrary character) patterned on the LCD panel.

FEATURES

- Serial interface with microcontroller
- Dot matrix LCD controller with 17-dot common driver and 80-dot segment driver (up to 16 digits × 2 lines can be displayed)
- 256 character ROM (5 × 7 dots)
- 1/9 duty (1 line; character + cursor + arbitrator) or 1/17 duty (2 lines; character + cursor, 1 line; arbitrator) display
- LCD driving bias voltage generation circuit
- 80-dot arbitrator
- Low standby current
- Gold bump chip
- Optional when TCP is adopted

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable pin
Supply Voltage	V_{DD}	Ta = 25°C, V_{DD}–V_{SS}	–0.3 to +3.5	V	V_{DD}, V_{SS}
Input Voltage	V_I	Ta = 25°C	0 to V_{DD} + 0.3	V	All inputs
Power Dissipation	P_D	—	*1	mW	—
Storage Temperature	T_{STG}	—	–55 to +150	°C	—

*1 Power dissipation depends on the radiation characteristic determined by assembling condition. Junction temperature should be set to 150°C or less.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable pin
Supply Voltage	V_{DD}	V_{DD}–V_{SS}	2.5 to 3.3	V	V_{DD}, V_{SS}
IC Internal Oscillation Frequency (*1)	f_{INT}	—	20 to 38.4	kHz	—
Operating Temperature	T_{op}	—	–10 to +70	°C	—

*1 For the IC internal oscillation frequency, see the explanation of the SF command in Command description.

Note: Completely shut off light to ensure that IC chips will not be exposed to light.

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 3V ±10%, Ta = −10 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage 1	V_{IH1}	—	V_{DD}−0.3	—	V_{DD}	V	XT
"L" Input Voltage 1	V_{IL1}	—	0	—	0.6	V	XT
"H" Input Voltage 2	V_{IH2}	—	0.8V_{DD}	—	V_{DD}	V	Input pins except XT
"L" Input Voltage 2	V_{IL2}	—	0	—	0.2V_{DD}	V	Input pins except XT
"H" Input Current 1	I_{IH1}	V_I = V_{DD}	—	—	1	µA	Input pins except TEST and XT
"L" Input Current	I_{IL}	V_I = 0V	—	—	−1	µA	Input pins except XT
"H" Input Current 2	I_{IH2}	V_I = V_{DD}	0.1	—	0.4	mA	TEST
"H" Output Voltage	V_{OH}	I_{OH} = −400µA	V_{DD}−0.5	—	—	V	SO
"L" Output Voltage	V_{OL}	I_{OL} = 1.5mA	—	—	0.5	V	SO
Off Leakage Current	I_{OFF}	V_I = V_{DD}/0V	—	—	±10	µA	SO
COM Output Resistance	R_C	I_O = ±50µA	—	—	5	kΩ	C1 to C17
SEG Output Resistance	R_S	I_O = ±10µA	—	—	15	kΩ	S1 to S80
Supply Current 1	I_{DD1}	*1	—	25	50	µA	—
Supply Current 2	I_{DD2}	*2	—	20	40	µA	—
Supply Current 3	I_{DD3}	*3	—	25	50	µA	—
Supply Current 4	I_{DD4}	*4	—	0.5	2	µA	—

*1 f=32.768 kHz ; crystal oscillation
*2 f=32.768 kHz ; external clock
*3 f=76.8 kHz ; external clock
*4 After reset input "L" pulse input or stop command input:

Note: The above values are guaranteed when the IC chip is not exposed to light.

DC Characteristics (2)

(V_{DD} = 0V, V_{SS} = −3V, Ta = 25°C)

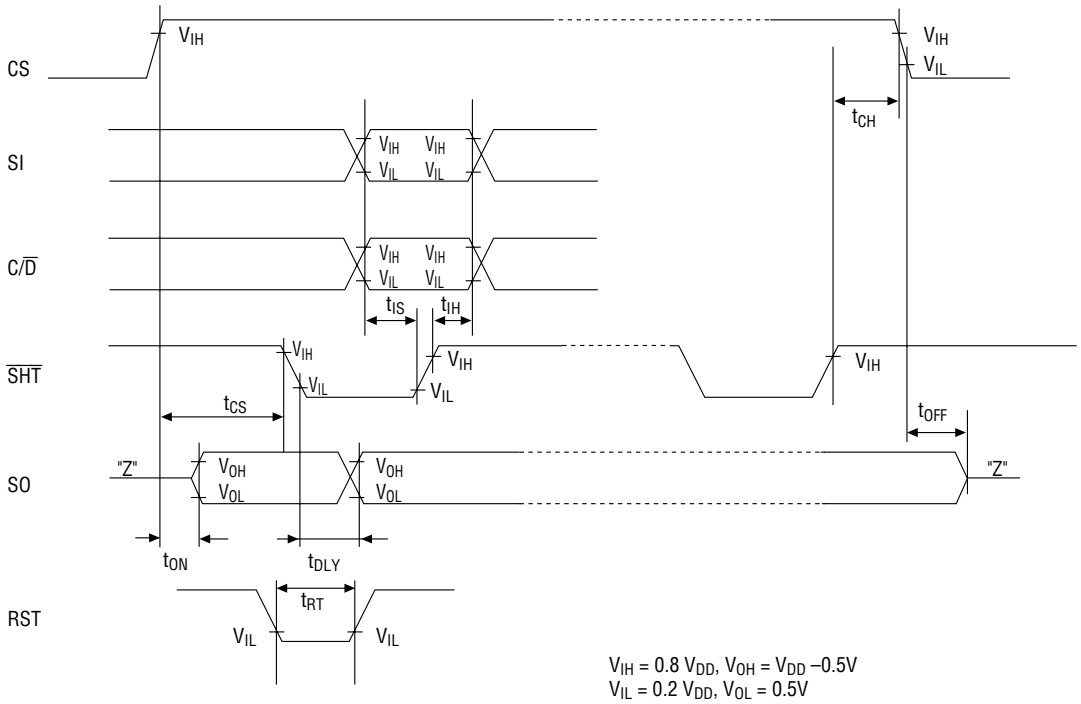
Parameter	Symbol	Condition (Note)	Min.	Typ.	Max.	Unit	Applicable pin
Bias Voltage 1	V_{SS1}	$V_{SS2, 3}$ = −2.0V	−1.1	−1.0	−0.9	V	V_{SS1}
Bias Voltage 2, 3	$V_{SS2, 3}$	N1 = "H", N2 = "L" contrast = "1"	−2.5	−2.15	−1.7	V	$V_{SS2, 3}$
Bias Voltage 4	V_{SS4}	$V_{SS2, 3}$ = −2.0V	−3.1	−3.0	−2.9	V	V_{SS4}
Bias Voltage 5	V_{SS5}	$V_{SS2, 3}$ = −2.0V	−4.2	−4.0	−3.8	V	V_{SS5}

Notes: 1. Connect a 0.1 µF capacitor to the LCD bias generator and the voltage doubler.
2. The above values are guaranteed when the IC chip is not exposed to light.

Switching Characteristics

(V_{DD} – V_{SS} = 3V ±10%, Ta = –10 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS Setup Time	t_{CS}	—	300	—	ns
CS Hold Time	t_{CH}	—	200	—	ns
SO ON Delay Time	t_{ON}	—	—	200	ns
SO OFF Delay Time	t_{OFF}	—	0	200	ns
SO Output Delay Time	t_{DLY}	—	0	200	ns
Input Setup Time	t_{IS}	C_L = 45pF	200	—	ns
Input Hold Time	t_{IH}	—	200	—	ns
Waveform Rise/Fall Time	t_r, t_f	All inputs	—	50	ns
Reset Pulse Input Pulse Width	t_{RT}	—	5	—	µs



V_{IH} = 0.8 V_{DD}, V_{OH} = V_{DD} –0.5V
V_{IL} = 0.2 V_{DD}, V_{OL} = 0.5V

FUNCTIONAL DESCRIPTION

Pin Functional Description

- SI (Serial Input)

  This is an input pin used to input the command and display data serially in the 8-bit unit, where "H" is defined as 1 and "L" is as 0. When the CS pin is at "H" level, command or display data is read by the rising edge of $\overline{SHT}$. Whether the input data is command or display data is determined by the setting of the C/$\overline{D}$ at the 8th rising edge of the $\overline{SHT}$. The input data is command when C/$\overline{D}$ = "H", and is display data when C/$\overline{D}$ = "L".

- C/$\overline{D}$ (Command/$\overline{Data}$)

  This is an input pin used to determine whether the data input into the SI pin is command or display data. It is read at the 8th rising edge of the $\overline{SHT}$. The input data is command when C/$\overline{D}$ = "H", and is display data when C/$\overline{D}$ = "L".

- $\overline{SHT}$ ($\overline{Shift\ Clock}$)

  This is a read clock for SI input and C/$\overline{D}$ input, which are read at the rising edge of $\overline{SHT}$. Reading completes in 8 clocks. Maintain this $\overline{SHT}$ pin at "H" when there is no command and data input from the SI pin. Input during the busy condition will result in operation errors. It is valid when the CS pin is at "H".

- SO (Serial Out)

  This is a busy/non-busy and display data serial read-out pin, where "H" is defined as 1 and "L" is as 0. It is output when CS = "H" and the Serial Out Enable is set by the command, while high impedance occurs otherwise.

  The busy/non-busy signal is output when CS input is at the "H" level. The "H" represents the non-busy state while "L" denotes the busy state. The busy state occurs after the 8th rising edge of the $\overline{SHT}$, and the state is automatically shifted to the non-busy state after the lapse of a specified time.

  Furthermore, the display data is output synchronously with the falling edge of the $\overline{SHT}$.

- CS (Chip Select)

  This is a chip select pin, where "H" represents the Select and "L" the Non-select. "L" input causes the SO pin to be opened, and the $\overline{SHT}$ pin corresponds to "H" inside the IC. For the SI, C/$\overline{D}$, $\overline{SHT}$, SO and CS, see "I/O Procedure".

- $\overline{RST}$ ($\overline{Reset}$)

  Input of "L" level pulse into this pin will suspend the oscillation to prevent the breakthrough current in the oscillation phase, and the Common and Segment outputs is set to the reset state where V_{DD} level is output. This reset state can be released only by command input. (See STOP command.) Furthermore, contrast control will be the minimum in the combination of N2 and N1.

  Setting this pin to "L" level during the command execution will cause operation errors. When power is turned on, the $\overline{RST}$ pin must be set to "L". This pin is based on direct input reset method. Current consumption is 5 to 10 µA during the process of "L" input, so fixed "L" input must not be set.

- 9D/$\overline{17D}$ (1/9Duty/$\overline{1/17Duty}$)
  This is a duty setting pin where "H" is defined as 1/9 duty and "L" as 1/17 duty. Select the level in conformity to the panel used.
  In the case of 1/17 duty, the Common outputs C10 to C16 must be kept open.

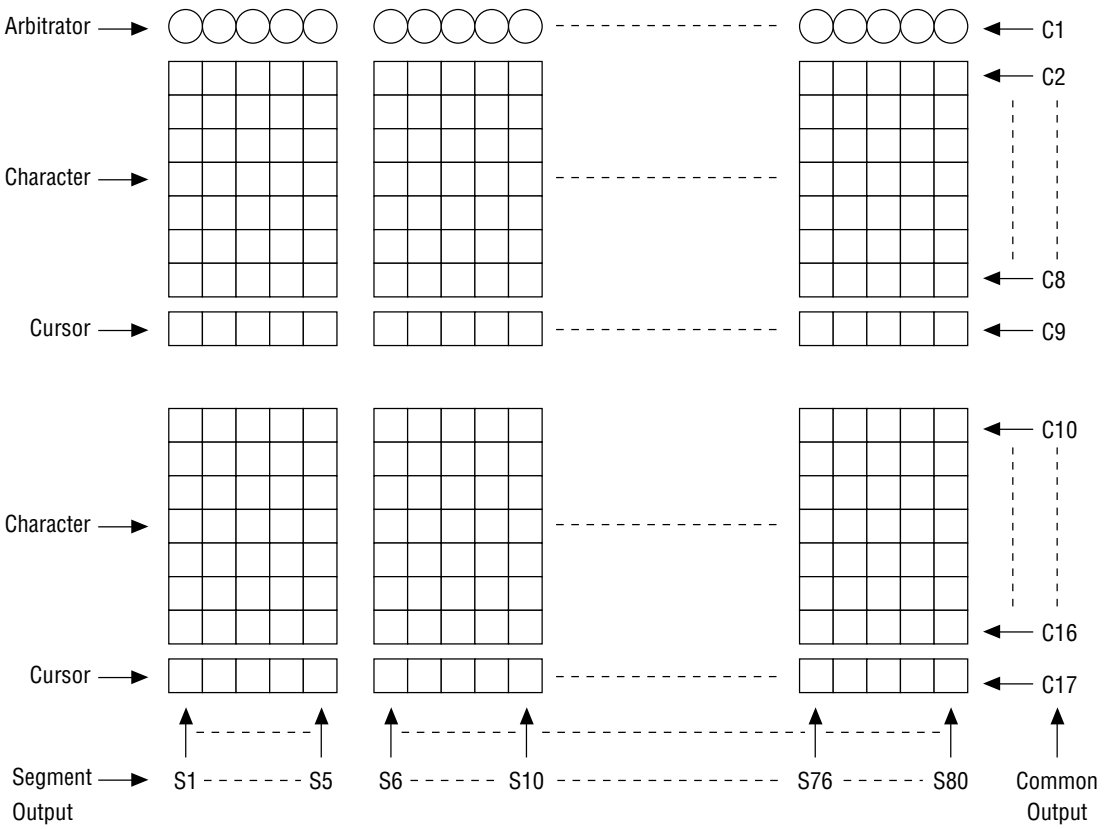
- 32K/$\overline{EXT}$ (32K x'tal osc/$\overline{External\ clock}$)
  This is an input pin used to set up the type of logic source oscillation.
  32K/$\overline{EXT}$ = "H" : In this setting, 32.768 kHz is used for source oscillation frequency. The oscillation feedback resistor (approx. 4 MΩ) is formed in the IC, and the external 32.768 kHz crystal and oscillating capacitors are connected to the XT and $\overline{XT}$, thereby forming the oscillator circuit. When the source oscillation clock is input from outside, it is put into the XT, and $\overline{XT}$ is kept open.
  32K/$\overline{EXT}$ = "L" : This is used to input the source oscillation clock of about n-th power (n=1 to 4) of 2 of 32kHz.
  Conforming to the command SF setting, the external source oscillation frequency is divided into 1/2 to 1/16 in the IC and is used as source oscillation frequency in the IC. The $\overline{XT}$ is kept open. → See SF command.

- TEST
  This is a pin used for test in our company. This pin is kept open for the user.

- XT, $\overline{XT}$
  These are pins for 32.768 kHz crystal-controlled oscillator circuit formation and external source oscillation input. $\overline{XT}$ is kept open, when the souce oscillation clock is input from outside.

- C1 to C17, S1 to S80 (COMMON 1 to 17, SEGMENT 1 to 80)
  These are output pins connected to the LCD panel. Alternation is provided by reserving the frame. During the 1/9 duty operation, C1 to C9 are used with C10 to C17 kept open.
  → See "Relation between Display Screen and Common and Segment Outputs".

- V_{C1}, V_{CC1}
  These are pins to connect the capacitor to double the battery voltage. They are connected with the capacitor of 0.1 µF.



Relation between Display Screen and Common and Segment Outputs

- V_{SS6}
  This is a pin to connect the capacitor to store the doubled voltage. The capacitor of 0.1 µF or more is connected between this pin and V_{DD}.

- $V_{SS2, 3}$
  This is power pin to be used after the doubled voltage has passed through the regulator. They provide the reference voltage used in the LCD bias voltage generator. The capacitor of 0.1 µF is connected between this pin and V_{DD} for electric charge distribution among capacitors and voltage stabilization during generation of various types of LCD bias voltage.

- V_{C2}, V_{CC2}
  These pins are used to connect the capacitors for electric charge distribution to generate LCD bias voltage with reference to $V_{SS2, 3}$.
  They are connected with the capacitor of 0.1 µF.

- V_{SS1}, V_{SS4}, V_{SS5}

  Connect a capacitor of 0.1 µF between these pins and V_{DD} for electric charge distribution and voltage stabilization concerning the capacitor of $V_{SS2, 3}$ during generation of various types of LCD bias voltage.

  The logical value for LCD bias voltage is as shown below.

  Highest voltage : V_{DD}
  $V_{SS1} = V_{SS2, 3}/2$
  $V_{SS2, 3}$
  $V_{SS4} = V_{SS2, 3} + V_{SS2, 3}/2$
  Lowest voltage : $V_{SS5} = V_{SS2, 3} + V_{SS2, 3}/2 + V_{SS2, 3}/2$

  → This is 1/4 bias, which is common to 1/9 duty and 1/17 duty.

- N1, N2

  These are input pins used to determine the voltage of $V_{SS2, 3}$ in combination with the Contrast Up/Down command.

N2	N1	Command contrast control range
L	L	0 to 7
L	H	1 to 8
H	L	2 to 9
H	H	3 to A

- V_{DD}, V_{SS}

  These are pins used to connect the V_{DD} to the positive pin of the battery, and the V_{SS} to the negative pin of the battery.

Command List

X : Don't Care

No.	Mnemonic	Operation	D								Comment
			7	6	5	4	3	2	1	0	
1	LPA	Load Pointer Address	1	1	A5	A4	A3	A2	A1	A0	• Addresses from 0 to 47
2	LOT	Load Option	1	0	1	1	X	X	I1	I0	• For the functions of I1 and I0, see the next page.
3	SF	Set Frequency	1	0	1	0	X	X	F1	F0	• Setting the source oscillation frequency conditions
4	BKCG 1/0	Bank Change 1/0	1	0	0	X	0	0	0	1/0	• Valid only for 1/19 duty • Switching between display addresses 0 to 15, and 16 and 31
5	CONT U/D	Contrast Up/Down	1	0	0	X	0	0	1	1/0	• V_{LCD} adjustment, 8 stages
6	STOP	Set Stop Mode	1	0	0	X	0	1	0	0	• Released by setting DO = 1 independently of the H/L of the C/D • Oscillation suspension and DISPOFF instruction
7	SOE/D	Serial Out Enable/Disable	1	0	0	X	0	1	1	1/0	• Switching output and high impedance of SO
8	DISP	Display On/Off	1	0	0	X	1	0	0	1/0	• On when DO = 1, and off when DO = 0 • Continued OSC • All COM and SEG are at V_{DD} level when turned off
9	AINC	Address Increment	1	0	0	X	1	X	1	X	• Pointer address is incremented by one • The relative operation with with (I1, I0) is exceptional.
10	WCHB	Write Character Blink	0	X	X	X	0	0	0	X	• Character and arbitrator blinking is controlled. The arbitrator is based on the 5-dot unit. • For the arbitrator, blink setting is accepted even if all 5 dots are displayed in blinks, but blinking does not occur.
11	CCHB	Clear Character Blink	0	X	X	X	0	0	1	X	
12	WCS	Write Cursor	0	X	X	X	0	1	0	X	• Cursor on
13	CCS	Clear Cursor	0	X	X	X	0	1	1	X	• Cursor off
14	WCSB	Write Cursor Blink	0	X	X	X	1	0	0	X	• Cursor blinking is controlled. If the cursor display not specified, blink setting is accepted, but blinking does not occur.
15	CCSB	Clear Cursor Blink	0	X	X	X	1	0	1	X	
16	WCCB	Write Character Cursor Blink	0	X	X	X	1	1	0	X	• WCHB + WCSB
17	CCCB	Clear Character Cursor Blink	0	X	X	X	1	1	1	X	• CCHB + CCSB

Note: 1. Commands number 1 to 8, do not affect pointer address.
2. When commands from 9 to 17 and display code data are input, the pointer address is automatically incremented by one (1).

LOT command function list

I1	I0	Function	Comment
0	0	Operation is cancelled (No operation)	—
0	1	Hereafter, equivalent to writing blank code at each AINC execution	Used to mechanical RAM clear when power is turned on
1	0	Hereafter, cursor off and blink-cancellation are carried out at each AINC execution	
1	1	Both of above two operations are indicated	

Command Description

[D7, D6, D5, D4, D3, D2, D1, D0] X = Don't care

• LPA (Load Pointer Address)
[1, 1, A5, A4, A3, A2, A1, A0]
This is a command to set up the address for the address pointer to specify the address subjected to command execution and address for display data input.

• LOT (Load Option)
[1, 0, 1, 1, X, X, I1, I0]
This is a command to process the display of the current address in conformity to execution of the AINC command. The I1 and I0 of the command are used to assign the definition.

I1 = 1 : Cancellation of cursor and stop of character and cursor blinking for each AINC execution
0 : Cancellation of above definition

I0 = 1 : The blank code is set up for each AINC execution and the display is turned off. When the current address is an arbitrator, all five dots are turned off.
0 : Cancellation of above definition

I1 and I0 can be set independently of each other.

• SF (Set Frequency)
[1, 0, 1, 0, X, X, F1, FO]
This command sets up the number of divisions to be applied the source oscillation frequency to be input from the XT in order to get the source oscillation inside the IC. This is valid when 32 K/$\overline{\text{EXT}}$ pin = "L". The following table lists the source frequencies inside the IC.

F1	F0	Source frequency inside IC
0	0	XT/2
0	1	XT/4
1	0	XT/8
1	1	XT/16

The following shows the blinking frequency:

32 K/$\overline{\text{EXT}}$ = "H" : The blinking frequency is 1 Hz when 32.768 kHz is input. When another frequency is input, the blinking frequency is proportionate to that frequency.

32 K/$\overline{\text{EXT}}$ = "L" :
If (F1, F0) = (0, 0):
The blinking frequency is 1 Hz when 76.8 kHz is input. When another frequency is input, the blinking frequency is proportionate to that frequency.

If (F1, F0) = (0, 1), (1, 0), (1, 1) the blinking frequency will be as follows:

$$1\ \text{Hz} \times 32.768\ \text{kHz} / A$$

A = XT input frequency/source frequency inside IC

The following shows the frame frequency:

When 32 K/$\overline{\text{EXT}}$ = "H", and 32.768 kHz input is assumed, we get the following:

approximately 65 Hz in the case of 1/9 duty

approximately 68.8 Hz in the case of 1/17 duty

When another frequency is input, the blinking frequency is proportionate to that frequency.

When 32 K/$\overline{\text{EXT}}$ = "L", the frame frequency is in proportion to the IC internal source oscillation set up by (F0, F1) with reference to the IC internal source oscillation of 32.768 kHz.

- BKCG1/0 (Bank Change 1/0)

  [1, 0, 0, X, 0, 0, 0, 1/0]

  This command is valid only for 1/9 duty display, and provides switching (BANK switching) of the display address group. When "0" is set, display addresses are in the range from 0 to 15 and from 32 to 47. When "1" is set, display addresses are in the range from 16 to 31 and from 32 to 47. The command and display data can be set despite BANK setting.

- CONT U/D (Contrast Up/Down)

  [1, 0, 0, X, 0, 0, 1, 1/0]

  This is a command to select the voltage $V_{SS2, 3}$ serving as bases for LCD. The contrast is changed by changing the voltage $V_{SS2, 3}$.

  The contrast is controlled by the value on the up/down three-bit counter and is available in 8 stages. The up/down counter counts up the number when "1" is input by this command, while it counts down the number when "0" is input by this command. Counting is carried out in a loop from "0" to "7". The counter execution values change from 1 to 8, from 2 to 9 and from 3 to A by setting the N2 and N1.

  Example : ...⇔6⇔7⇔0⇔1⇔2⇔3⇔4⇔5⇔6⇔7⇔0⇔...

- STOP (Set Stop Mode)

  [1, 0, 0, X, 0, 1, 0, 0]

  The oscillation stage is stopped to prevent breakthrough current in the oscillation stage. At the same time, V_{DD} level is output to all pins of LCD output to start the standby mode. The standby mode is released when D0 = 1 is set by serial input, independently of C/$\overline{\text{D}}$ input setting.

  When D0 = 1 command or data is input, this command or data is executed and input, and the standby mode is also released.

- SOE/D (Serial Out Enable/Disable)

  [1, 0, 0, X, 0, 1, 1, 1/0]

  This is a command to control the impedance of SO output pin. When "1" is set, the display data is output from the SO pin. When "0" is set, the SO pin becomes a high impedance.

• DISP (Display On/Off)
[1, 0, 0, X, 1, 0, 0, 1/0]
This is a control command to turn on and off the LCD panel display. The display turns on when "1" is set, and turns off when "0" is set. When it turns off, the V_{DD} level is output to both Common and Segment pins. It should be noted, however, that oscillation is not stopped even when the display is set to the off position.

• AINC (Address Increment)
[1, 0, 0, X, 1, X, 1, X]
This is a command to increment the address pointer value by one. The value is incremented by one every time this command is input. Furthermore, processing specified by the LOT command is applied to the address denoted by the address pointer value before it is incremented by one every time this command is input.

• WCHB (Write Character Blink)
[1, X, X, X, 0, 0, 0, X]
This is a command to specify the character and arbitrator blinking. This is done to the address denoted by the address pointer. In the case of characters, blinking alternates between all-display-off state (35 dots) and character display state. In the case of arbitrator, only the On-bit alternates between the display on/off states. Arbitrator blinking control is made in the 5-dot unit.

• CCHB (Clear Character Blink)
[0, X, X, X, 0, 0, 1, X]
This is a command to cancel the blinking of characters and arbitrators, and is done to the address indicated by the address pointer.

• WCS (Write Cursor)
[0, X, X, X, 0, 1, 0, X]
This is a command to turn on the cursor, and is done to the address indicated by the address pointer.

• CCS (Clear Cursor)
[0, X, X, X, 0, 1, 1, X]
This is a command to turn off the cursor, and is done to the address indicated by the address pointer.

• WCSB (Write Cursor Blink)
[0, X, X, X, 1, 0, 0, X]
This is a command to blink the cursor, and is done to the address indicated by the address pointer. It should be noted, however, that blinking does not occur to the address where cursor display is not specified. Blinking starts when the cursor display is specified.

• CCSB (Clear Cursor Blink)
[0, X, X, X, 1, 0, 1, X]
This is a command to cancel cursor blinking, and is done to the address indicated by the address pointer. It can be set to the address where cursor display is not specified.

• WCCB (Write Character Cursor Blink)
[0, X, X, X, 1, 1, 0, X]
This is a command to execute both the WCHB and WCSB commands.

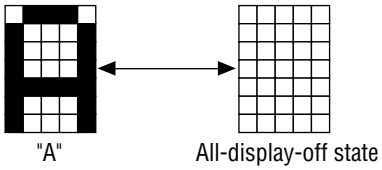
• CCCB (Clear Character Cursor Blink)
[0, X, X, X, 1, 1, 1, X]
This is a command to execute both the CCHB and CCSB commands.

• Address Pointer Increment (+1)
When display data are input and the following command is executed, the address pointer is incremented by one:

AINC, WCHB, CCHB, WCS, CCS, WCSB, CCSB, WCCB and CCCB

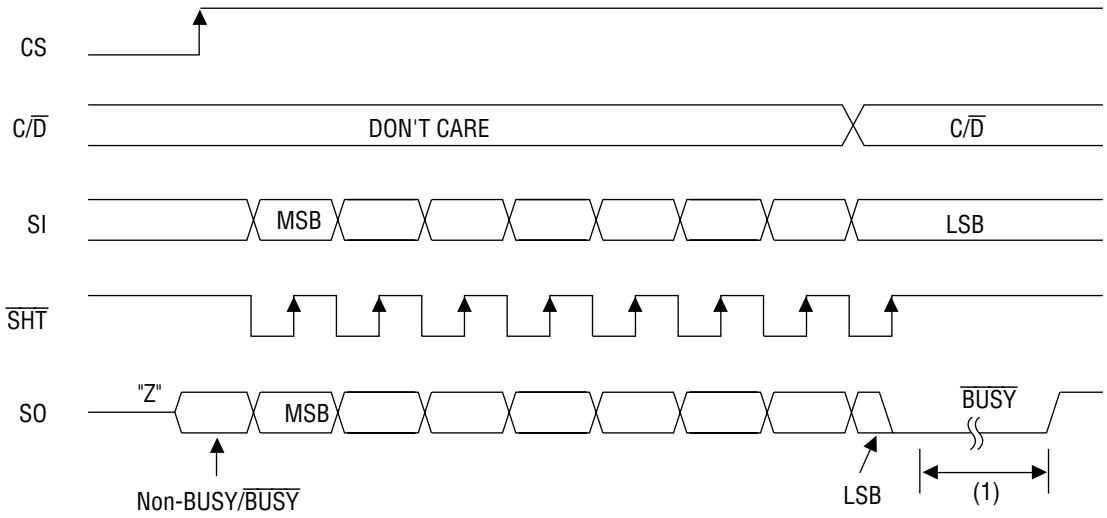
• Character Blink Method
The character on-state alternates with the character dot all-display-off state, as illustrated below:

Example of blinking (Character "A")



I/O Procedure

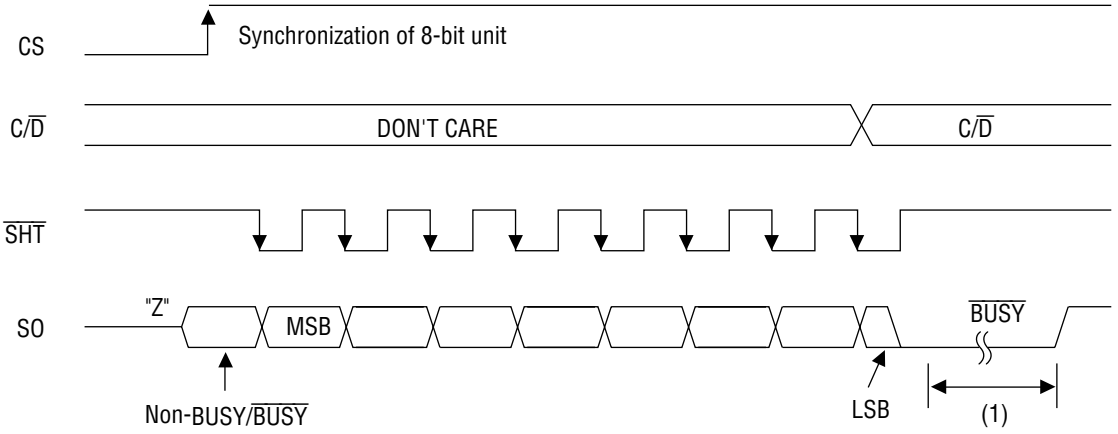
• Input timing (command input, display code and data input)



(1) Max 2 × {COMMON 1-line display time}

Starting of the CS provides input synchronization in the 8-bit unit. Subsequent CS rising edge is not necessary if the 8-bit unit is maintained.

• Output timing (display code and data read)
If the SOE command has already been input, the code or the arbitrator data of the address currently indicated by the address pointer is output from SO pin.

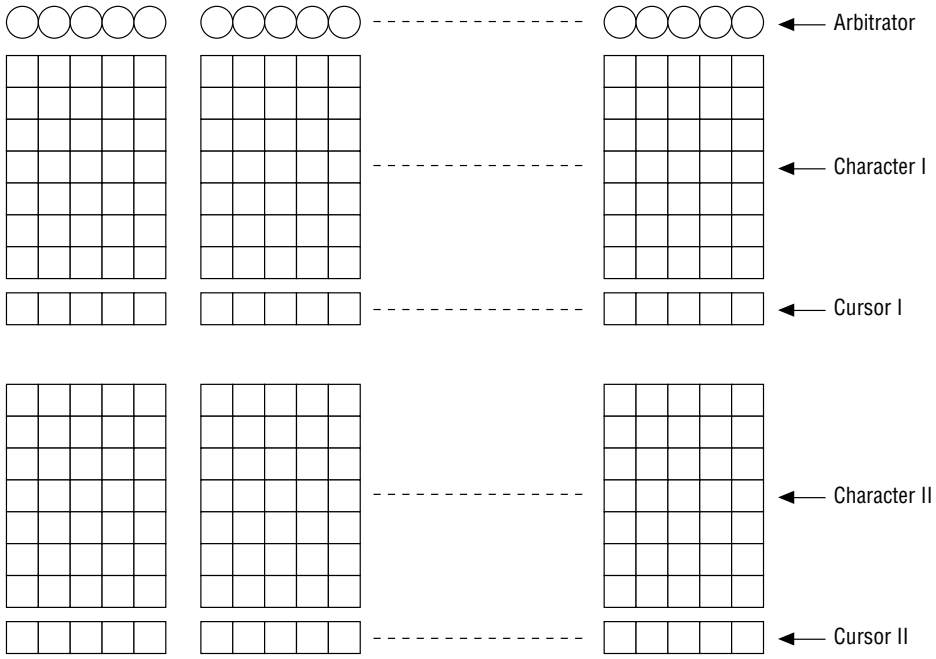


(1) Max 2 × {COMMON 1-line display time}

Note: If CS is set to "L" and is again set to "H" without completion of read-out 8 bits, the previous uncompleted portion will be output continuously, the extra read-out data will be "0".

Display Screen and Memory Address

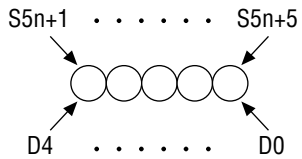
Display



RAM Map

32	33		47	← Arbitrator
0	1		15	← Character I
0	1		15	← Cursor I
16	17		31	← Character II
16	17		31	← Cursor II

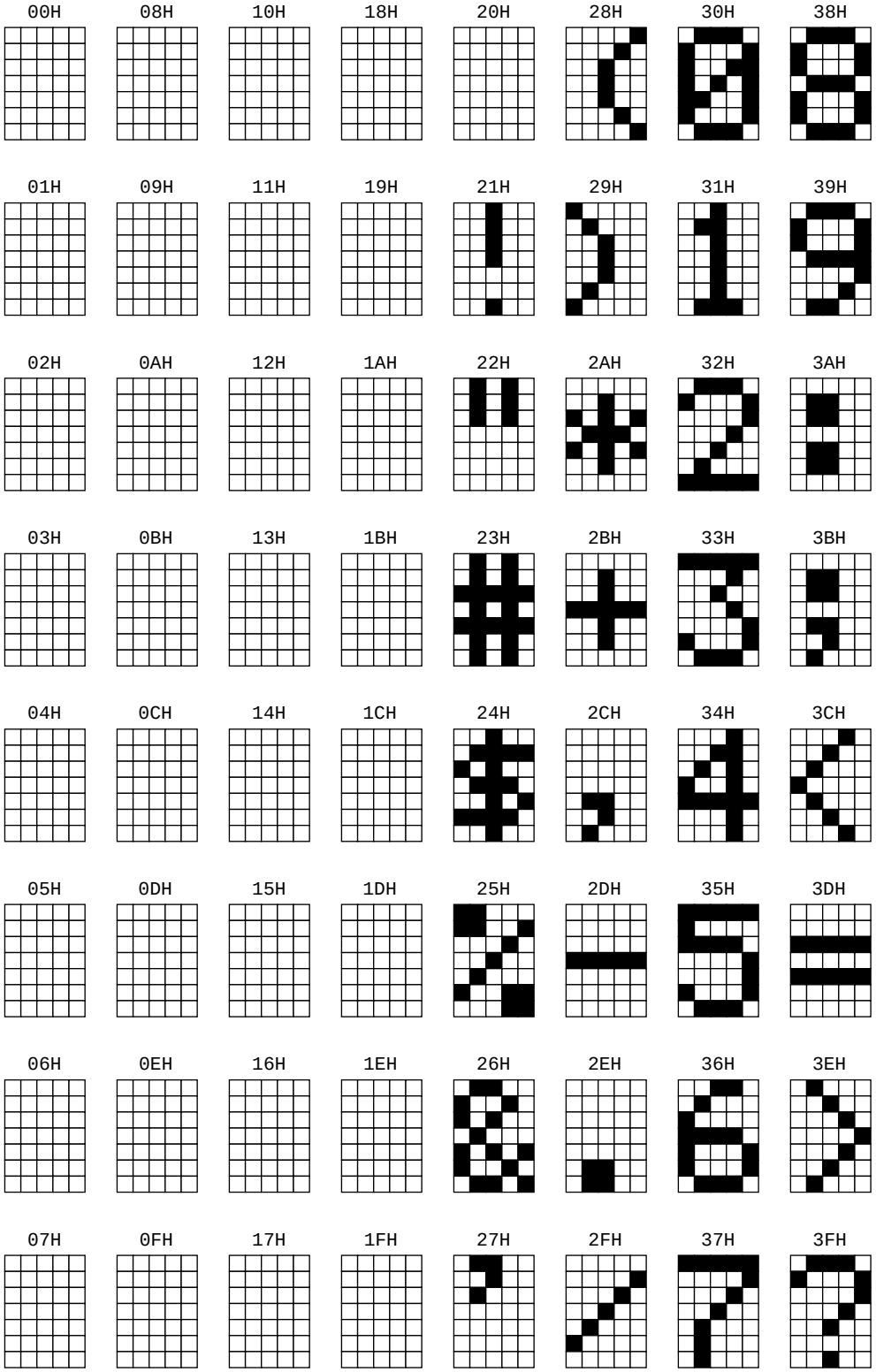
Note: Characters are input by codes. Arbitrators are displayed independently of the CG ROM. The following shows the relationship between the input data and display of Arbitrators:

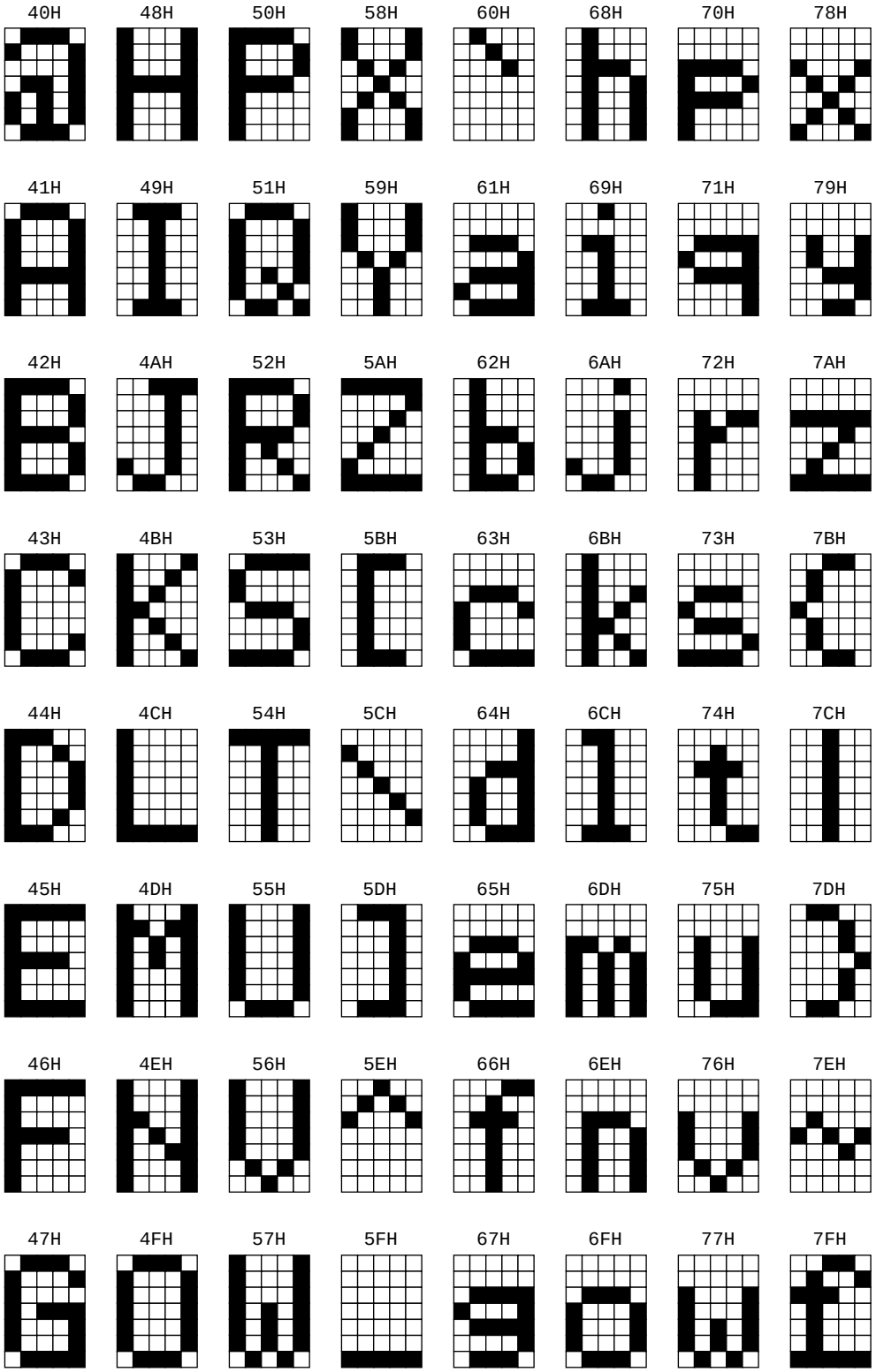


S: Segment
n: 0 to 15

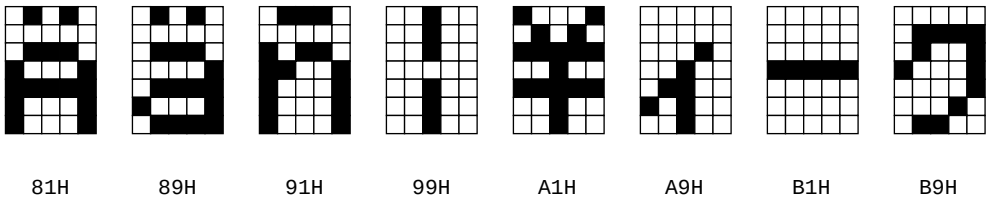
Serial input data from D7 to D5 require dummy input.
Either "1" or "0" may be used for input data from D7 to D5.

Code and Character Font of MSM6555B-02

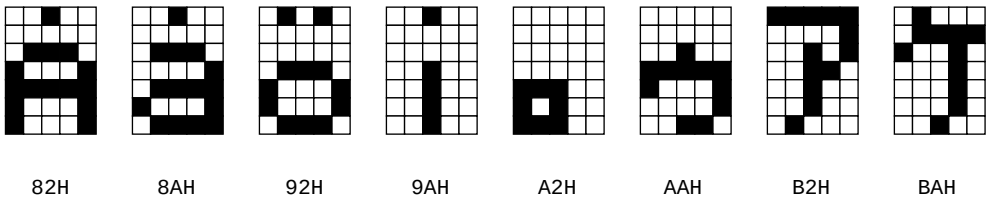




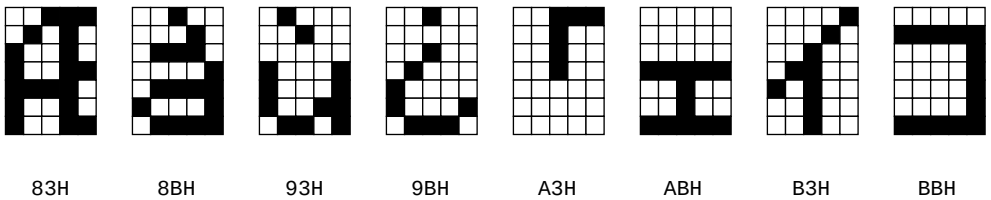
80H 88H 90H 98H A0H A8H B0H B8H



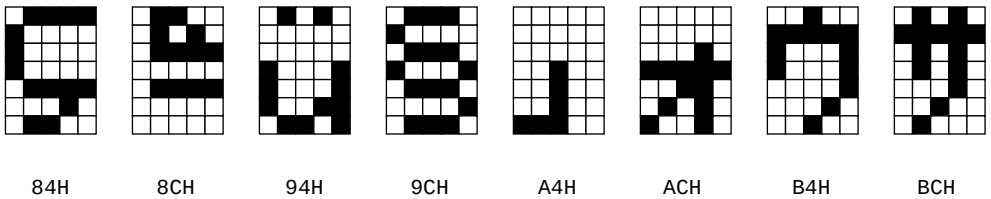
81H 89H 91H 99H A1H A9H B1H B9H



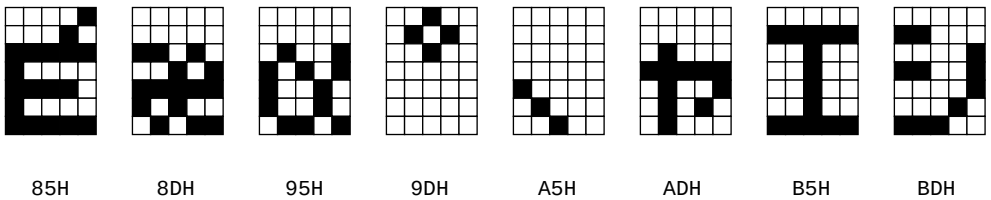
82H 8AH 92H 9AH A2H AAH B2H BAH



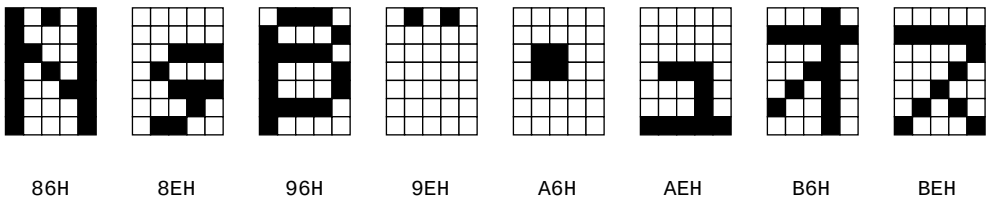
83H 8BH 93H 9BH A3H ABH B3H BBH



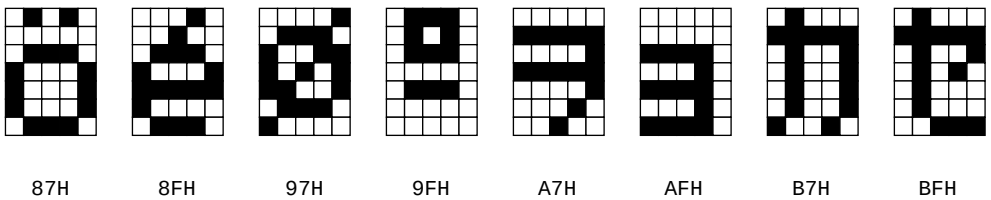
84H 8CH 94H 9CH A4H ACH B4H BCH



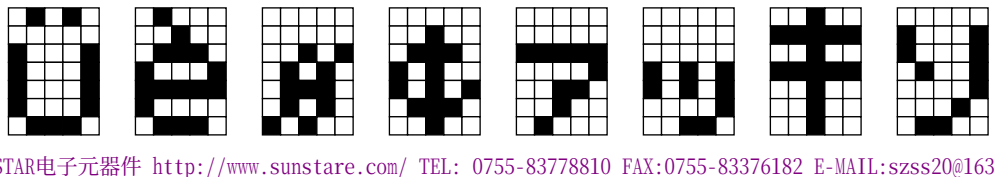
85H 8DH 95H 9DH A5H ADH B5H BDH



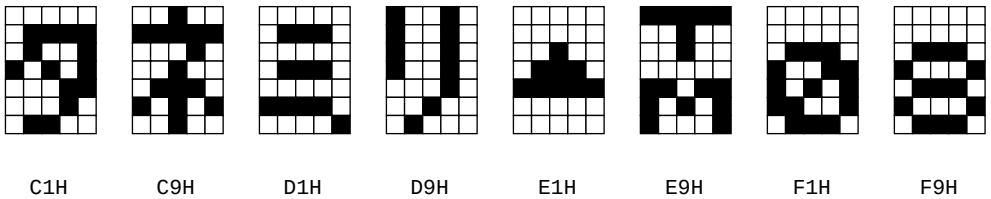
86H 8EH 96H 9EH A6H AEH B6H BEH



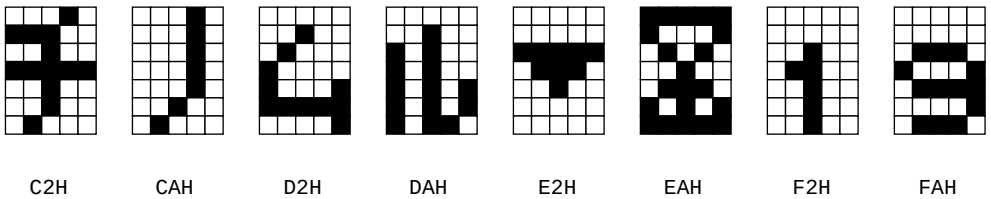
87H 8FH 97H 9FH A7H AFH B7H BFH



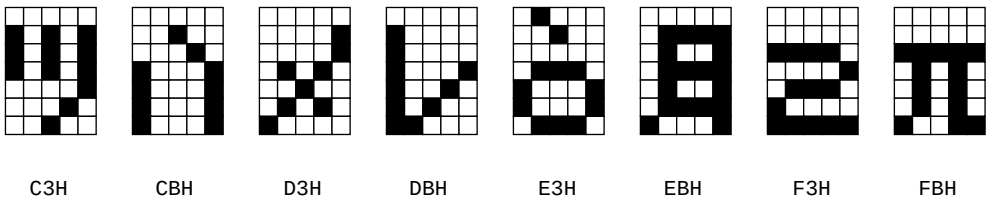
C0H C8H D0H D8H E0H E8H F0H F8H



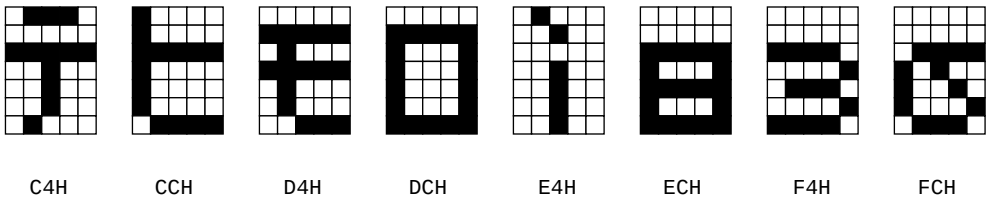
C1H C9H D1H D9H E1H E9H F1H F9H



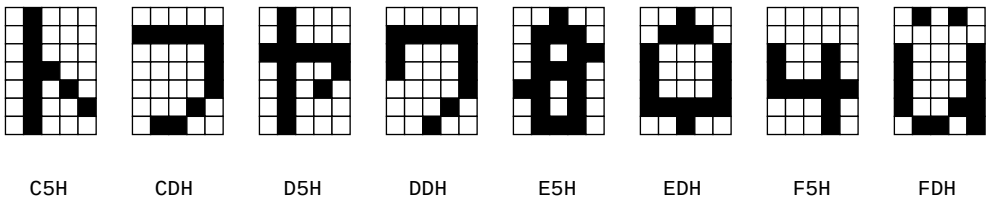
C2H CAH D2H DAH E2H EAH F2H FAH



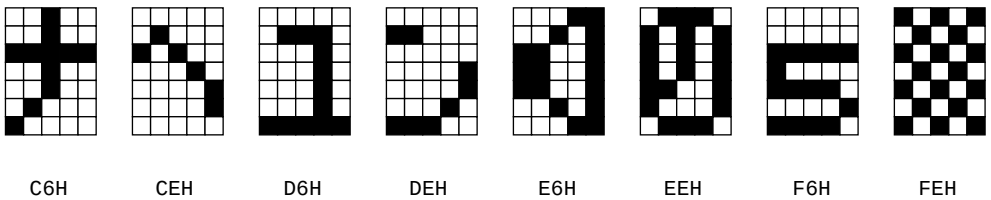
C3H CBH D3H DBH E3H EBH F3H FBH



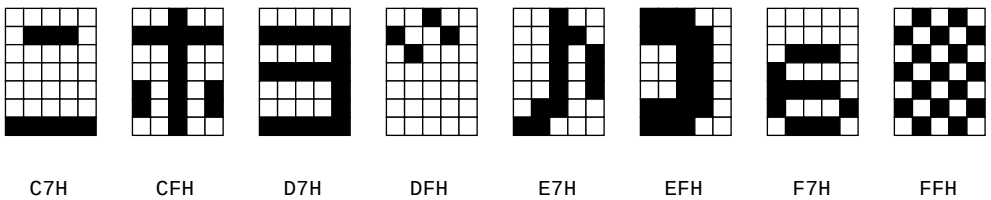
C4H CCH D4H DCH E4H ECH F4H FCH



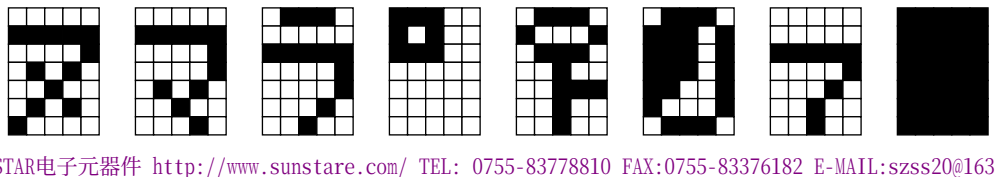
C5H CDH D5H DDH E5H EDH F5H FDH



C6H CEH D6H DEH E6H EEH F6H FEH



C7H CFH D7H DFH E7H EFH F7H FFH



Supplement

(1) Display when power is turned on, and command execution time (for 32K/$\overline{EXT}$ = L)

- When 32K/$\overline{EXT}$ = L, source oscillation is subjected to frequency division inside the IC by the value of (F1, F0), and is utilized for logic operation as a source oscillation inside the IC.
- When power is turned on, (F1, F0) is not stable, and the source oscillation inside the IC uses the range from 1/2 to 1/16 of XT frequency.
- On the other hand, the LCD frame frequency is determined by the ratio of the source oscillation inside the IC to 32.768 kHz.

  Example 1: When XT = 65.536 kHz and (F1, F0) = (0, 0), the source oscillation inside the IC is 32.768 kHz, and frame frequency is as follows:
  approximately 65 Hz in the case of 1/9 duty
  approximately 68.8 Hz in the case of 1/17 duty

  Example 2: When XT = 65.536 kHz and (F1, F0) = (1, 1), the source oscillation inside the IC is 4.096 kHz, and frame frequency is as follows:
  approximately 8.13 Hz in the case of 1/9 duty
  approximately 8.6 Hz in the case of 1/17 duty

- Thus, (F1, F0) must be determined before start of display.
- The command execution time depends on the source oscillation inside the IC. The maximum command execution time corresponds to the display time for two Common lines.
- Thus, the command execution time will be as follows in the case of Examples: 1 and 2:

  Example 1: in the case of 1/17 duty
  Common one-line display time (Ct0)
  (Ct0) = 1 ÷ 68.8 (Hz) ÷ 17 (common) = 855 µs
  Thus, command execution time is Ct0 × 2 = 1710 µs (max.)

  Example 2: in the case of 1/9 duty
  Common one-line display time (Ct0)
  (Ct0) = 1 ÷ 8.13 (Hz) ÷ 9 (common) = 13.67 ms
  Thus, command execution time is Ct0 × 2 = 27.33 ms (max.)

- As described above, command execution time to completion of setting the (F1, F0) after power is turned on from 0 volt (Note: including this SF command execution time) depends on the incidental (F1, F0) value when power is turned on and external source frequency, so it is necessary to calculate the maximum value to reflect the result in software design up to completion of setting the (F1, F0).

(2) Standby mode

The standby mode can be started either by the $\overline{RST}$ pin method or Stop command method.

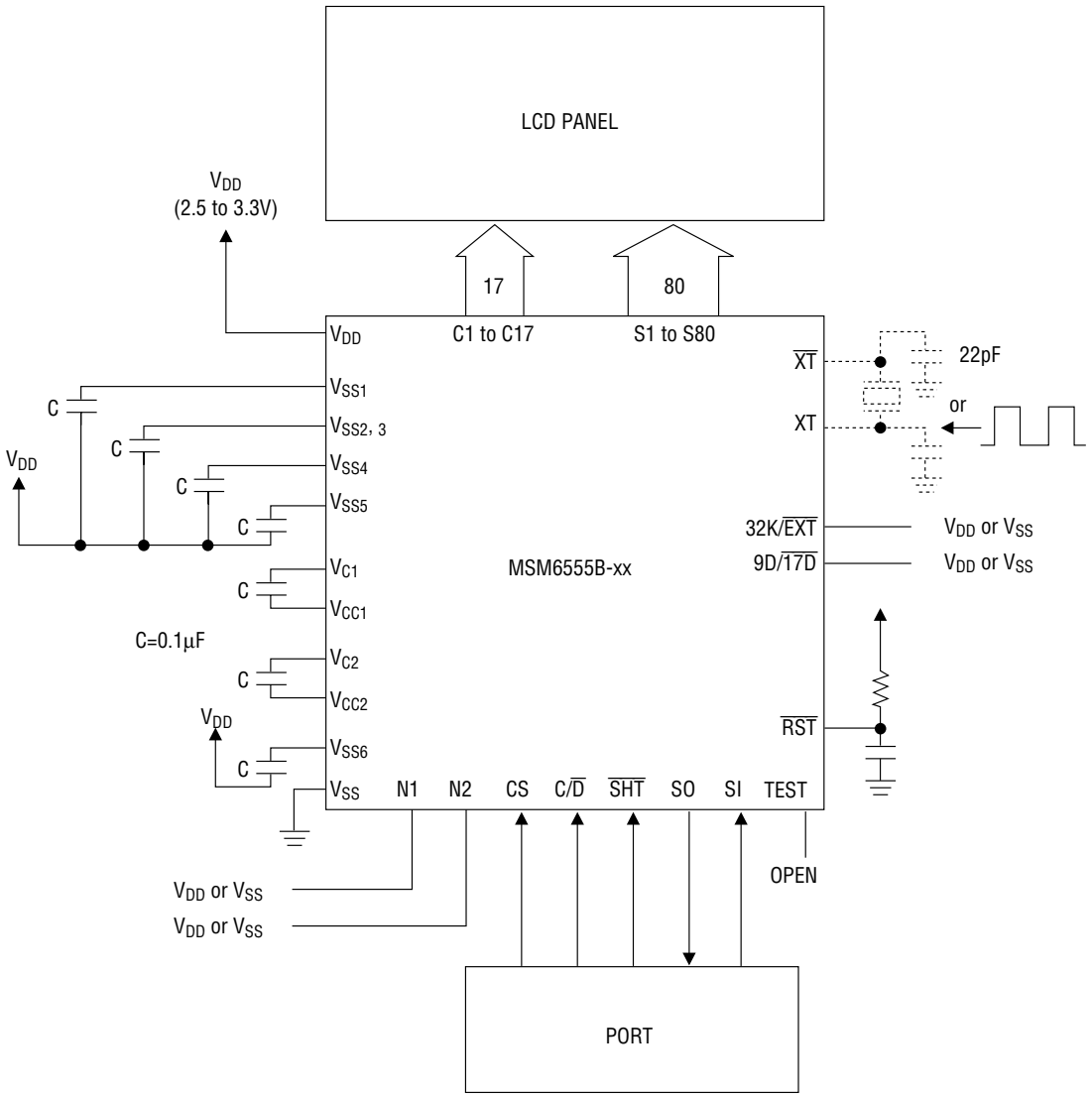
The following shows the difference between the $\overline{RST}$ pin method and Stop command method at the time of resetting:

—	$\overline{RST}$ pin method	Stop command method
Contrast Value	Minimum value in combination of (N1, N2)	Holding of the value before standby mode

For registers except for the above (blink setting, bank switching, etc.), there is no difference between the $\overline{RST}$ pin method and Stop command method; the state before the standby mode is held.

The standby mode is released when D0 = 1 is set by serial input, independently of C/$\overline{D}$ input setting. The command or data input in this case is also valid.

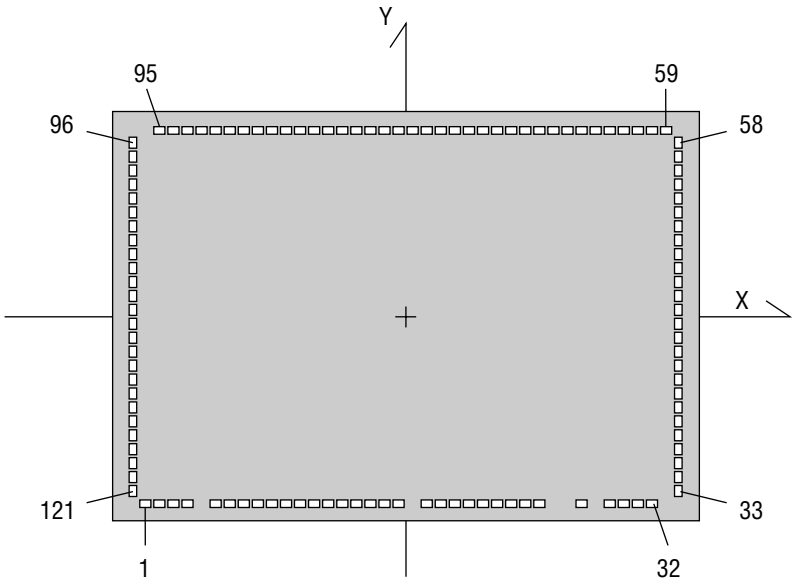
APPLICATION CIRCUITS



PAD CONFIGURATION

Pad Layout

Chip size : 7.16 × 4.96mm



Pad Coordinates

Pad No.	Pad Name	x (μm)	y (μm)
1	S77	–3023	–2325
2	S78	–2857	–2325
3	S79	–2691	–2325
4	S80	–2525	–2325
5	V_{DD}	–2139	–2325
6	SO	–1944	–2325
7	XT	–1764	–2325
8	$\overline{XT}$	–1591	–2325
9	TEST	–1418	–2325
10	32K/$\overline{EXT}$	–1245	–2325
11	$\overline{RST}$	–1072	–2325
12	9D/$\overline{17D}$	–899	–2325
13	$\overline{SHT}$	–726	–2325
14	SI	–553	–2325
15	C/$\overline{D}$	–380	–2325
16	CS	–207	–2325
17	N2	–34	–2325
18	N1	139	–2325
19	V_{SS5}	380	–2325
20	V_{SS4}	560	–2325

Pad No.	Pad Name	x (μm)	y (μm)
21	$V_{SS2, 3}$	740	–2325
22	V_{SS1}	920	–2325
23	V_{CC2}	1100	–2325
24	V_{C2}	1280	–2325
25	V_{CC1}	1460	–2325
26	V_{C1}	1640	–2325
27	V_{SS6}	1820	–2325
28	V_{SS}	2188	–2325
29	C1	2528	–2325
30	C2	2694	–2325
31	C3	2860	–2325
32	C4	3026	–2325
33	C5	3426	–2083
34	C6	3426	–1917
35	C7	3426	–1751
36	C8	3426	–1585
37	C9	3426	–1419
38	C10	3426	–1253
39	C11	3426	–1087
40	C12	3426	–921

Pad No.	Pad Name	x (μm)	y (μm)
41	C13	3426	−755
42	C14	3426	−589
43	C15	3426	−423
44	C16	3426	−257
45	C17	3426	−92
46	S1	3426	75
47	S2	3426	240
48	S3	3426	406
49	S4	3426	572
50	S5	3426	738
51	S6	3426	904
52	S7	3426	1070
53	S8	3426	1236
54	S9	3426	1402
55	S10	3426	1568
56	S11	3426	1734
57	S12	3426	1900
58	S13	3426	2066
59	S14	3027	2325
60	S15	2861	2325
61	S16	2695	2325
62	S17	2529	2325
63	S18	2363	2325
64	S19	2197	2325
65	S20	2031	2325
66	S21	1865	2325
67	S22	1699	2325
68	S23	1533	2325
69	S24	1367	2325
70	S25	1201	2325
71	S26	1035	2325
72	S27	869	2325
73	S28	703	2325
74	S29	537	2325
75	S30	371	2325
76	S31	205	2325
77	S32	39	2325
78	S33	−127	2325
79	S34	−293	2325
80	S35	−459	2325
81	S36	−625	2325
82	S37	−791	2325
83	S38	−957	2325
84	S39	−1123	2325
85	S40	−1289	2325

Pad No.	Pad Name	x (μm)	y (μm)
86	S41	−1455	2325
87	S42	−1621	2325
88	S43	−1787	2325
89	S44	−1953	2325
90	S45	−2119	2325
91	S46	−2285	2325
92	S47	−2451	2325
93	S48	−2617	2325
94	S49	−2783	2325
95	S50	−2949	2325
96	S51	−3426	2066
97	S52	−3426	1900
98	S53	−3426	1734
99	S54	−3426	1568
100	S55	−3426	1402
101	S56	−3426	1236
102	S57	−3426	1070
103	S58	−3426	904
104	S59	−3426	738
105	S60	−3426	572
106	S61	−3426	406
107	S62	−3426	240
108	S63	−3426	75
109	S64	−3426	−92
110	S65	−3426	−257
111	S66	−3426	−423
112	S67	−3426	−589
113	S68	−3426	−755
114	S69	−3426	−921
115	S70	−3426	−1087
116	S71	−3426	−1253
117	S72	−3426	−1419
118	S73	−3426	−1585
119	S74	−3426	−1751
120	S75	−3426	−1917
121	S76	−3426	−2083