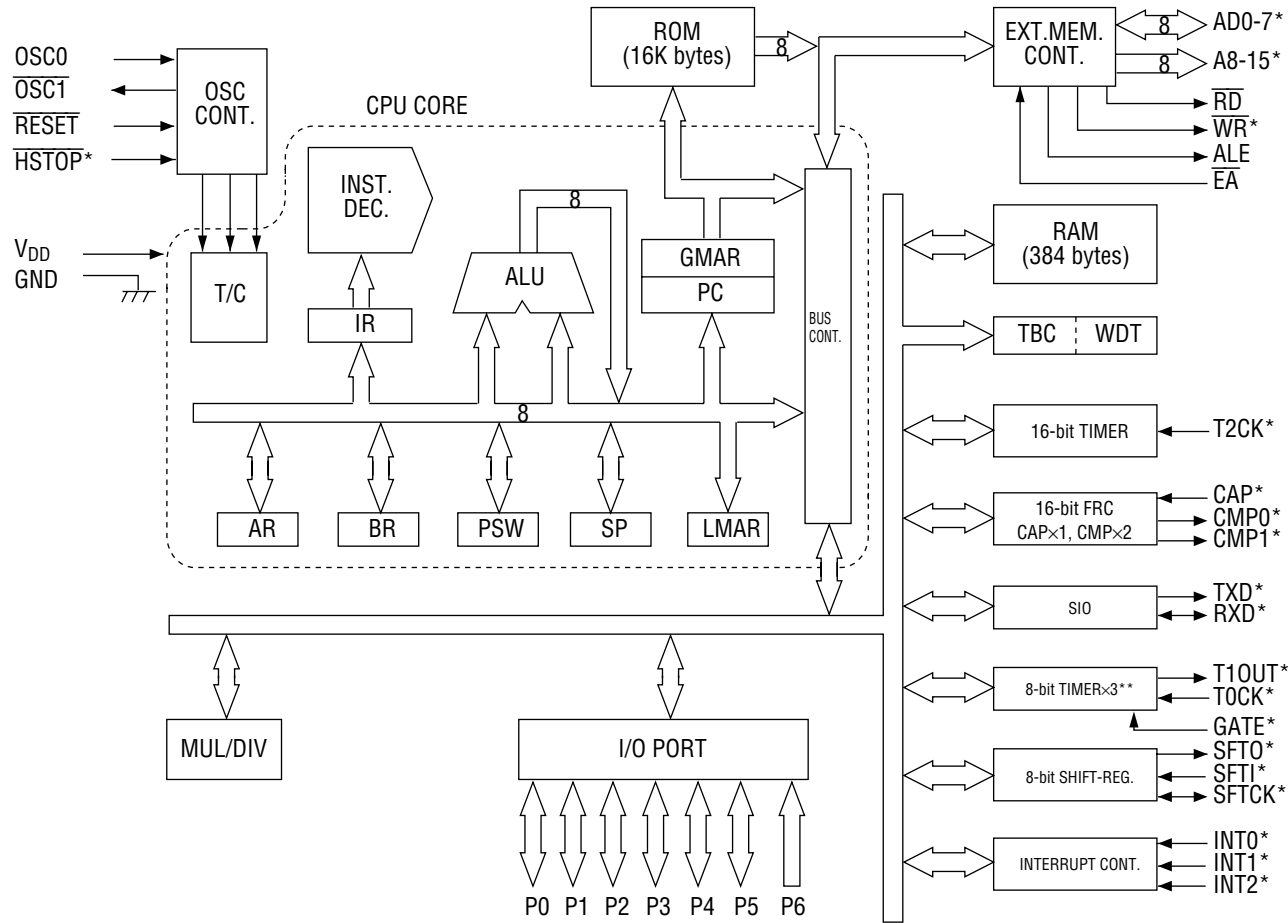


MSM65514/65P514**High Performance 8-Bit Microcontroller****GENERAL DESCRIPTION**

The MSM65514 is a high-performance 8-bit microcontroller that employs OKI original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65514 is capable of high-speed processing, and includes 16K bytes of program memory, 384 bytes of data memory, timers and serial ports on chip. Also available are the MSM65P514, which replaces the on-chip program memory with one-time PROM, and the MSM65X514, which uses external program memory.

FEATURES

- Operating range
 - Operating frequency : 0 to 10MHz ($V_{DD}=4.5$ to 5.5V)
0 to 5MHz ($V_{DD}=2.7$ to 5.5V)
 - Operating voltage : 2.7 to 5.5V
 - Operating temperature : -40 to +85°C
 - Memory space : 64K bytes
 - Internal program memory : 16K bytes
 - Internal data memory : 384 bytes
 - Minimum instruction execution time : 400ns @ 10MHz
 - Powerful instruction set : 83 basic instructions
8/16-bit operation instructions
Bit manipulation instructions
Compound function instructions
 - Abundant addressing modes
 - Multiplication/division operation functions : $8 \times 8 \rightarrow 16$
 $16 \div 8 \rightarrow 16 \dots 8$
 - I/O port
 - Input-output port : 6 ports \times 8 bits
 - Input port : 1 port \times 8 bits
 - Timers : 8-bit auto-reload timer \times 2
16-bit auto-reload timer \times 1
Watchdog timer \times 1
 - Counters : Time base counter \times 1
16-bit free-running counter \times 1
 - Capture input : 1 channel
 - Compare output : 2 channels
 - Serial ports : Shift register \times 1
Serial port with baud rate generator
(UART/synchronous) \times 1
 - External interrupts : 3
 - Interrupt sources : 15
 - Package
 - 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (MSM65514-xxxSS, MSM65P514-xxxSS)
 - 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (MSM65514-xxxGS-BK, MSM65P514-xxxGS-BK)
 - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27): (MSM65514-xxxJS, MSM65P514-xxxJS)
- xxx indicates the code number.

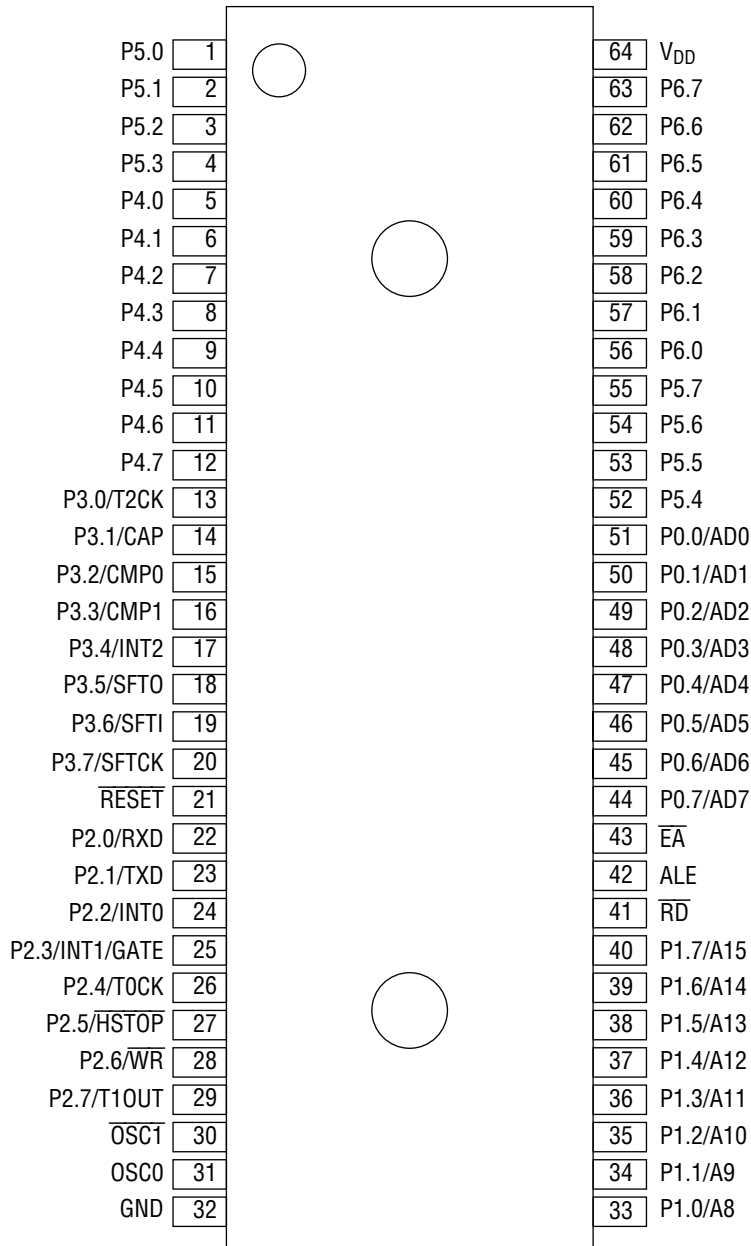


* Secondary functions of ports

** One timer is used for the SIO baud rate generator.

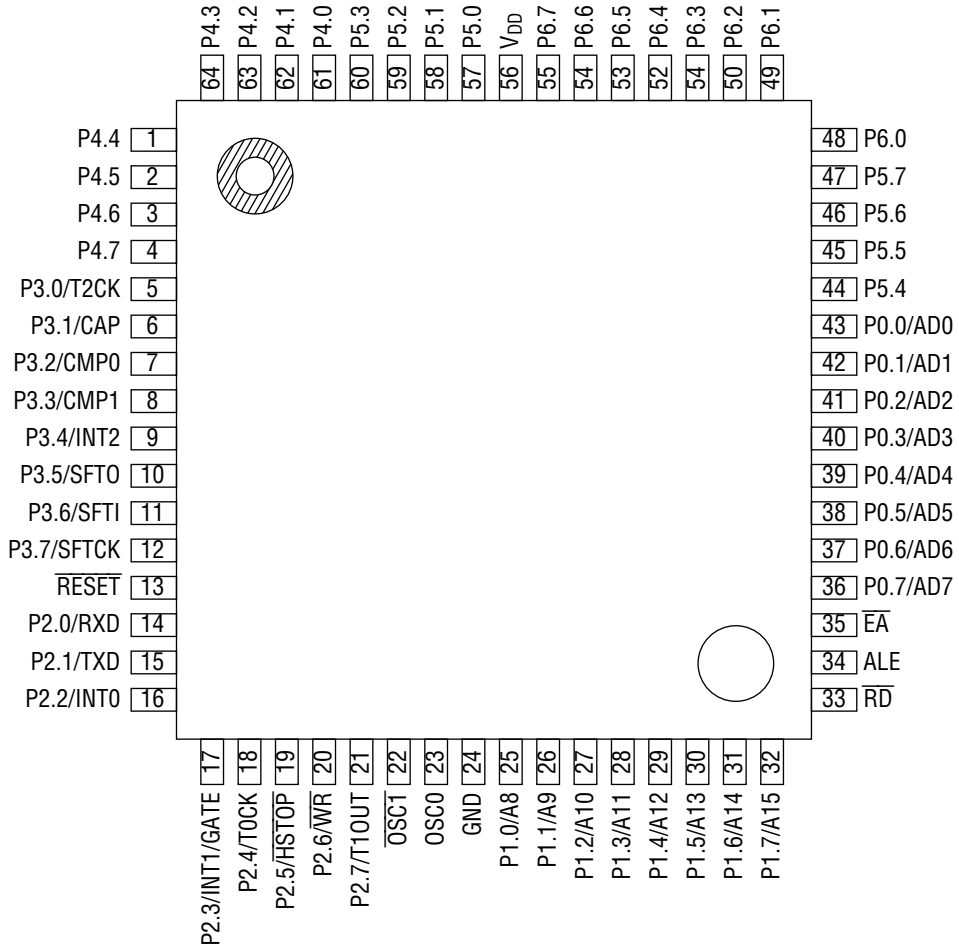
BLOCK DIAGRAM

PIN CONFIGURATION (TOP VIEW)



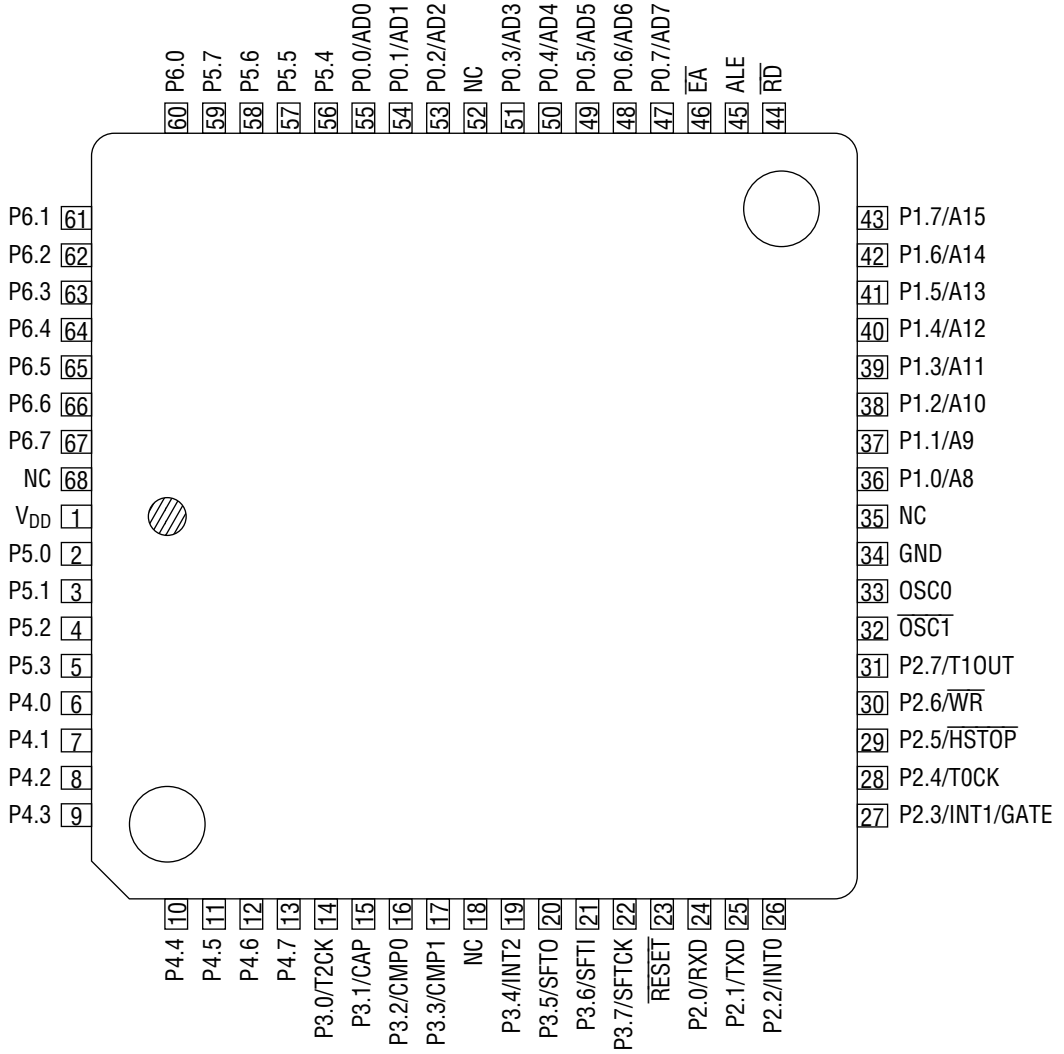
64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC: No-connection pin

68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTION

Basic Functions

Function	Symbol	Type	Description
Power Supply	V _{DD}	—	+5V power supply
	GND	—	0V ground
Oscillation	OSCO	I	System clock input pin. Quartz oscillator or ceramic oscillator is connected between OSC0 and $\overline{\text{OSC1}}$. For external clock, input at OSC0, leaving $\overline{\text{OSC1}}$ open.
	$\overline{\text{OSC1}}$	O	System clock output pin
Control	$\overline{\text{RESET}}$	I	System reset input (program starts from address 0040H); internal pull-up resistance
	$\overline{\text{EA}}$	I	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory.
	$\overline{\text{RD}}$	O	Read strobe signal during external memory access
	ALE	O	Address latch signal during external memory access
Port	PORT 0	I/O	8-bit Input-output port During external memory access, becomes address/data bus for address output, instruction fetch or data read/write along with ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins.
	PORT 1	I/O	8-bit Input-output port Address bus during external memory access
	PORT 2 PORT 3 PORT 4 PORT 5	I/O	8-bit Input-output port × 4. Secondary functions shown in following table are added for ports 2 and 3.
	PORT 6	I	8-bit Input port

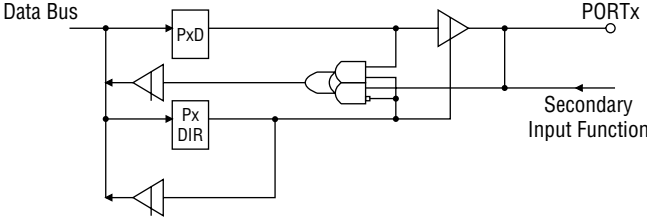

Secondary Functions

Symbol	Type	Description
RXD	I/O	P2.0 secondary function UART: Input pin for serial port receive data. Synchronous: Input/output pin for serial port transmit/receive data.
TXD	0	P2.1 secondary function UART: Output pin for serial port transmit data. Synchronous: Output pin for serial port synchronizing clock.
INT0	I	P2.2 secondary function External interrupt 0 input pin.
INT1/GATE	I	P2.3 secondary functions External interrupt 1 input pin. Also used as input pin for gate signal for timer 0 count enable/disable.
T0CK	I	P2.4 secondary function Timer 0 external clock input pin.
$\overline{\text{HSTOP}}$	I	P2.5 secondary function Hard stop mode input pin; stops system clock oscillation with "L" level input.
$\overline{\text{WR}}$	0	P2.6 secondary function Write strobe signal output pin during external data memory access.
T1OUT	0	P2.7 secondary function Output pin for signal that 2-divided timer 1 overflow.
T2CK	I	P3.0 secondary function Timer 2 external clock input pin.
CAP	I	P3.1 secondary function Capture trigger input pin.
CMP0	0	P3.2 secondary function Compare output channel 0 output pin.
CMP1	0	P3.3 secondary function Compare output channel 1 output pin.
INT2	I	P3.4 secondary function External interrupt 2 input pin.
SFT0	0	P3.5 secondary function Shift register data output pin.
SFTI	I	P3.6 secondary function Shift register data input pin.
SFTCK	I/O	P3.7 secondary function Shift register synchronizing clock input/output pin.

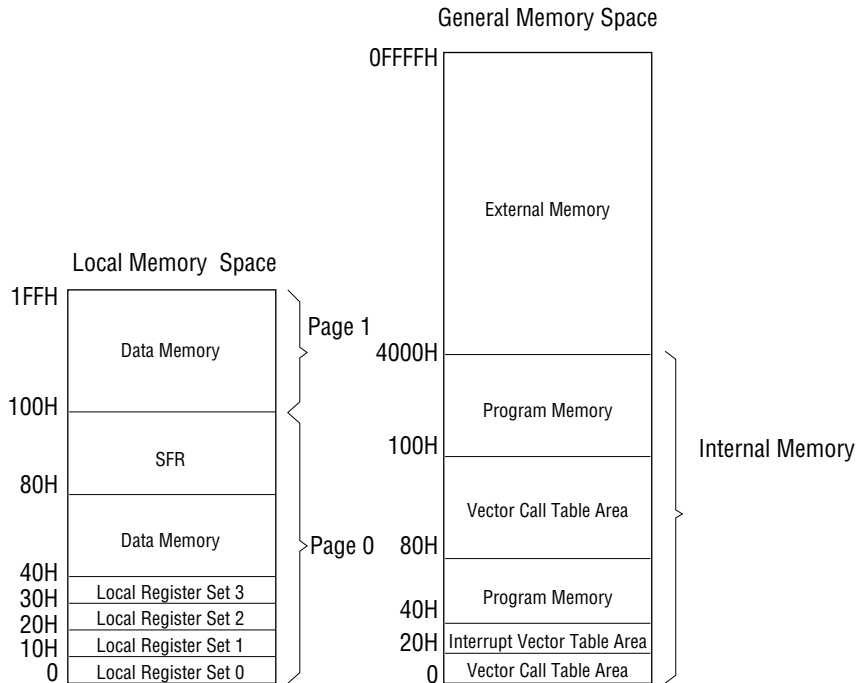
Port Circuit Configuration

Type	Port	Circuit Configuration	Electrical Characteristics (V _{DD} =5V)
1	P0.0/AD0 to P0.7/AD7		<p>"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V</p> <p>"H" Output Voltage: • V_{OH}=3.75V • I_{OH}=-400μA</p> <p>"L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA</p>
2	P1.0/A8 to P1.7/A15		<p>"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V</p> <p>"H" Output Voltage: • V_{OH}=3.75V • I_{OH}=-200μA</p> <p>"L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA</p>
3	P2.0/RXD, P2.1/TXD, P2.6/ \overline{WR} , P2.7/T1OUT, P3.2/CMP0, P3.3/CMP1, P3.5/SFT0, P3.7/SFTCK		<p>"H" Input Voltage: • V_{IH}=2.4V "L" Input Voltage: • V_{IL}=0.8V</p> <p>P2.6/\overline{WR} "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=-400μA</p> <p>"L" Output Voltage: • V_{OL}=0.4V • I_{OL}=3.2mA</p> <p>Excluding P2.6/\overline{WR} "H" Output Voltage: • V_{OH}=3.75V • I_{OH}=-200μA</p> <p>"L" Output Voltage: • V_{OL}=0.4V • I_{OL}=1.6mA</p>

Port Circuit Configuration (Continued)

Type	Port	Circuit Configuration	Electrical Characteristics (V _{DD} =5V)
4	P2.2/INT0, P2.3/INT1/GATE, P2.4/T0CK, P2.5/HSTOP, P3.0/T2CK, P3.1/CAP, P3.4/INT2, P3.6/SFTI, P4.0 to P4.7, P5.0 to P5.7	 <p style="text-align: right;">(x=2 to 5)</p>	"H" Input Voltage: • V _{IH} =2.4V "L" Input Voltage: • V _{IL} =0.8V "H" Output Voltage: • V _{OH} =3.75V • I _{OH} =-200μA "L" Output Voltage: • V _{OL} =0.4V • I _{OL} =1.6mA
5	P6.0 to P6.7		"H" Input Voltage: • V _{IH} =2.4V "L" Input Voltage: • V _{IL} =0.8V

MEMORY MAPS



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	$T_a=25^\circ\text{C}$	-0.3 to 7.0	V
Input Voltage	V_I		-0.3 to $V_{DD}+0.3$	
Output Voltage	V_O		-0.3 to $V_{DD}+0.3$	
Power Dissipation	P_D	$T_a=25^\circ\text{C}$ per package	400	mW
		$T_a=25^\circ\text{C}$ per output	50	
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	Refer to Figure 1	2.7 to 5.5	V
Memory Hold Voltage	V_{DDMH}	$f_{OSC}=0$ Hz	2.0 to 5.5	
Oscillation Operating Frequency *1	f_{OSC}	Refer to Figure 1	1 to 10	MHz
External Clock Operating Frequency	f_{EXTCLK}	Refer to Figure 1	0 to 10	MHz
Operating Temperature	T_{op}	—	-40 to +85	$^\circ\text{C}$

*1 This is due to the standard of a crystal oscillator or resonator.

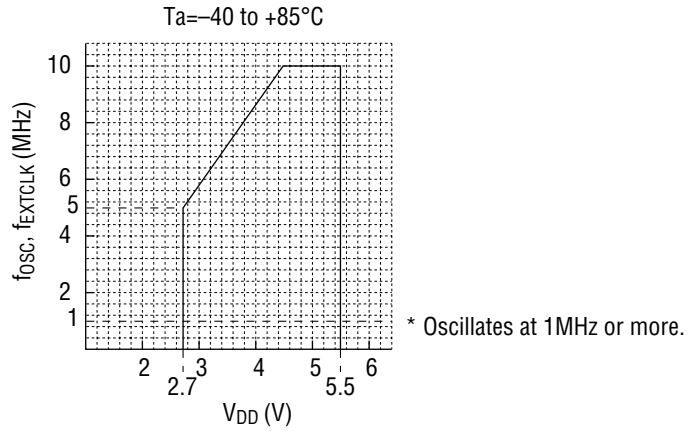


Figure 1. Operating Frequency vs. Power Supply Voltage

ELECTRICAL CHARACTERISTICS**DC Characteristics 1 ($V_{DD}=4.5$ to $5.5V$)**(GND=0V, $T_a=-40$ to $+85^{\circ}C$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 ^{*1}	V_{IH1}	—	2.4	—	$V_{DD}+0.3$	V
"H" Input Voltage 2 ^{*2}	V_{IH2}	—	$0.7V_{DD}$	—	$V_{DD}+0.3$	
"L" Input Voltage	V_{IL}	—	-0.3	—	0.8	
"H" Output Voltage 1 ^{*3}	V_{OH1}	$I_{OH}=-200\mu A$	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 ^{*4}	V_{OH2}	$I_{OH}=-400\mu A$	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 ^{*3}	V_{OL1}	$I_{OL}=1.6mA$	—	—	0.4	
"L" Output Voltage 2 ^{*4}	V_{OL2}	$I_{OL}=3.2mA$	—	—	0.4	μA
Input Leak Current 1 ^{*5}	I_{LI1}	$V_I=V_{DD}/0V$	—	—	± 1	
Input Leak Current 2 ^{*6}	I_{LI2}	$V_I=V_{DD}/0V$	—	—	± 10	
"L" Input Current ^{*7}	I_{IL}	$V_I=0V$	-40	-200	-400	
Input Capacity	C_i	$f=1MHz, T_a=25^{\circ}C$	—	5	—	pF
Still Current Consumption	I_{DDS}	5V, Stop mode ^{*8}	—	—	50	μA
Operating Current Consumption	I_{DD}	10MHz, 5V, no load Refer to Fig.2	—	20	40	mA

*1 Excluding OSC0 and \overline{RESET} *2 OSC0 and \overline{RESET} *3 Excluding P0, ALE, \overline{RD} , P2.6/ \overline{WR} *4 P0, ALE, \overline{RD} , P2.6/ \overline{WR} *5 \overline{EA} , P6*6 Excluding \overline{RESET} , \overline{EA} , P6*7 \overline{RESET} *8 The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.

DC Characteristics 2 ($2.7 \leq V_{DD} < 4.5V$)(GND=0V, $T_a = -40$ to $+85^\circ C$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1 ^{*1}	V_{IH1}	—	$0.5V_{DD}+0.2$	—	$V_{DD}+0.3$	V
"H" Input Voltage 2 ^{*2}	V_{IH2}	—	$0.6V_{DD}+0.4$	—	$V_{DD}+0.3$	
"L" Input Voltage	V_{IL}	—	-0.3	—	$0.15V_{DD}+0.1$	
"H" Output Voltage 1 ^{*3}	V_{OH1}	$I_{OH}=-10\mu A$	$0.75V_{DD}$	—	—	
"H" Output Voltage 2 ^{*4}	V_{OH2}	$I_{OH}=-20\mu A$	$0.75V_{DD}$	—	—	
"L" Output Voltage 1 ^{*3}	V_{OL1}	$I_{OL}=10\mu A$	—	—	0.1	
"L" Output Voltage 2 ^{*4}	V_{OL2}	$I_{OL}=20\mu A$	—	—	0.1	
Input Lack Current 1 ^{*5}	I_{LI1}	$V_I=V_{DD}/0V$	—	—	± 1	
Input Lack Current 2 ^{*6}	I_{LI2}	$V_I=V_{DD}/0V$	—	—	± 10	
"L" Input Current ^{*7}	I_{IL}	$V_{DD}=2.7$ to $3.3V$, $V_I=0V$	-40	-120	-240	
Input Capacity	C_I	$f=1MHz$, $T_a=25^\circ C$	—	5	—	pF
Still Current Consumption	I_{DDS}	3V, Stop mode ^{*8}	—	—	25	μA
Operating Current Consumption	I_{DD}	5MHz, 3V, no load Refer to Fig.2	—	6	15	mA

*1 Excluding OSC0 and \overline{RESET} *2 OSC0 and \overline{RESET} *3 Excluding P0, ALE, \overline{RD} , P2.6/ \overline{WR} *4 P0, ALE, \overline{RD} , P2.6/ \overline{WR} *5 \overline{EA} , P6*6 Excluding \overline{RESET} , \overline{EA} , P6*7 \overline{RESET} *8 The ports configured as inputs should be coupled to V_{DD} or 0V. Other ports should not be loaded.

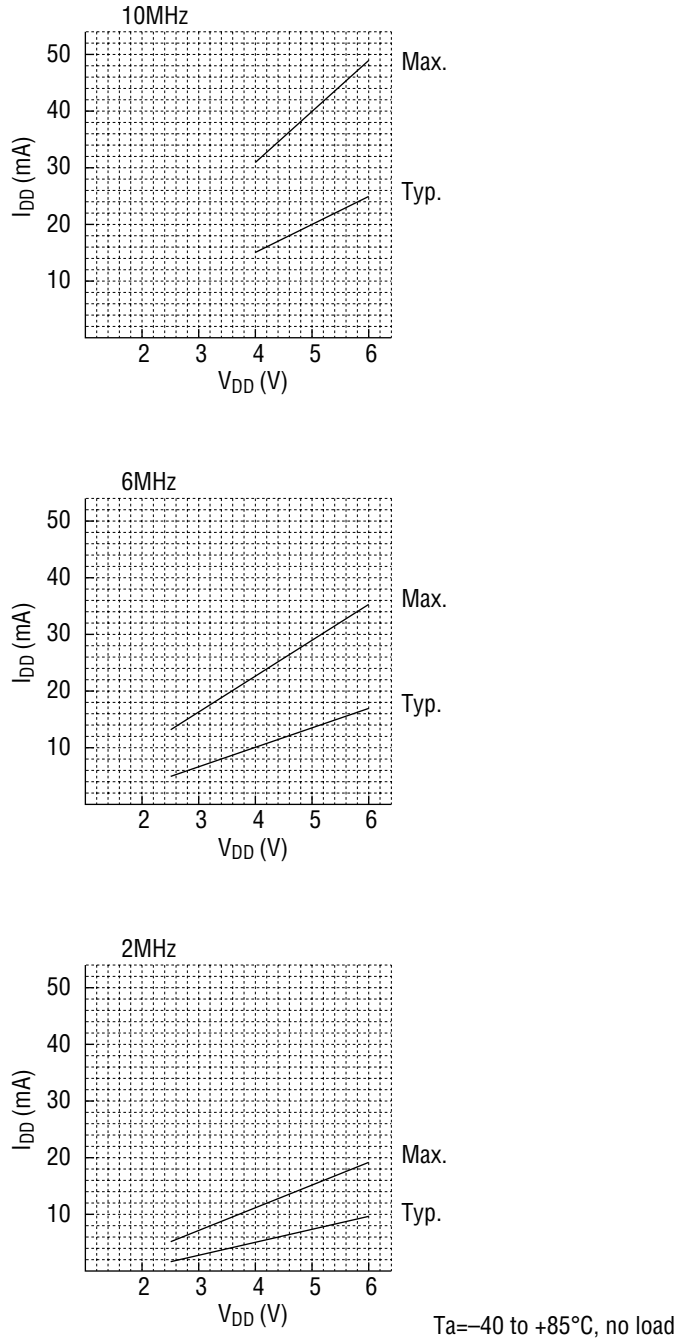


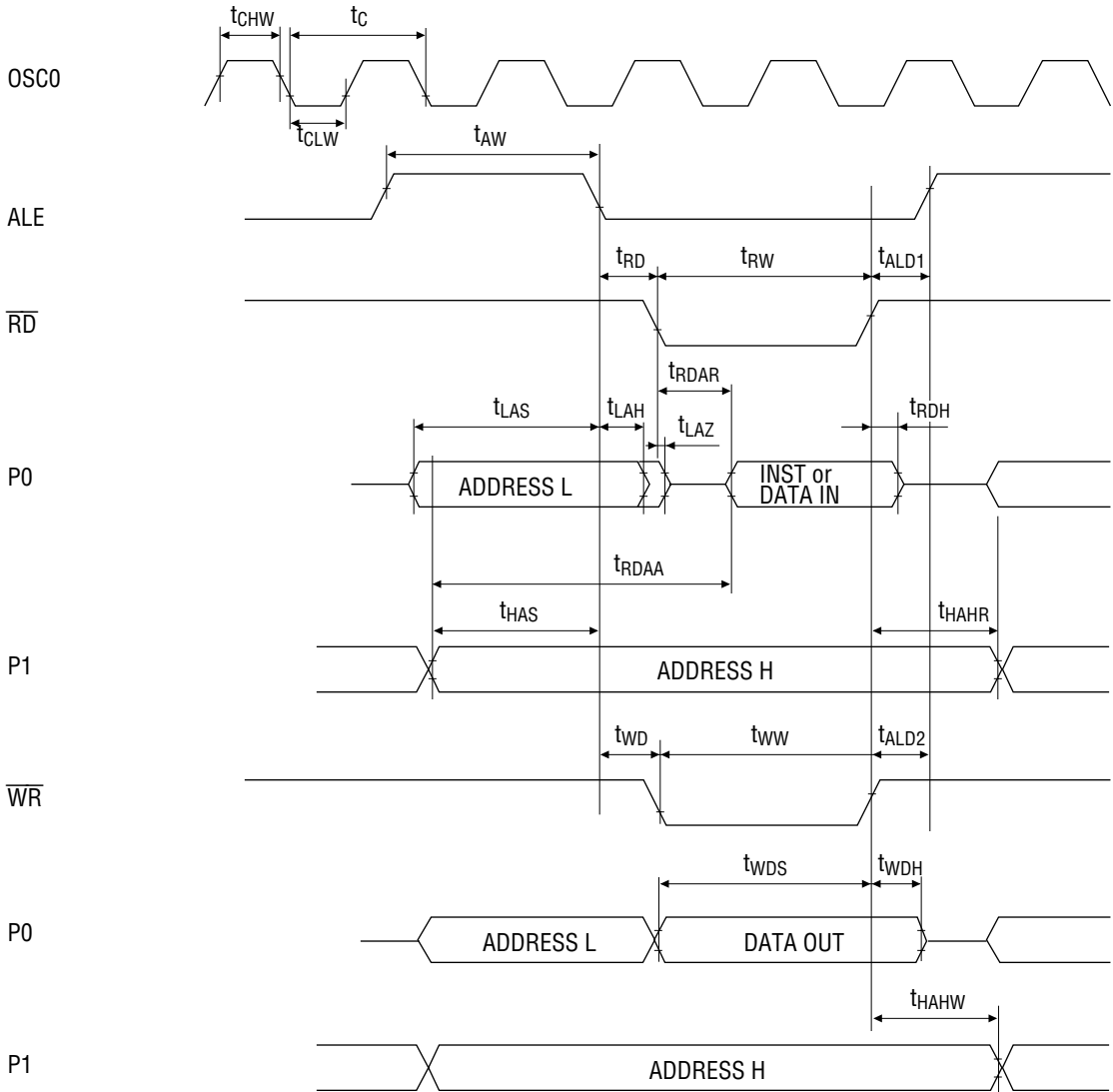
Figure 2. Operating Current Consumption vs. Power Supply Voltage

AC Characteristics

- External memory control

(V_{DD}=2.7 to 5.5V, GND=0V, T_a=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Period	t _C	V _{DD} =4.5 to 5.5V	100	—	ns
"L" Clock Pulse Width	t _{CLW}		45	—	
"H" Clock Pulse Width	t _{CHW}		45	—	
Clock Period	t _C	V _{DD} =2.7 to 5.5V	200	—	
"L" Clock Pulse Width	t _{CLW}		90	—	
"H" Clock Pulse Width	t _{CHW}		90	—	
ALE Pulse Width	t _{AW}	C _L =100pF	t _C +t _{CHW} -20	—	
ALE Pulse Delay Time 1	t _{ALD1}		t _{CLW} -20	—	
ALE Pulse Delay Time 2	t _{ALD2}		t _{CLW} -20	—	
\overline{RD} Pulse Width	t _{RW}		t _C +t _{CHW} -20	—	
\overline{RD} Pulse Delay Time	t _{RD}		t _{CLW} -40	t _{CLW} +20	
\overline{WR} Pulse Width	t _{WW}		t _C +t _{CHW} -40	—	
\overline{WR} Pulse Delay Time	t _{WD}		t _{CLW} -20	t _{CLW} +40	
"L" Address Setup Time	t _{LAS}		t _C -40	—	
"H" Address Setup Time	t _{HAS}		t _C -40	—	
"L" Address Hold Time	t _{LAH}		t _{CLW} -20	—	
Bus Float Time	t _{LAZ}		—	20	
"H" Address Hold Time	t _{HAHR}		t _C -20	—	
"H" Address Hold Time	t _{HAHW}		t _C -20	—	
Read Data Access Time	t _{RDAA}		—	t _C +t _{CLW} -15	
Read Data Access Time	t _{RDAR}		—	t _{CHW} +10	
Read Data Hold Time	t _{RDH}		0	—	
Write Data Setup Time	t _{WDS}		t _C +t _{CLH} -40	—	
Write Data Hold Time	t _{WDH}		t _{CLW} -20	—	



• CPU control

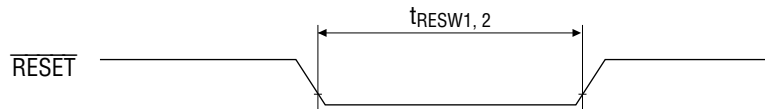
(V_{DD}=2.7 to 5.5V, GND=0V, T_a=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
RESET Pulse Width *1	t _{RESW1}	—	20	—	ns
RESET Pulse Width *2	t _{RESW2}	—	*3	—	—

*1 Excluding power ON, stop mode and hard stop mode.

*2 In power ON, stop mode and hard stop mode.

*3 Oscillation stabilization time depends on resonator.

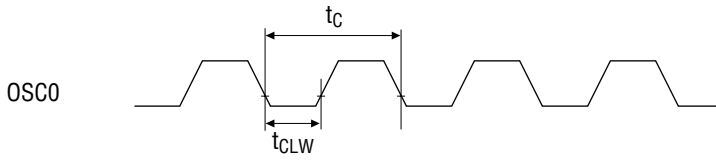
RESET pulse width

• Peripheral control 1

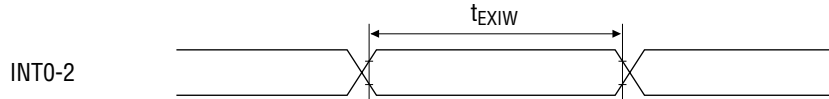
(V_{DD}=2.7 to 5.5V, GND=0V, T_a=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	V _{DD} =4.5 to 5.5V	100	—	ns
		V _{DD} =2.7 to 5.5V	200	—	
EXI	External Interrupt Pulse Width	—	4 t _c	—	
T0	External Clock Pulse Width		4 t _c	—	
	GATE Pulse Width		1 t _{TOCLK} *	—	
T2	External Clock Pulse Width		4 t _c	—	
CAP	CAP Pulse Width	12 t _c	—		

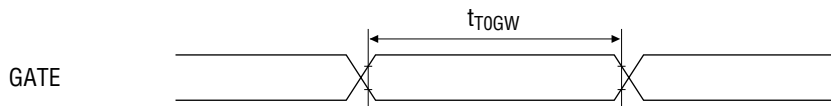
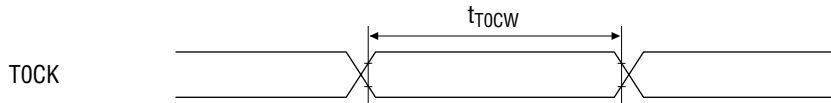
* t_{TOCLK} : Timer 0 count clock period selected by T0CON.



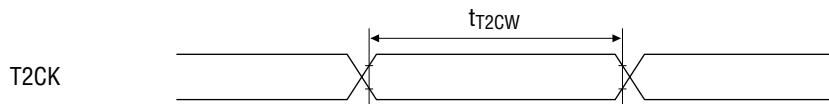
1) EXI pulse width



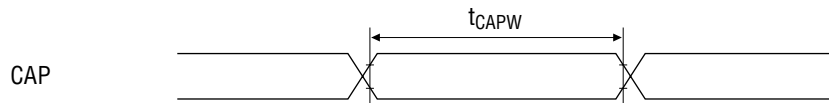
2) T0



3) T2



4) CAP



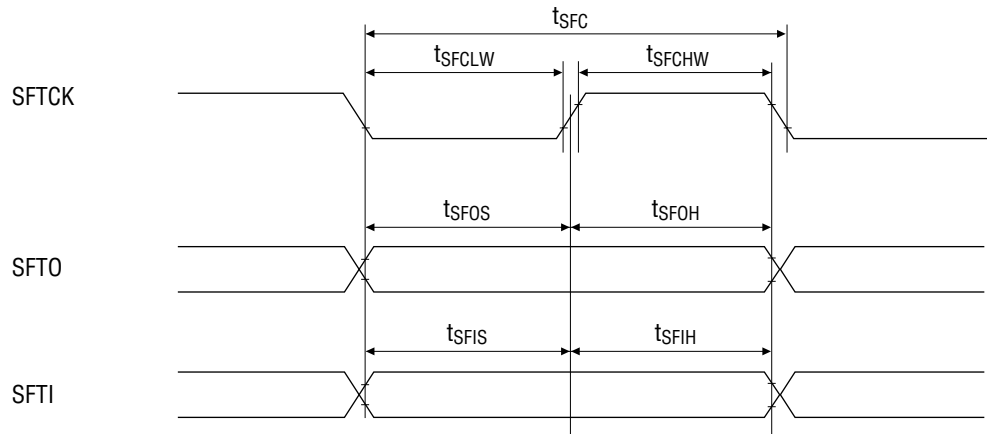
• Peripheral control 2

(V_{DD}=2.7 to 5.5V, GND=0V, T_a=-40 to +85°C)

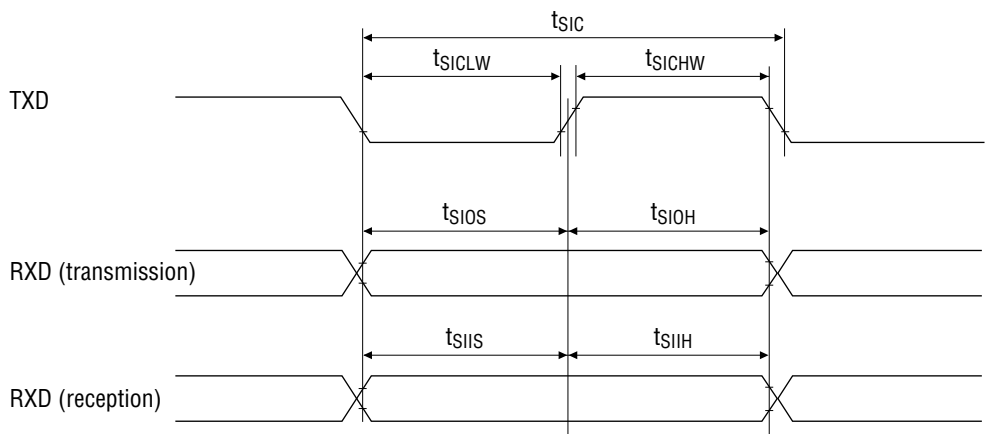
	Parameter	Symbol	Condition	Min.	Max.	Unit
OSC	Clock Period	t _c	V _{DD} =4.5 to 5.5V	100	—	ns
			V _{DD} =2.7 to 5.5V	200	—	
SFT	SFTCK Period	t _{SFC}	C _L =100pF	8 t _c	—	
	SFTCK "L" Pulse Width	t _{SFCLW}		4 t _c -20	—	
	SFTCK "H" Pulse Width	t _{SFCHW}		4 t _c -20	—	
	SFTCK Setup Time	t _{SFOS}		t _{SFCLW} -100	—	
	SFTO Hold Time	t _{SFOH}		t _{SFCHW} -100	—	
	SFTI Setup Time	t _{SFIS}		100	—	
	SFTI Hold Time	t _{SFIH}		100	—	
SIO (Clock Synchronous Mode)	Synchronous Clock Period	t _{SIC}	C _L =100pF	8 t _c	—	
	Synchronous Clock "L" Pulse Width	t _{SICLW}		4 t _c -20	—	
	Synchronous Clock "H" Pulse Width	t _{SICHW}		4 t _c -20	—	
	Output Data Setup Time	t _{SIOS}		6 t _c -100	—	
	Output Data Hold Time	t _{SIOH}		2 t _c -100	—	
	Input Data Setup Time	t _{SII S}		t _c +t _{CLW} +100	—	
	Input Data Hold Time	t _{SIIH}		0	—	

See TIMING DIAGRAM.

1) SFT

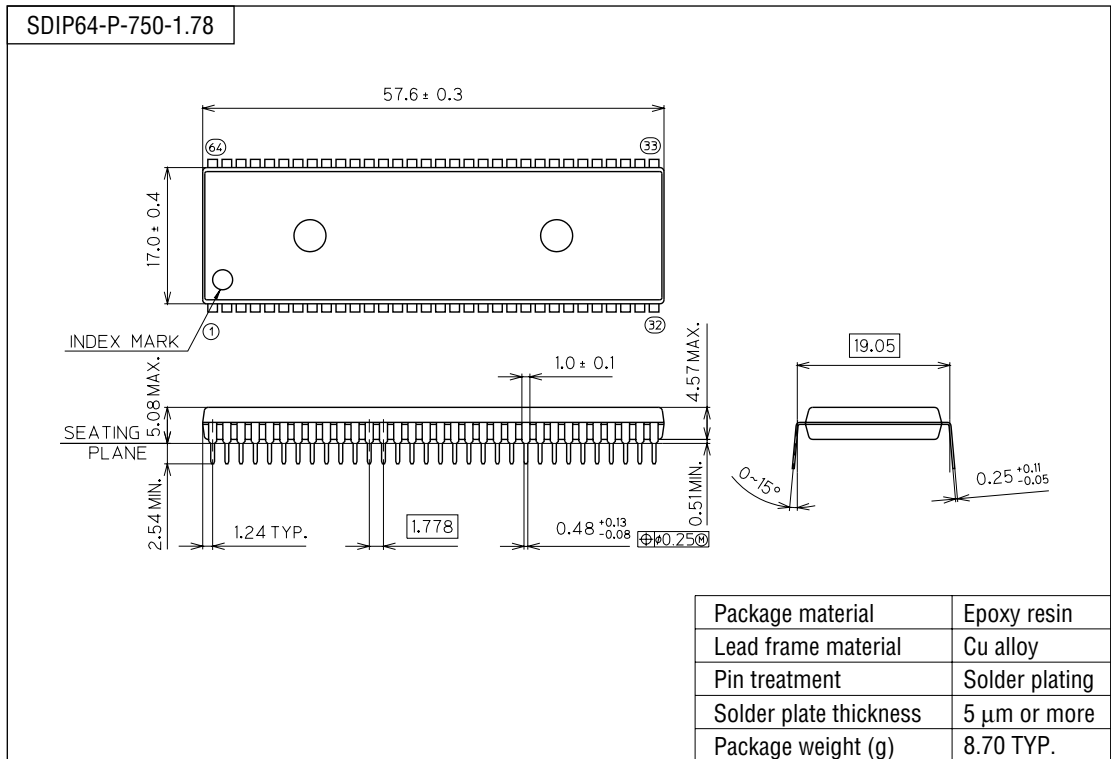


2) SIO
(Clock synchronous mode)



PACKAGE DIMENSIONS

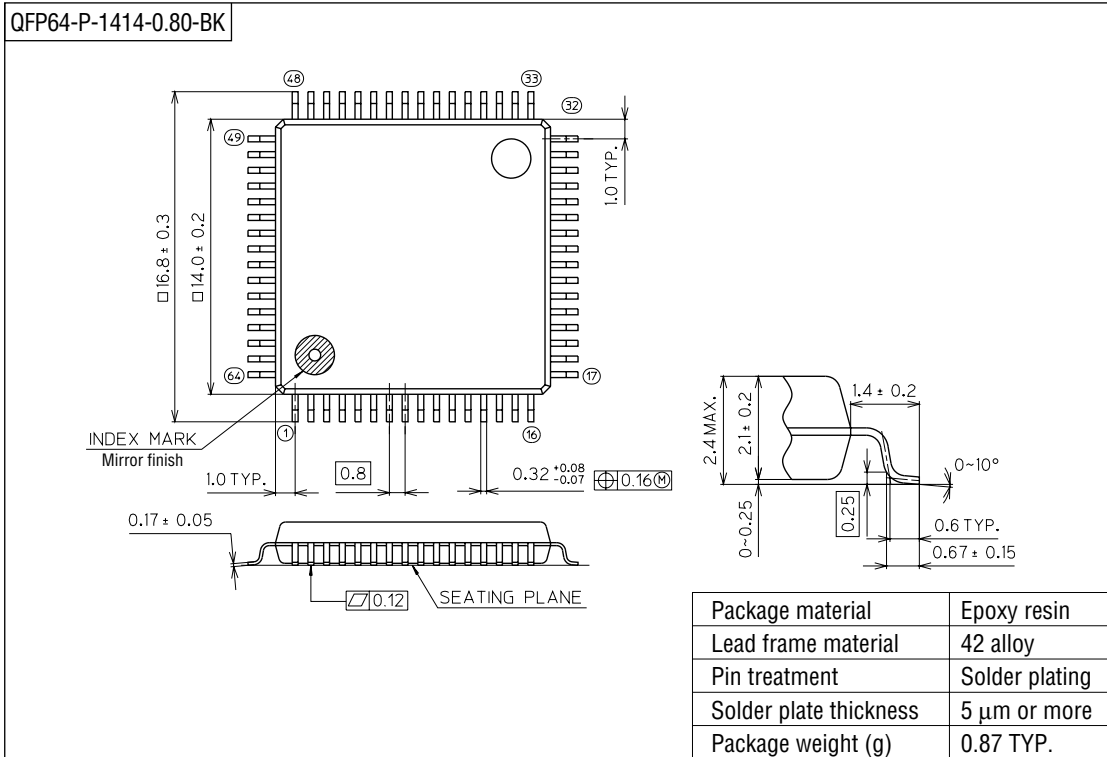
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

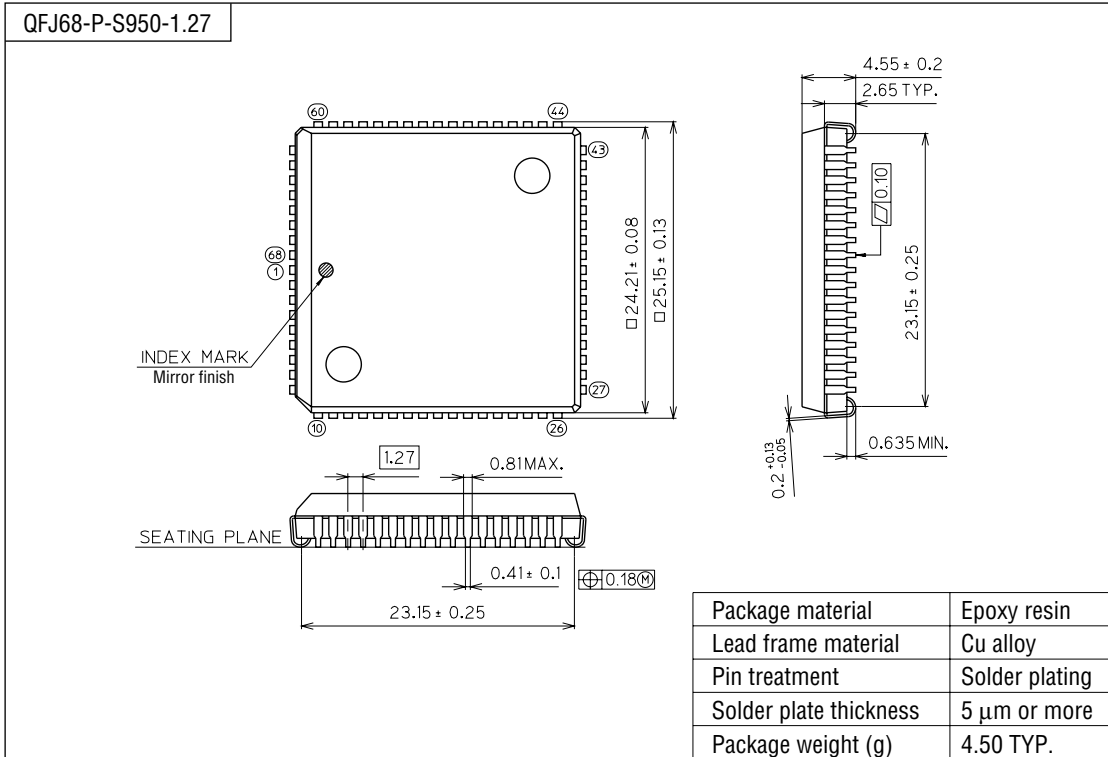
(Unit : mm)



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(Unit : mm)



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