OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM6234

DTMF Tone Dialer LSI

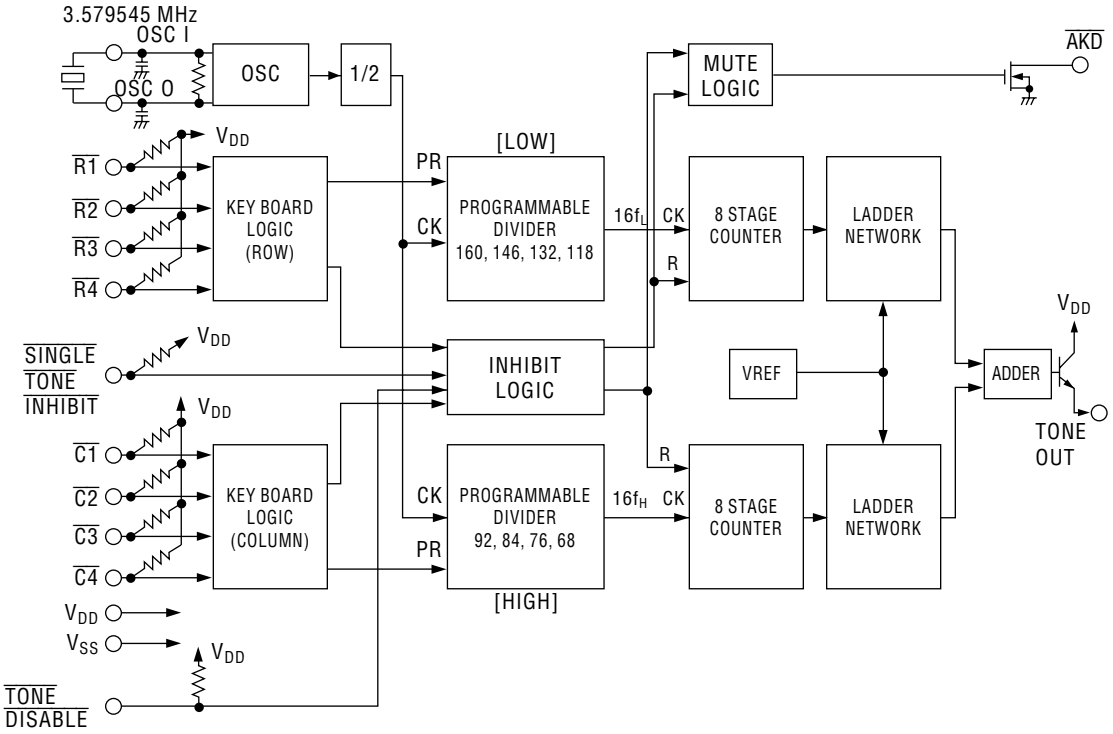
GENERAL DESCRIPTION

The MSM6234 is a tone dialer LSI which is fabricated by Oki's low power consumption CMOS silicon gate technology.
The MSM6234 can generate 16 DTMF (Dual Tone Multi Frequency) signals which consists of 4 higher group frequencies and 4 lower group frequencies.

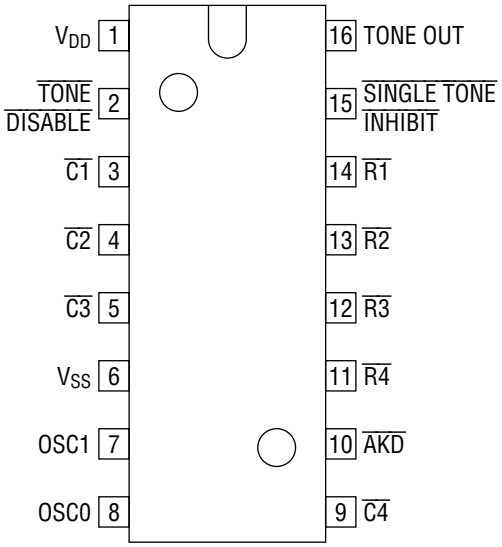
FEATURES

- The standard 2 of 8 keyboard can be used.
- The low power consumption by use of CMOS silicon gate technology.
- Supply voltage 2.5 V to 8.5 V.
- Either single tone or dual tone output.
- 3.579545 MHz crystal oscillation.
- Interface with microcotroller.
- Package:
  16-pin plastic DIP (DIP16-P-300-2.54) (Product name : MSM6234RS)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

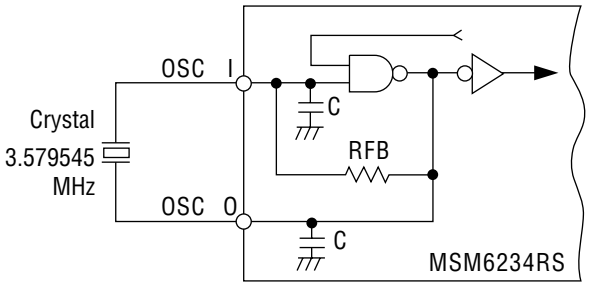


16-Pin Plastic DIP

PIN AND FUNCTIONAL DESCRIPTIONS

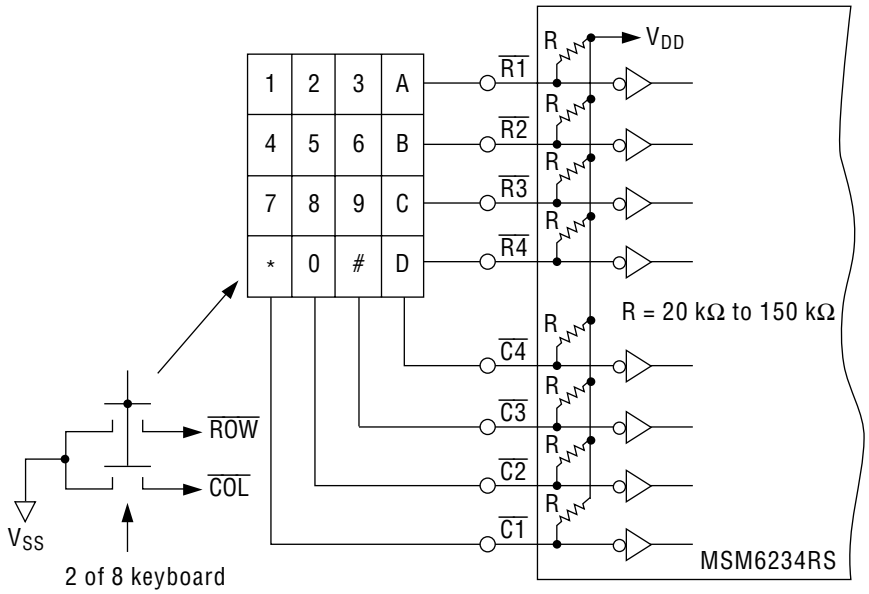
OSCI, OSCO

The 3.579545 MHz crystal oscillator is connected to these pins.
A feedback resistor and the condensers are incorporated.



$\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$, $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$

These are input pins of negative logic to be connected to the keyboard.
The standard 2 of 8 keyboard can be used with MSM6234RS as illustrated below.



$\overline{R1}$ to $\overline{R4}$ are the input pins of the row side, while $\overline{C1}$ to $\overline{C4}$ are the input pins of the column side. All the pins are provided with the pull-up resistor of 20 kΩ to 150 kΩ internally.

The dual tone is output from the TONE OUT pin, by setting both of a row input and a column input to the ground voltage.

The Table 1 (See Note) shows the relation between the nominal frequency and the tone output frequency, while the Table 2 (See Note) shows the input condition of $\overline{R1}$ to $\overline{R4}$ pins and $\overline{C1}$ to $\overline{C4}$ pins.
• Refer to the Table 1 and Table 2

Table-1

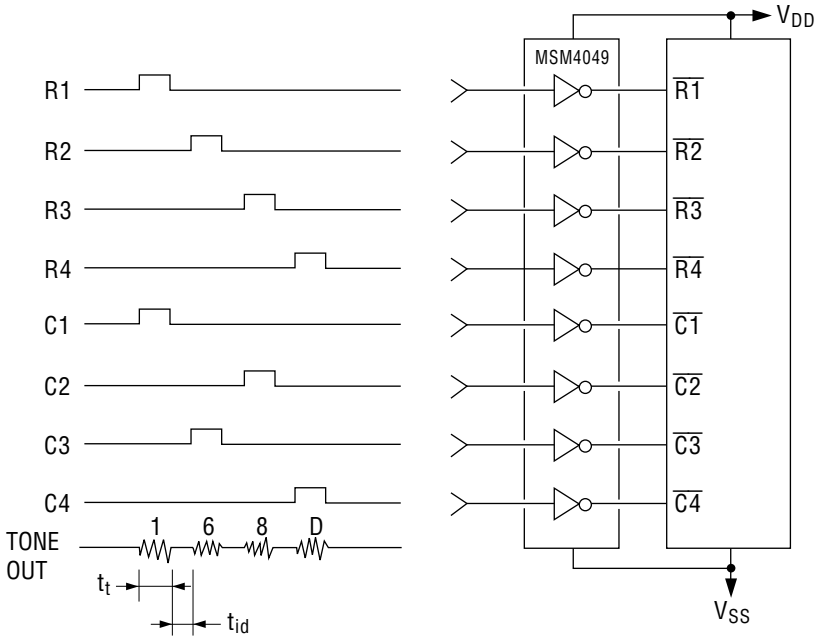
Effective Input		Nominal Frequency	Tone Output Frequency	Accuracy (%)	Remarks
(ROW)	$\overline{R1}$	697 Hz	699.1 Hz	+0.30%	Low Group
	$\overline{R2}$	770 Hz	766.2 Hz	–0.49%	
	$\overline{R3}$	852 Hz	847.4 Hz	–0.54%	
	$\overline{R4}$	941 Hz	948.0 Hz	+0.74%	
(COLUMN)	$\overline{C1}$	1209 Hz	1215.9 Hz	+0.57%	High Group
	$\overline{C2}$	1336 Hz	1331.7 Hz	–0.32%	
	$\overline{C3}$	1477 Hz	1471.9 Hz	–0.35%	
	$\overline{C4}$	1633 Hz	1645.0 Hz	+0.73%	

Table-2

Row Input	Column Input	Tone Output *	Remarks
No	No	0 V	
1	1	$f_L + f_H$	Dual tone
No	1	f_H	Single tone (Only column)
1	No	0 V	
More than 2	No	0 V	
More than 2	1	f_H	Single tone
No	More than 2	0 V	
1	More than 2	f_L	Single tone
More than 2	More than 2	0 V	

f_L: Low Group
f_H: High Group
* : The tone output shown is in the case when the load resistance is connected between the TONE OUT pin and the V_{SS}.

Sample Interface Circuit with Microcontroller

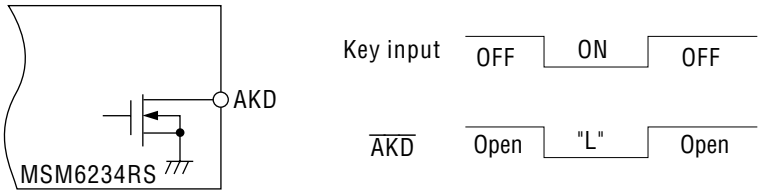


$t_t \geq 50$ ms and 30 ms $\leq$ tid $\leq$ 3 s

Figure 1

$\overline{\text{AKD}}$

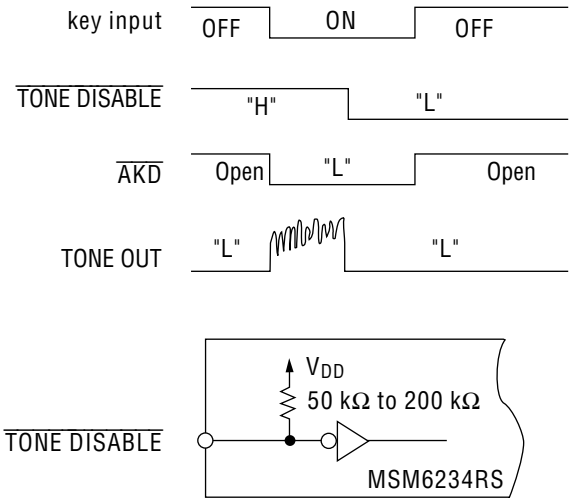
The $\overline{\text{AKD}}$ pin drives the external bipolar transistor by its N-channel open drain output. This pin is open when the key input is off, while it becomes low when the key input is on. $\overline{\text{AKD}}$ is used for the mute of the transmitter/receiver.



$\overline{\text{TONE DISABLE}}$

This is an input pin to control the output of the TONE OUT pin.
When the input to this pin is high level, the TONE OUT pin normally operates. When the input to this pin is low level, however, the output from the TONE OUT pin is prohibited even if the key input is on.

AKD is effective at that time. This pin is provided with the pull-up resistance of 50 kΩ to 200 kΩ internally.

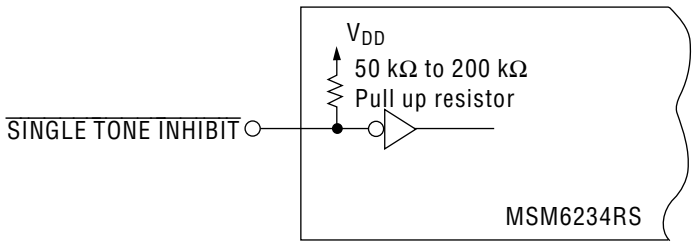


SINGLE TONE INHIBIT

When more than two columns are selected against only one row, or when more than 2 rows are selected against only one column, the single tone is output from the TONE OUT pin. This $\overline{\text{SINGLE TONE INHIBIT}}$ pin is a negative logic input pin to control the output of the TONE OUT pin in those cases. Refer to the Table-2.

When the input to this pin is high level, both of the single tone and dual tone are output from the TONE OUT pin. When the input to this pin is low level, however, the single tone is prohibited to output from the TONE OUT pin and becomes DC level.

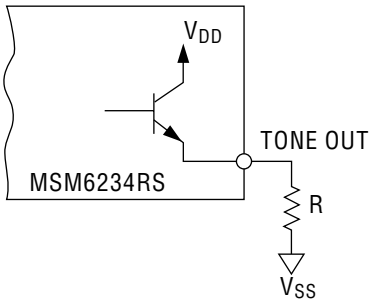
This pin is provided with the pull-up resistor of 50 kΩ to 200 kΩ.



TONE OUT

The low group frequency and the high group frequency selected by the keyboard are synthesized and output from this TONE OUT pin. Because the output form is the NPN open emitter style, the load resistance must be connected externally. It is same for the case of the single tone output. The output amplitude of the high group is bigger than that of the low group by 1 to 2 dB.

The distortion of the dual tone is maximum 10%.



V_{DD}, V_{SS}

V_{DD} is a power supply.
V_{SS} is ground.

Sample Output Waveform of the Single Tone

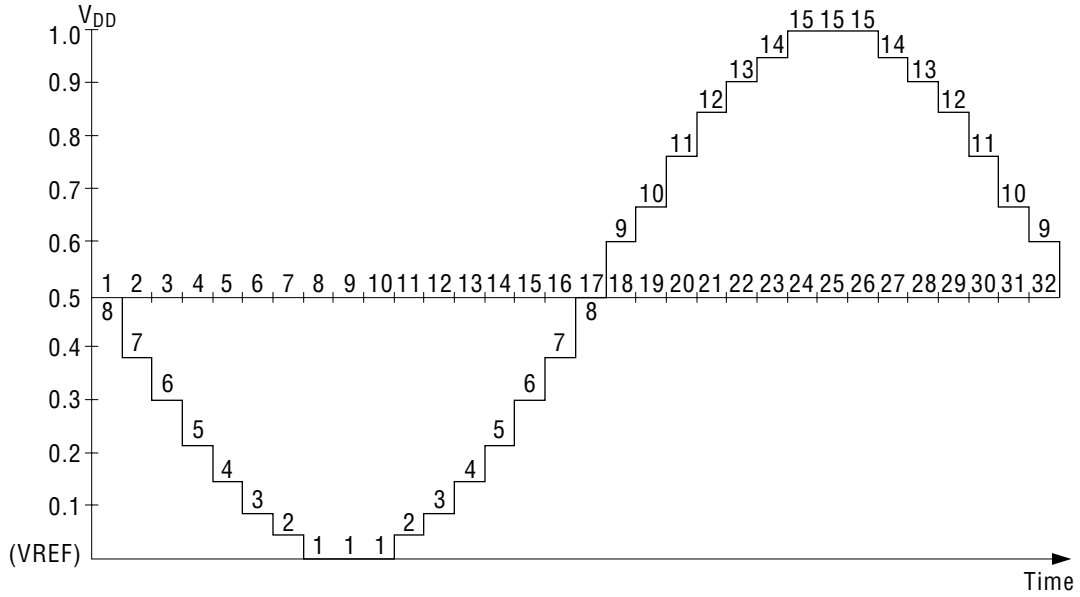


Figure 2

Tone Amplitude (mV rms)

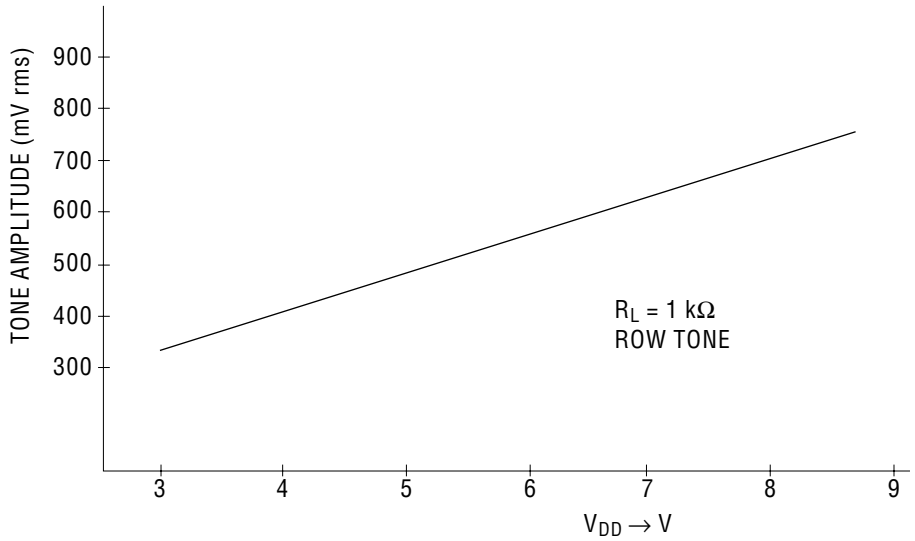


Figure 3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to 9.5	V
Storage Temperature	T_{STG}	—	–55 to +150	°C
Power Dissipation	P_D	Ta = 25°C	500	mW
Input Voltage	V_I	—	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	—	V_{SS} – 0.3 to V_{DD} + 0.3	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.5	5	8.5	V
Operating Temperature	Top	—	–30	—	+70	°C
Crystal Frequency	$f_{(XT)}$	Ta = –30°C to +70°C V_{DD} = 2.5 V to 8.5 V	—	3.579545	—	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –30°C to +70°C)

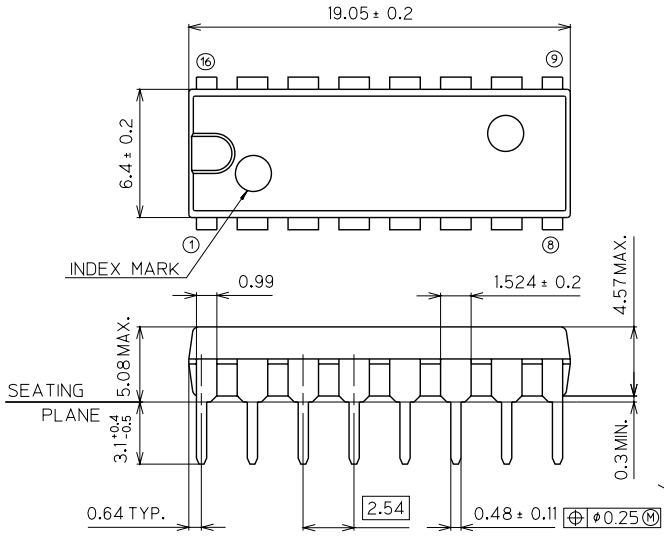
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Input High Voltage	V_{IH}	—	$0.7V_{DD}$	—	V_{DD}	V	$\overline{C}_1$ to $\overline{C}_4$, $\overline{R}_1$ to $\overline{R}_4$
Input Low Voltage	V_{IL}	—	V_{SS}	—	$0.3V_{DD}$	V	$\overline{C}_1$ to $\overline{C}_4$, $\overline{R}_1$ to $\overline{R}_4$
Low Level Input Leakage Current	I_{IL}	V_{DD} = 8.5 V, V_{IL} = 0 V	–0.0567	—	–0.425	mA	$\overline{C}_1$ to $\overline{C}_4$, $\overline{R}_1$ to $\overline{R}_4$
"TONE OUT" Output Voltage	V_{OUT}	V_{DD} = 3.0 V, R_L = 1 kΩ	235	—	437	mV rms	TONE OUT
Difference of High/Low Band Level	dB_{CR}	V_{DD} = 3.0 V to 8.5 V	1	1.5	2	dB	TONE OUT
Distortion	$\%_{DIS}$	V_{DD} = 3.0 V to 8.5 V	—	—	10	%	TONE OUT
High Level Input Leakage Current	I_{IH}	V_{DD} = 8.5 V, V_{IH} = 8.5 V	—	—	1	µA	$\overline{C}_1$ to $\overline{C}_4$, $\overline{R}_1$ to $\overline{R}_4$ $\overline{STI}$, $\overline{TOND}$*
Low Level Input Leakage Current	I_{IL}	V_{DD} = 8.5 V, V_{IL} = 0 V	–42.5	—	–170	µA	$\overline{STI}$, $\overline{TOND}$*
Input High Voltage	V_{IH}	—	$0.7V_{DD}$	—	V_{DD}	V	$\overline{STI}$, $\overline{TOND}$*
Input Low Voltage	V_{IL}	—	V_{SS}	—	$0.3V_{DD}$	V	$\overline{STI}$, $\overline{TOND}$*
Power Supply Current (Stand-by)	I_{DDS}	V_{DD} = 8.5 V, No load, Key-OFF	—	—	200	µA	
Power Supply Current (Operating)	I_{DD}	V_{DD} = 8.5 V, R_L = 1 kΩ, No load, Key-ON	—	—	25	mA	
Low Level Output Leakage Current	I_{OL}	V_{DD} = 3 V, V_{OL} = 0.5 V	0.53	1.3	—	mA	$\overline{AKD}$
		V_{DD} = 8.5 V, V_{OL} = 0.5 V	2.0	5.3	—		
"OFF" Leakage Current	I_{OFF}	V_{DD} = 8.5 V	—	—	10	µA	$\overline{AKD}$
TONE OUT Rise Time	t_{rise}	V_{DD} = 3.0 V to 8.5 V	—	3.0	5.0	ms	TONE OUT

*: $\overline{STI}$ → $\overline{SINGLE\ TONE\ INHIBIT}$
$\overline{TOND}$ → $\overline{TONE\ DISABLE}$

PACKAGE DIMENSIONS

(Unit : mm)

DIP16-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.99 TYP.