

MSM512200/L

1,048,576-Word × 2-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM512200/L is a 1,048,576-word × 2-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM512200/L achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM512200/L is available in a 26/20-pin plastic SOJ or 26/20-pin plastic TSOP. The MSM512200L (the low-power version) is specially designed for lower-power applications.

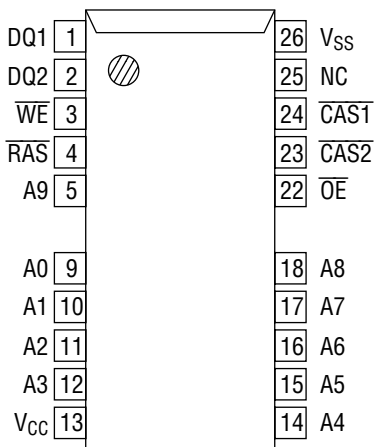
FEATURES

- 1,048,576-word × 2-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (L-version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Package options:
 - 26/20-pin 300 mil plastic SOJ (SOJ26/20-P-300-1.27) (Product : MSM512200/L-xxSJ)
 - 26/20-pin 300 mil plastic TSOP (TSOPII26/20-P-300-1.27-K) (Product : MSM512200/L-xxTS-K)
 xx indicates speed rank.

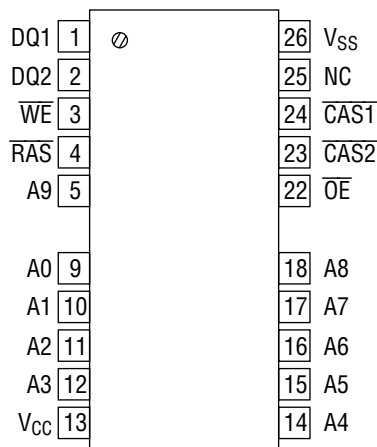
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM512200/L-60	60 ns	30 ns	15 ns	15 ns	110 ns	440 mW	5.5 mW/ 0.55 mW (L-version)
MSM512200/L-70	70 ns	35 ns	20 ns	20 ns	130 ns	385 mW	
MSM512200/L-80	80 ns	40 ns	20 ns	20 ns	150 ns	330 mW	

PIN CONFIGURATION (TOP VIEW)



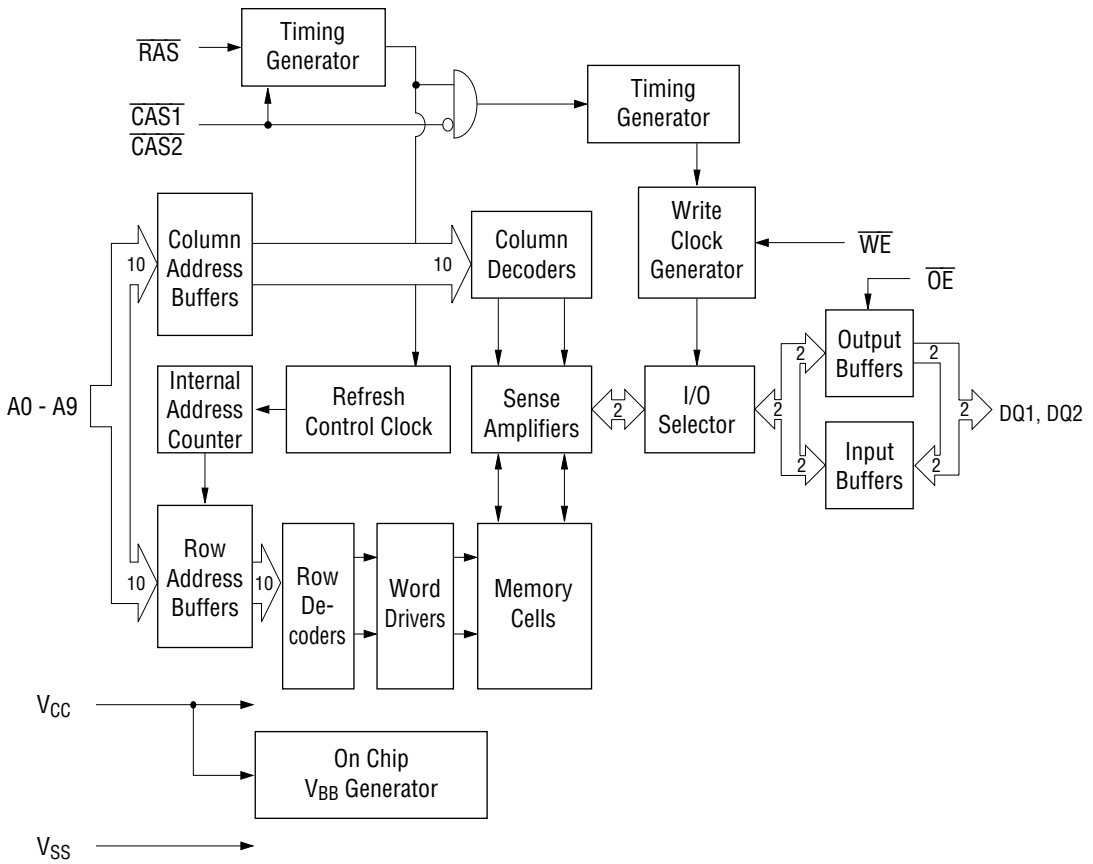
26/20-Pin Plastic SOJ



26/20-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A9	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$	Column Address Strobe
DQ1, DQ2	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-1.0 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operating Temperature	T _{opr}	0 to 70	°C
Storage Temperature	T _{stg}	-55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	6.5	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

Capacitance(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C _{IN1}	—	6	pF
Input Capacitance (<u>RAS</u> , <u>CAS1</u> , <u>CAS2</u> , <u>WE</u> , <u>OE</u>)	C _{IN2}	—	7	pF
Output Capacitance (DQ1, DQ2)	C _{I/O}	—	7	pF

DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ\text{C} \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	MSM512200 /L-60		MSM512200 /L-70		MSM512200 /L-80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0 \text{ V} \leq V_I \leq 6.5 \text{ V}$; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	DQ disable $0 \text{ V} \leq V_O \leq 5.5 \text{ V}$	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS1}}, \overline{\text{CAS2}}$ cycling, $t_{RC} = \text{Min.}$	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}, \overline{\text{CAS1}}, \overline{\text{CAS2}} = V_{IH}$	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}, \overline{\text{CAS1}}, \overline{\text{CAS2}} \geq V_{CC} - 0.2 \text{ V}$	—	1	—	1	—	1		
				—	100	—	100	—	100	μA
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS1}}, \overline{\text{CAS2}} = V_{IH}$, $t_{RC} = \text{Min.}$	—	80	—	70	—	60	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS1}}, \overline{\text{CAS2}} = V_{IL}$, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS1}}, \overline{\text{CAS2}}$ before $\overline{\text{RAS}}$	—	80	—	70	—	60	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS1}}, \overline{\text{CAS2}}$ cycling, $t_{PC} = \text{Min.}$	—	60	—	55	—	50	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	$t_{RC} = 125 \mu\text{s}$, $\overline{\text{CAS1}}, \overline{\text{CAS2}}$ before $\overline{\text{RAS}}$, $t_{RAS} \leq 1 \mu\text{s}$	—	200	—	200	—	200	μA	1, 4, 5

- Notes : 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
3. The address can be changed once or less while $\overline{\text{CAS1}}, \overline{\text{CAS2}} = V_{IH}$.
4. $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq 6.5 \text{ V}$, $-1.0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM512200 /L-60		MSM512200 /L-70		MSM512200 /L-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t _{RWC}	150	—	180	—	200	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	80	—	95	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	ns	4, 14
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	0	20	ns	7
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t _{REF}	—	128	—	128	—	128	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10	—	10	—	10	—	ns	16
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	14
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	45	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	45	20	50	20	60	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	13
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	ns	13
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	40	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3, 11, 12

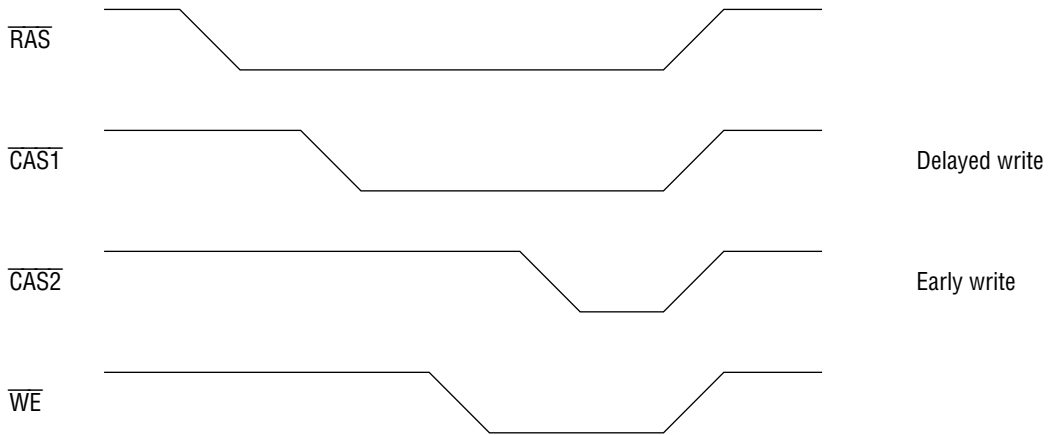
Parameter	Symbol	MSM512200 /L-60		MSM512200 /L-70		MSM512200 /L-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	13
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8, 13
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9, 13
Write Command Hold Time	t _{WCH}	10	—	10	—	10	—	ns	13
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	45	—	50	—	60	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	20	—	ns	15
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	10, 13
Data-in Hold Time	t _{DH}	15	—	15	—	15	—	ns	10, 13
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—	60	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OEED}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	35	—	45	—	45	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	50	—	60	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80	—	95	—	105	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	55	—	65	—	70	—	ns	9, 14
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	5	—	5	—	5	—	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	ns	14
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t _{WTH}	10	—	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 11. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.
 13. These parameters are determined by the falling edge of either $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$, whichever is earlier.
 14. These parameters are determined by the rising edge of either $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$, whichever is later.
 15. t_{CWL} , t_{DH} and t_{DS} should be satisfied by both $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$.
 16. t_{CP} is determined by the time both $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$ are high.

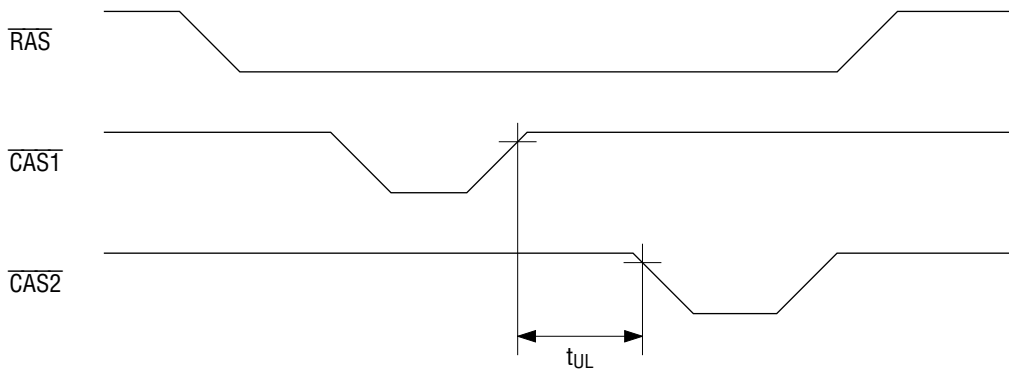
Notes concerning $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$ control

Overlap the active-low timings of $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$. Skew between $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$ is allowed under the following conditions:

- (1) The timing specification for $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$ should be met individually.
- (2) Different operation modes for $\overline{\text{CAS1}}/\overline{\text{CAS2}}$ are not allowed (as shown below).

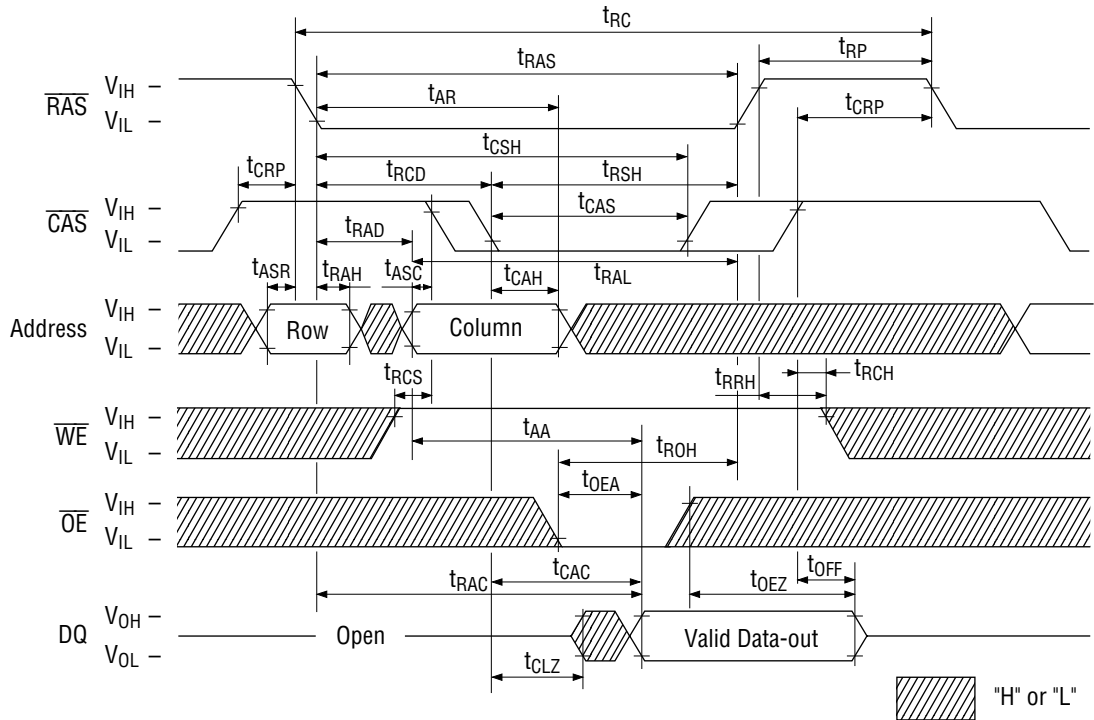


- (3) Closely separated $\overline{\text{CAS1}}/\overline{\text{CAS2}}$ control is not allowed. However, when the condition ($t_{\text{CP}} \leq t_{\text{UL}}$) is satisfied, fast page mode can be performed.

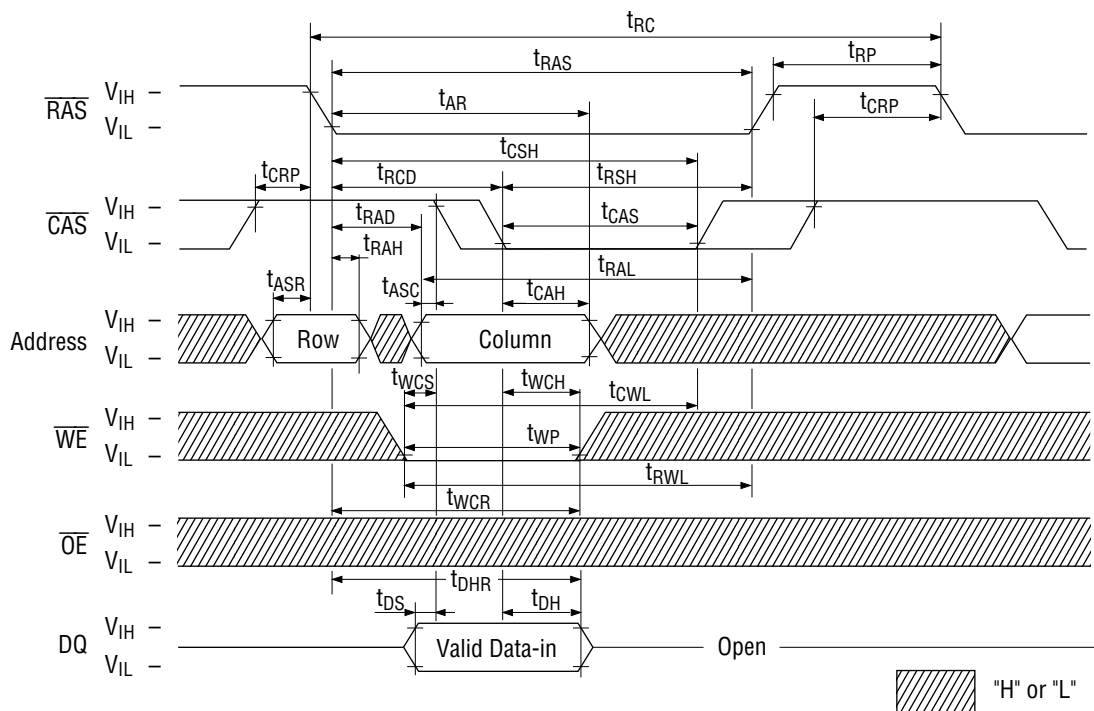


TIMING WAVEFORM

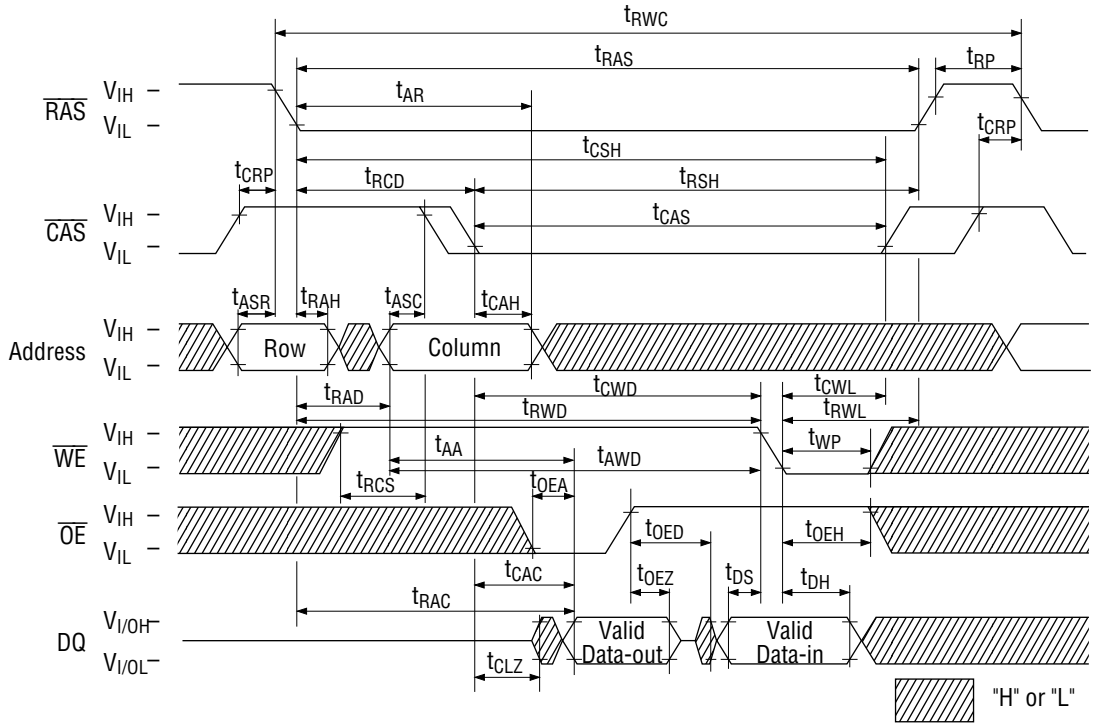
Read Cycle



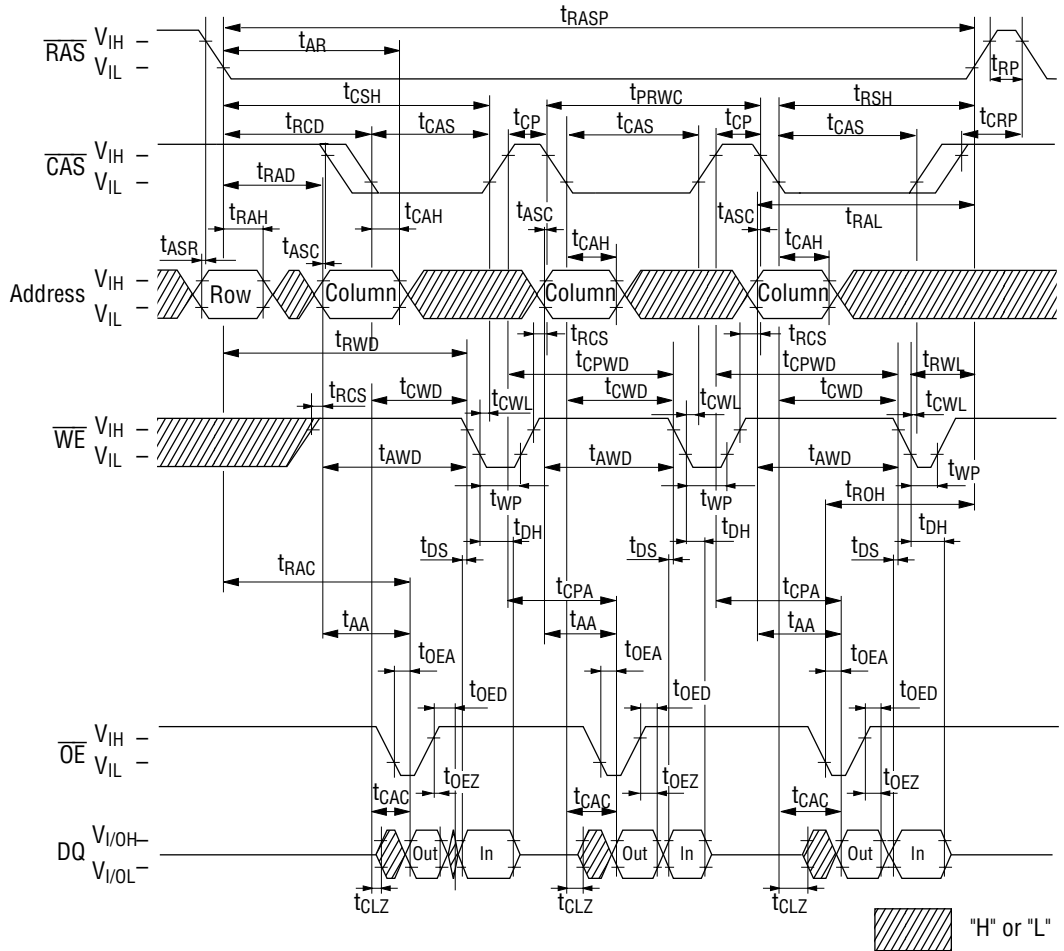
Write Cycle (Early Write)



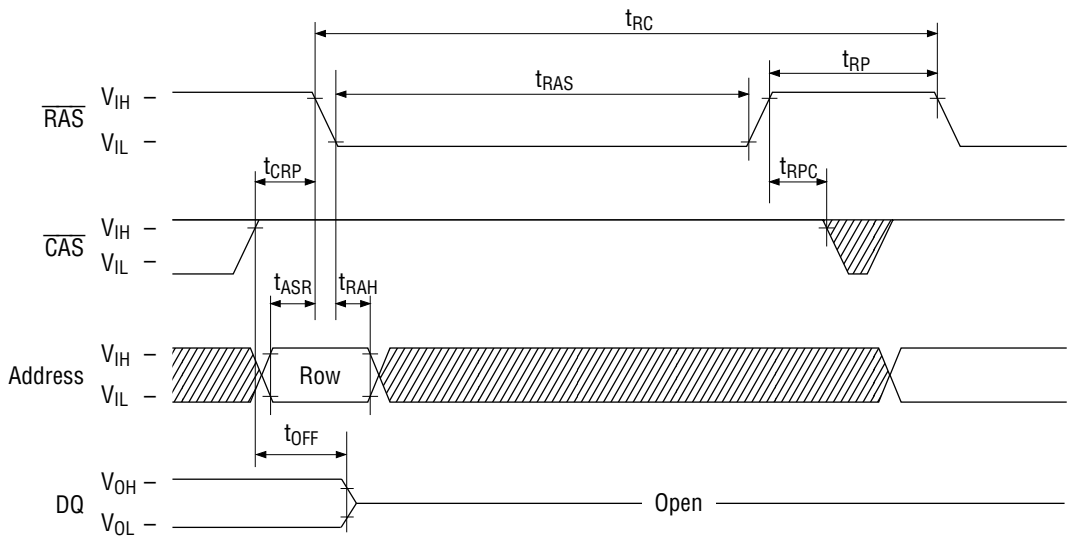
Read Modify Write Cycle



Fast Page Mode Read Modify Write Cycle



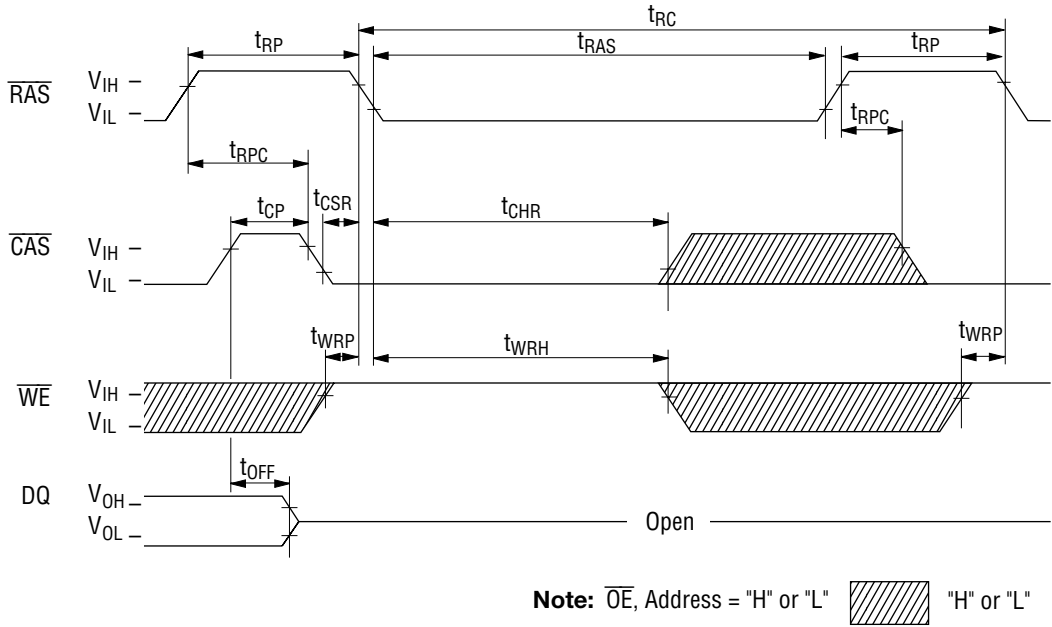
RAS-Only Refresh Cycle



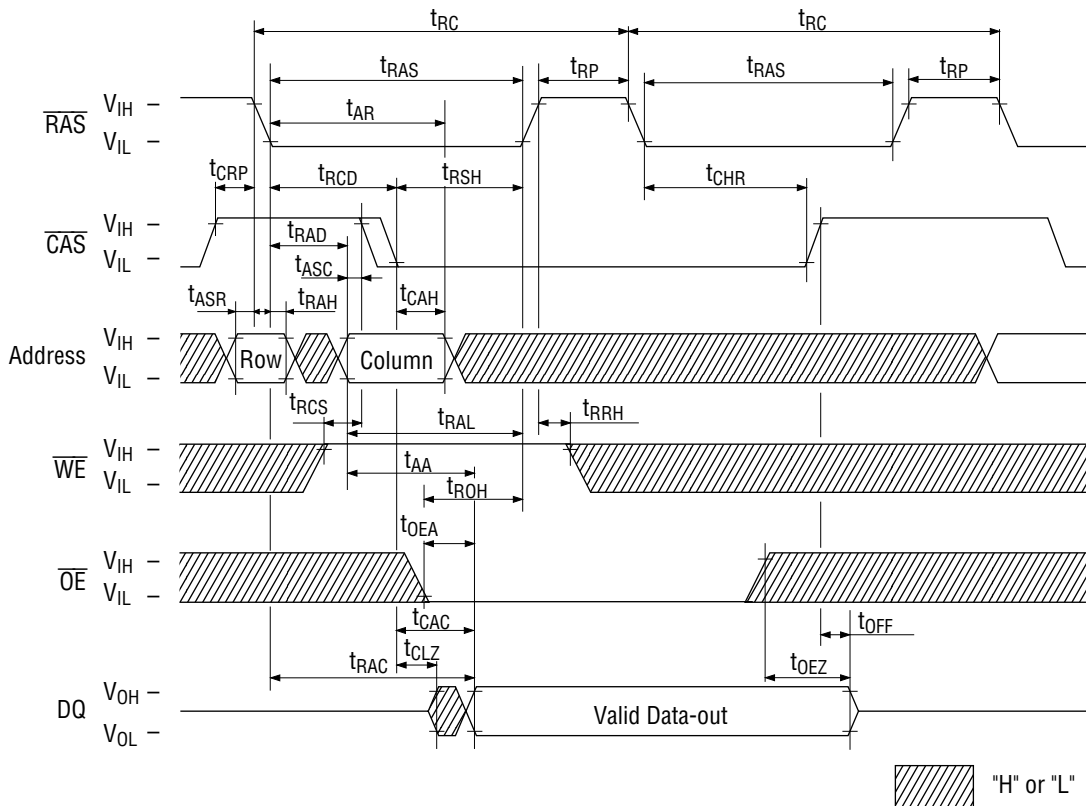
Note: \overline{WE} , \overline{OE} = "H" or "L"

"H" or "L"

CAS before RAS Refresh Cycle

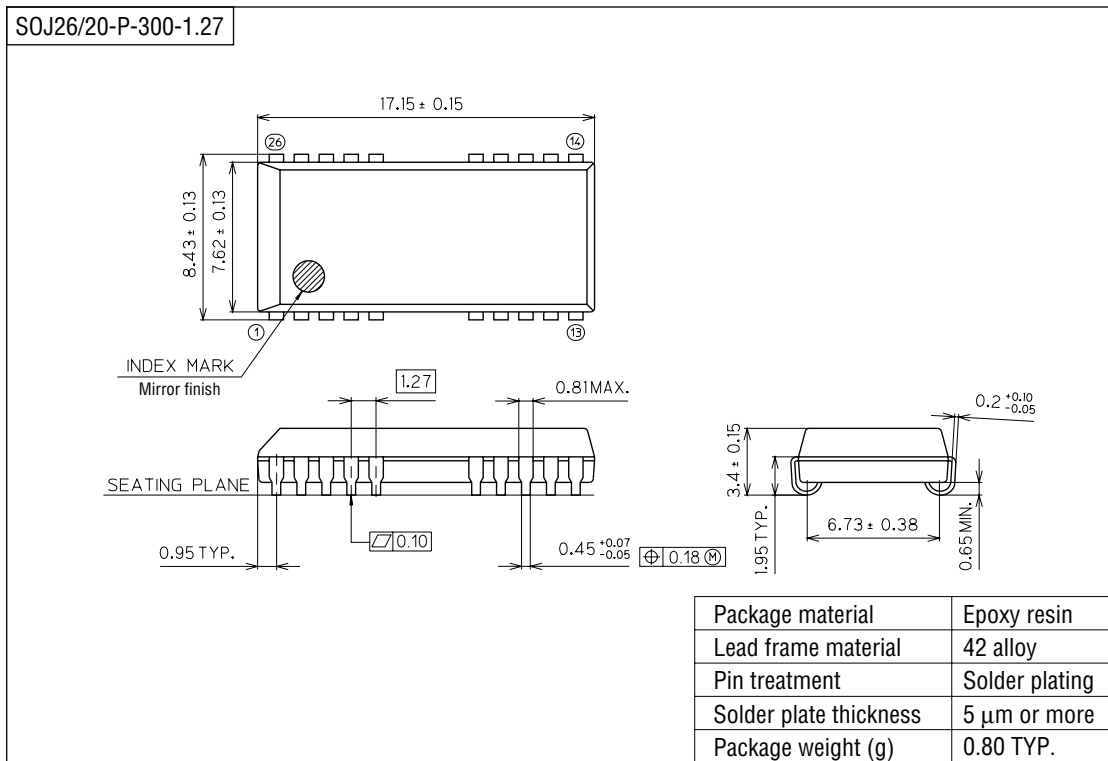


Hidden Refresh Read Cycle



PACKAGE DIMENSIONS

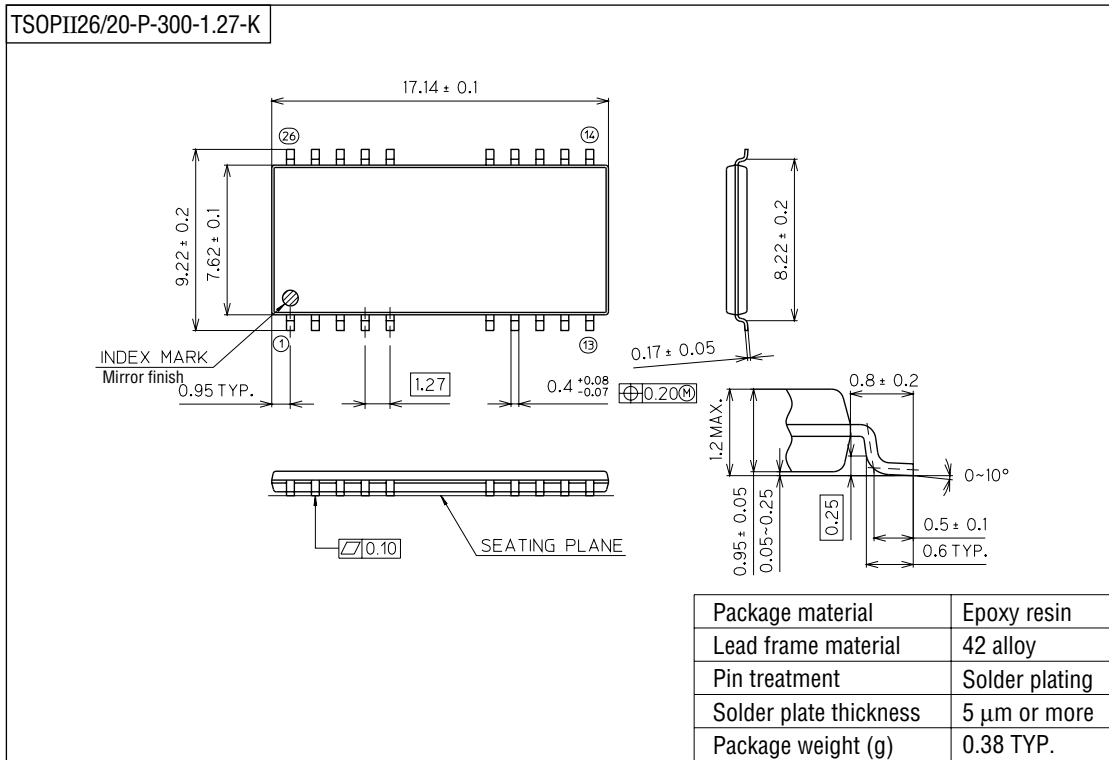
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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