

OKI Semiconductor

MSC23837D-xxBS18/DS18

8,388,608-word x 36-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The MSC23837D-xxBS18/DS18 is an 8,388,608-word x 36-bit CMOS dynamic random access memory module which is composed of eighteen 16Mb DRAMs (4Mx4) in SOJ packages mounted with eighteen decoupling capacitors. This is a 72-pin single in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

FEATURES

- 8,388,608-word x 36-bit organization (ECC)
- 72-pin Single In-Line Memory Module
 MSC23837D-xxBS18 : Gold tab
 MSC23837D-xxDS18 : Solder tab
- Single 5V power supply, $\pm 10\%$ tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 4096cycles/64ms
- Fast page mode, read modify write capability
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Multi-bit test mode capability

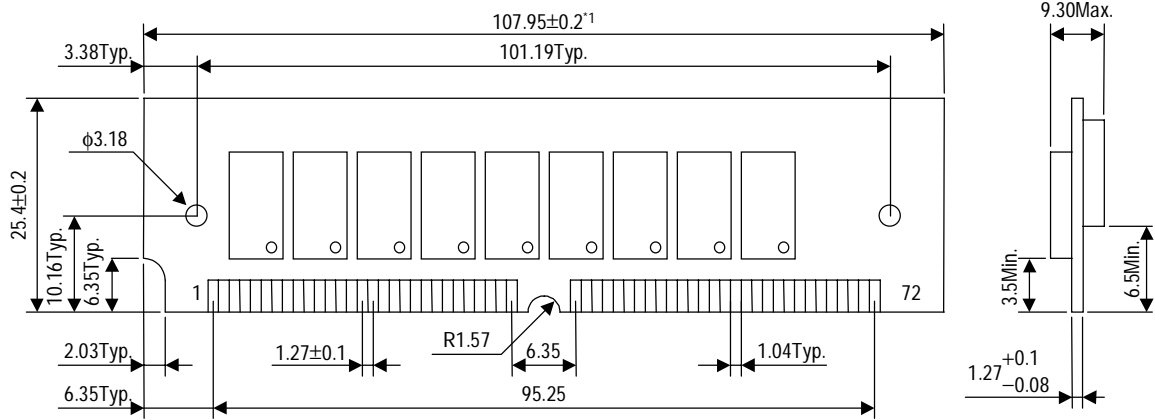
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation (Max.)	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating	Standby
MSC23837D-60BS18/DS18	60ns	30ns	15ns	15ns	110ns	3713mW	99mW
MSC23837D-70BS18/DS18	70ns	35ns	20ns	20ns	130ns	3465mW	

MODULE OUTLINE

MSC23837D-xxBS18/DS18

(Unit : mm)



Note:

1. Tolerance over 12.5mm from board edge is ± 0.5 .

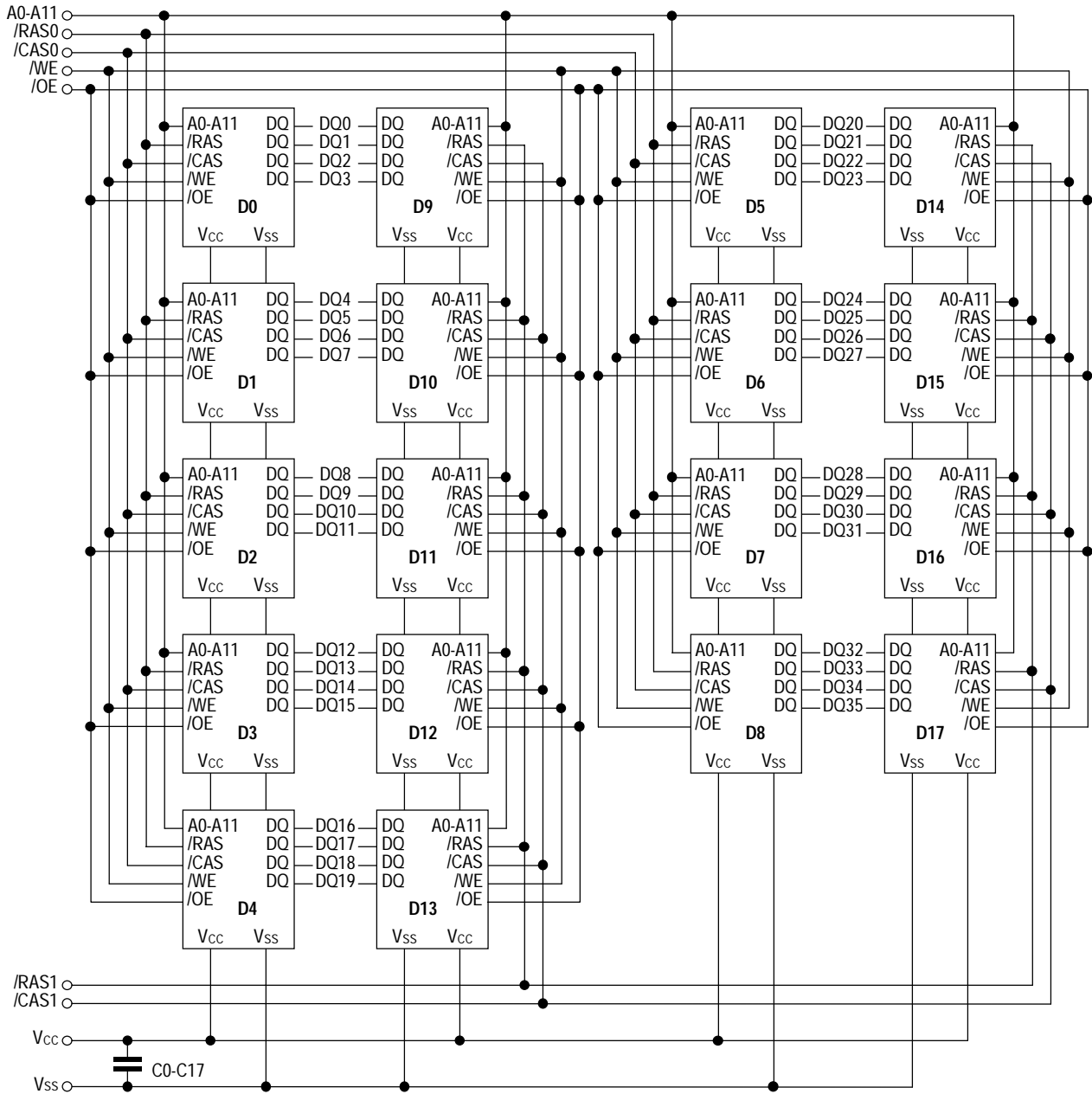
PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	/OE	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V _{SS}	57	DQ30
4	DQ2	22	DQ10	40	/CAS0	58	DQ31
5	DQ3	23	DQ11	41	A10	59	V _{CC}
6	DQ4	24	DQ12	42	A11	60	DQ32
7	DQ5	25	DQ13	43	/CAS1	61	DQ33
8	DQ6	26	DQ14	44	/RAS0	62	DQ34
9	DQ7	27	DQ15	45	/RAS1	63	DQ35
10	V _{CC}	28	A7	46	DQ21	64	NC
11	PD5	29	DQ16	47	/WE	65	NC
12	A0	30	V _{CC}	48	V _{SS}	66	NC
13	A1	31	A8	49	DQ22	67	PD1
14	A2	32	A9	50	DQ23	68	PD2
15	A3	33	NC	51	DQ24	69	PD3
16	A4	34	NC	52	DQ25	70	PD4
17	A5	35	DQ17	53	DQ26	71	NC
18	A6	36	DQ18	54	DQ27	72	V _{SS}

Presence Detect Pins

Pin No.	Pin Name	-60	-70
67	PD1	NC	NC
68	PD2	V _{SS}	V _{SS}
69	PD3	NC	V _{SS}
70	PD4	NC	NC
11	PD5	V _{SS}	V _{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-0.5 to 7.0	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	18	W
Operating Temperature	T _{OPR}	0 to 70	°C
Storage Temperature	T _{STG}	-40 to 125	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A11)	C _{IN1}	—	122	pF
Input Capacitance (/RAS0, /RAS1, /CAS0, /CAS1)	C _{IN2}	—	73	pF
Input Capacitance (/WE, /OE)	C _{IN3}	—	140	pF
I/O Capacitance (DQ0 - DQ35)	C _{I/O}	—	26	pF

DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ C \text{ to } 70^\circ C)$

Parameter	Symbol	Condition	-60		-70		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -5.0mA$	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 4.2mA$	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq 6.5V$; All other pins not under test = 0V	-180	180	-180	180	μA	
Output Leakage Current	I_{LO}	DQ disable $0V \leq V_{OUT} \leq V_{CC}$	-20	20	-20	20	μA	
Average Power Supply Current (Operating)	I_{CC1}	/RAS, /CAS cycling, $t_{RC} = \text{Min.}$	—	675	—	630	mA	1, 2
Power supply current (Standby)	I_{CC2}	/RAS, /CAS = V_{IH}	—	36	—	36	mA	1
		/RAS, /CAS $\geq V_{CC} - 0.2V$	—	18	—	18		
Average Power Supply Current (/RAS only refresh)	I_{CC3}	/RAS cycling, /CAS = V_{IH} , $t_{RC} = \text{Min.}$	—	675	—	630	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	I_{CC6}	/RAS cycling, /CAS before /RAS	—	675	—	630	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	/RAS = V_{IL} , /CAS cycling, $t_{PC} = \text{Min.}$	—	630	—	585	mA	1, 3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while /RAS = V_{IL} .
 3. The address can be changed once or less while /CAS = V_{IH} .

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	ns	
Read Modify Write Cycle Time	t _{RWC}	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	85	—	100	—	ns	
Access Time from /RAS	t _{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from /CAS	t _{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	30	—	35	ns	4, 6
Access Time from /CAS Precharge	t _{CPA}	—	35	—	40	ns	4
Access Time from /OE	t _{OEA}	—	15	—	20	ns	4
Output Low Impedance Time from /CAS	t _{CLZ}	0	—	0	—	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	ns	7
/OE to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	ns	7
Transition Time	t _T	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	64	—	64	ms	
/RAS Precharge Time	t _{RP}	40	—	50	—	ns	
/RAS Pulse Width	t _{RAS}	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	100K	70	100K	ns	
/RAS Hold Time	t _{RSH}	15	—	20	—	ns	
/RAS Hold Time referenced to /OE	t _{ROH}	15	—	20	—	ns	
/CAS Precharge Time (Fast Page Mode)	t _{CP}	10	—	10	—	ns	
/CAS Pulse Width	t _{CAS}	15	10K	20	10K	ns	
/CAS Hold Time	t _{CSH}	60	—	70	—	ns	
/CAS to /RAS Precharge Time	t _{CRP}	5	—	5	—	ns	
/RAS Hold Time from /CAS Precharge	t _{RHCP}	35	—	40	—	ns	
/RAS to /CAS Delay Time	t _{RCD}	20	45	20	50	ns	5
/RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	ns	
Column Address to /RAS Lead Time	t _{RAL}	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	ns	8
Read Command Hold Time referenced to /RAS	t _{RRH}	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Write Command Set-up Time	t _{WCS}	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t _{WP}	10	—	10	—	ns	
/OE Command Hold Time	t _{OEH}	15	—	20	—	ns	
Write Command to /RAS Lead Time	t _{RWL}	15	—	20	—	ns	
Write Command to /CAS Lead Time	t _{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	ns	10
Data-in Hold Time	t _{DH}	10	—	15	—	ns	10
/OE to Data-in Delay Time	t _{OED}	15	—	20	—	ns	
/CAS to /WE Delay Time	t _{CWD}	40	—	50	—	ns	9
Column Address to /WE Delay Time	t _{AWD}	55	—	65	—	ns	9
/RAS to /WE Delay Time	t _{RWD}	85	—	100	—	ns	9
/CAS Precharge /WE Delay Time	t _{CPWD}	60	—	70	—	ns	9
/CAS Active Delay Time from /RAS Precharge	t _{RPC}	5	—	5	—	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t _{CSR}	10	—	10	—	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t _{CHR}	10	—	10	—	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t _{WRP}	10	—	10	—	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	t _{WRH}	10	—	10	—	ns	
/RAS to /WE Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	ns	
/RAS to /WE Hold Time (Test Mode)	t _{WTH}	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.
 2. The AC characteristics assumes $t_T = 5$ ns.
 3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100pF.
 5. Operation within the $t_{RCD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then the access time is controlled by t_{CAC} .
 6. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then the access time is controlled by t_{AA} .
 7. $t_{OFF}(\text{Max.})$ and $t_{OEZ}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{Min.})$, $t_{RWD} \geq t_{RWD}(\text{Min.})$, $t_{AWD} \geq t_{AWD}(\text{Min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{Min.})$, then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the /CAS leading edge in an early write cycle, and to the /WE leading edge in an /OE control write cycle, or a read modify write cycle.
 11. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 4-bit parallel test function. CA0 and CA1 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by a /RAS only refresh or /CAS before /RAS refresh cycle.
 12. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.