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OKI Semiconductor

This version: Nov. 1997
Previous version: Jul. 1996

MSC1230

111-Bit 2/3-Duty Controller/Driver with Digital Dimming Function

GENERAL DESCRIPTION

The MSC1230 is a Bi-CMOS display driver with digital dimming function. It enables switching between 1/3-duty vacuum fluorescent (VF) display tube and universal VF display tube by pin control.
The MSC1230 consists of a 112-bit shift register, a 111-bit latch, a 10-bit digital dimming circuit, 37 segment drivers, and 3 grid drivers.
The MSC1230 provides an interface with a microcomputer only by three signal lines: $\overline{CS}$, DATA-IN, and CLOCK.
By using the chip select function, the DATA-IN and CLOCK signal lines can be shared by other peripheral circuits.

FEATURES

- Power supply voltage : V_{DD}=8 V to 18 V (built-in 5 V regulator for logic circuit)
- Operating temperature range : Ta=–40 °C to +85 °C
- 37-segment driver outputs : I_{OH}=–6 mA at $V_{OH} = V_{DD}$ –0.8 V
- 3-grid driver outputs : I_{OH}=–30 mA at $V_{OH} = V_{DD}$ –0.8 V
- Built-in digital dimming circuit (10-bit resolution)
- Switchable between 1/3-duty VF display tube and universal VF display tube*
  When SEL pin is left open : Selects universal VF display tube (The grids GRID1, GRID2, and GRID1+GRID2 are turned on repeatedly in this order)
  When SEL pin is used at 0 V : Selects 1/3-duty VF display tube (The grids GRID1, GRID2, and GRID3 are turned on repeatedly in this order)
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K)(Product name: MSC1230GS-2K)

* A universal VF display tube is a display tube for which, like a gate array, the user can freely design characters and patterns on the master layer (grid). (Pattern can be created without gaps between grids.)
Since the outline dimensions of the display tube and the grid layout are predetermined, desired patterns can be displayed in a short time.
The universal VF display tube is used for the display parts for audio equipment, household appliances, and automobile equipment.

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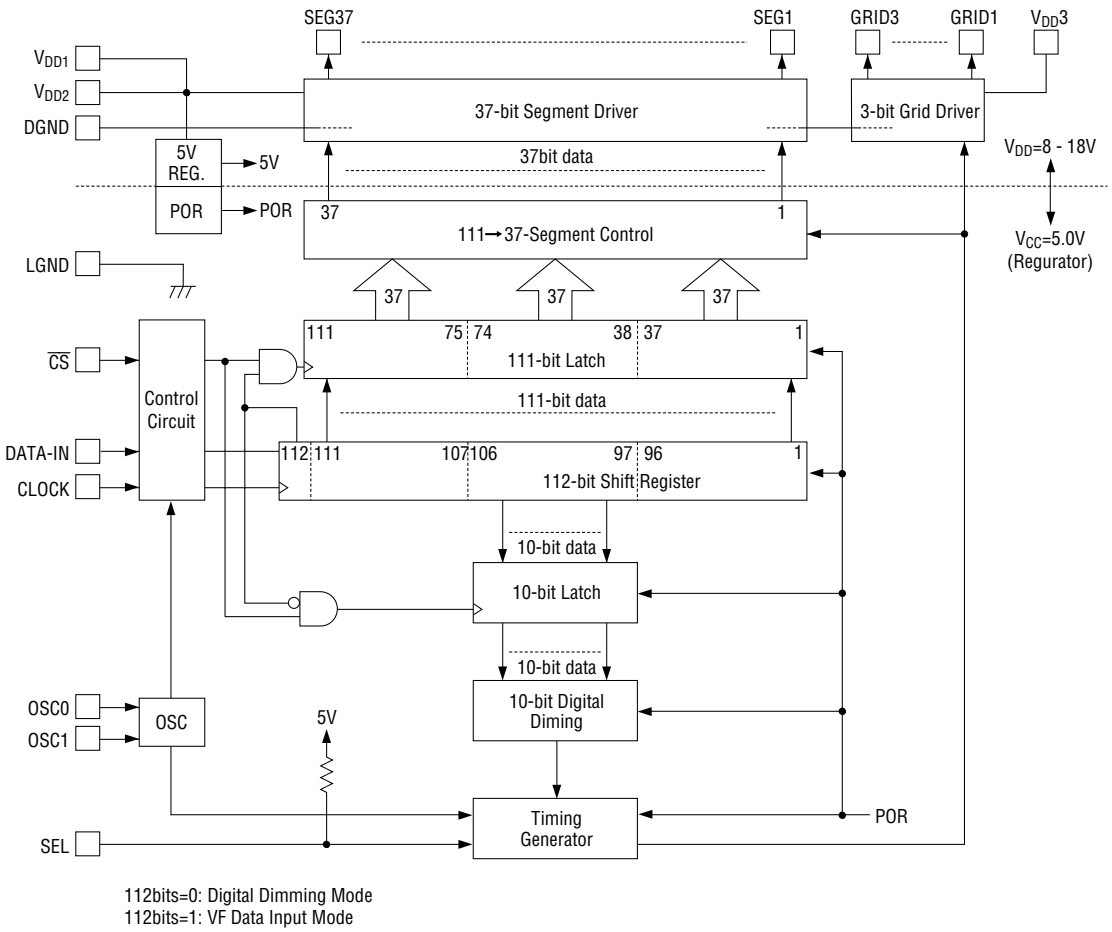
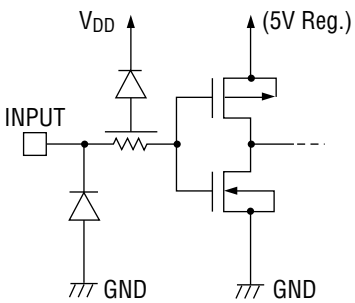
BLOCK DIAGRAM

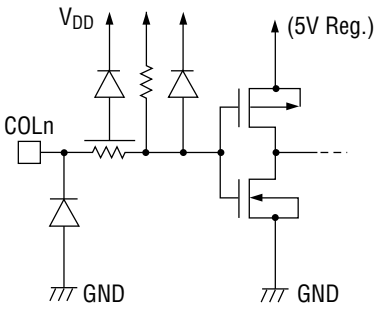


INPUT AND OUTPUT CONFIGURATION

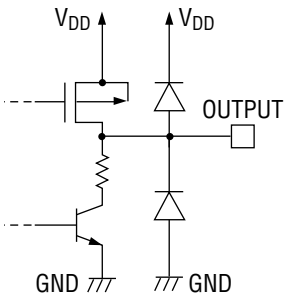
● Schematic Diagram 1 of Logic Portion Input Circuit



● Schematic Diagram 2 of Logic Portion Input Circuit



● Schematic Diagram of Driver Output Circuit



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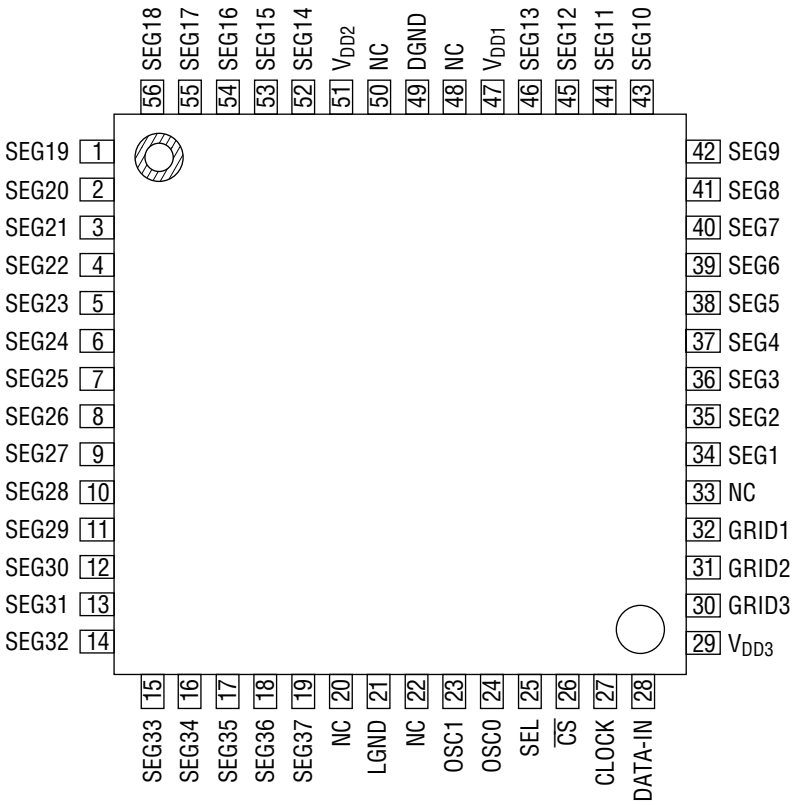
PIN CONFIGURATION (TOP VIEW)



NC: No connection

56-Pin Plastic QFP

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PIN DESCRIPTION

Pin	Symbol	Type	Decription
34 to 46, 52 to 56, 1 to 19	SEG1 to 37	O	Output pins for segment signals for driving VF display tube.
30 to 32	GRID1 to 3	O	Output pins for grid signals for driving VF display tube. The GRID3 output is not used when the universal VF display tube is used.
25	SEL	I	When at a "L" level, this pin selects 1/3-duty VF display tube. When at a "H" level (or when used in the open state), this pin selects universal VF display tube.
28	DATA-IN	I	Pin for series data input from microprocessor. Data is input to the shift register on the rising edge of the CLOCK signal.
27	CLOCK	I	Serial clock input pin. Data is input through the DATA-IN pin at the rising edge of the serial clock.
24	OSC0	I	RC oscillator connecting pins. Connect a resistor between the OSC1 and OSC0 pins and a capacitor between the OSC0 pin and the ground.
23	OSC1	O	
26	$\overline{CS}$	I	Chip select input pin. Circuit operation is valid when this pin is at a "L" level.
47 51 29	V_{DD1} V_{DD2} V_{DD3}	—	Power supply pins. When using these pins, connect each of them to the power supply.
49	DGND	—	Ground pins for driver and logic. These pins can be connected with each other when they are used.
21	LGND	—	

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings	Unit
Supply Voltage	V_{DD}	—	–0.3 to +20	V
Input Voltage	V_{IN}	All inputs	–0.3 to +6.0	V
Storage Temperature	T_{STG}	—	–65 to +150	°C
Power Dissipation	P_D	Ta=85°C	400	mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	—	8	—	18	V
High Level Input Voltage (1)	V_{IH1}	All inputs except OSC0	3.8	—	5.5	V
High Level Input Voltage (2)	V_{IH2}	OSC0	4.5	—	5.5	V
Low Level Input Voltage (1)	V_{IL1}	All inputs except OSC0	0.0	—	0.8	V
Low Level Input Voltage (2)	V_{IL2}	OSC0	0.0	—	0.5	V
Clock Frequency	f_C	—	—	—	250	kHz
Oscillation Frequency	f_{OSC}	R=4.7 kΩ, C=10 pF	—	3.2	—	MHz
Frame Frequency	f_{FR}	f_{OSC}=3.2 MHz	—	260	—	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

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ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Input Voltage (1) *1	V_{IH1}	—	3.8	5.5	V
"H" Input Voltage (2) *2	V_{IH2}	—	4.5	5.5	V
"L" Input Voltage (1) *1	V_{IL1}	—	0.0	0.8	V
"L" Input Voltage (2) *2	V_{IL2}	—	0.0	0.5	V
"H" Input Current (1) *3	I_{IH1}	V_{IH}=5 V	–5	5	µA
"H" Input Current (2) *4	I_{IH2}	V_{IH}=5 V	–200	200	µA
"L" Input Current (1) *3	I_{IL1}	V_{IL}=0 V	–5	5	µA
"L" Input Current (2) *4	I_{IL2}	V_{IL}=0 V	–0.6	–0.1	mA
"H" Output Voltage (1) *5	V_{OH1}	V_{DD}=9.5 V I_{OH1}=–6 mA	V_{DD} –0.8	—	V
"H" Output Voltage (2) *6	V_{OH2}	V_{DD}=9.5 V I_{OH2}=–30 mA	V_{DD} –0.8	—	V
"L" Output Voltage *7	V_{OL1}	V_{DD}=9.5 V I_{OL1}=500 µA	—	2	V
	V_{OL2}	V_{DD}=9.5 V I_{OL2}=200 µA	—	1	V
	V_{OL3}	V_{DD}=9.5 V I_{OL3}=2 µA	—	0.3	V
Supply Current	I_{DD}	f_{osc}=3.2 MHz no Load	—	13	mA

*1 All input pins except OSC0
*2 OSC0 pin
*3 $\overline{CS}$, CLOCK and DATA-IN pins
*4 SEL pin
*5 SEG1 to SEG37 pins
*6 GRID1 to GRID3 pins
*7 SEG1 to SEG37 and GRID1 to GRID 3 pins

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AC Characteristics

(Ta=–40 to +85°C, V_{DD}=8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	f_{OSC}	R=4.7 kΩ , C=10 pF	2	4.4	MHz
External Input Frequency into OSC0	f_{OSCI}	External input only	2.7	3.7	MHz
Clock Frequency	f_C	—	—	250	kHz
Clock Pulse Width	t_{CW}	—	1.3	—	µs
DATA Setup Time	t_{DS}	—	1	—	µs
DATA Hold Time	t_{DH}	—	200	—	ns
$\overline{CS}$ Pulse Width	t_{CSW}	—	8	—	µs
$\overline{CS}$ Off Time	t_{CSL}	—	32	—	µs
$\overline{CS}$ Setup Time $\overline{CS}$-Clock Time	t_{CSS}	—	2	—	µs
$\overline{CS}$ Hold Time Clock-$\overline{CS}$ Time	t_{CSH}	—	2	—	µs
$\overline{CS}$-All Data Output Delay	t_{ODS}	C_I=100 pF	—	8	µs
Slew Rate (All Drivers)	t_R	C_I=100 pF t=20% to 80% or 80% to 20%	—	5	µs
$\overline{CS}$ Time at Power-on	t_{PCS}	—	300	—	µs
Hold Time at Power-off	t_{POF}	When monuted on the unit V_{DD}=0.0 V	5	—	ms
Rise Time at Power-on	t_{PRZ}	When monuted on the unit	—	100	µs

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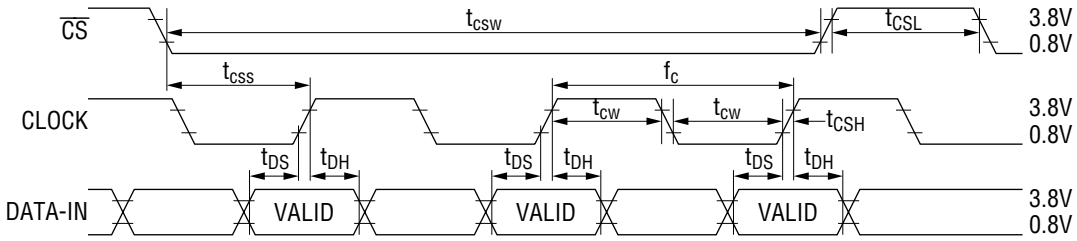

Figure 1. Data Input Timing

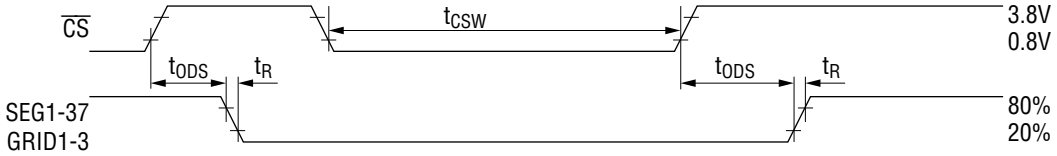

Figure 2. SEG or GRID Driver Output Timing

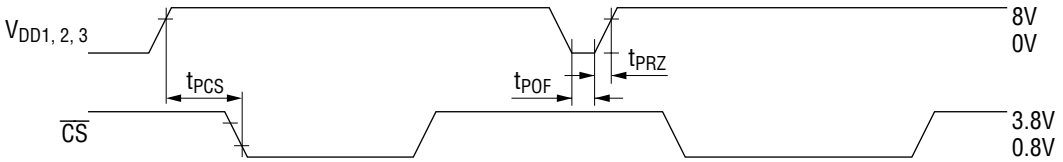

Figure 3. Power-on Timing

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FUNCTIONAL DESCRIPTION

Power-on Reset

When power is turned on, the IC is initialized by the internal power-on reset circuit. The status of the internal circuit after initialization is as follows:

– The contents of the shift registers and latches are set to "0".
– The digital dimming duty cycle is set to "0".

Data Input

Data input to the DATA-IN pin is valid only when the $\overline{CS}$ pin is at a "L" level.
The input data to DATA-IN is shifted into the shift registers on the rising edge of the clock. The data is automatically loaded to the latches on the rising edge of the $\overline{CS}$ pin.
When M0 = "1", the IC enters the display data input mode and a total of 112 bits of data are input.
When M0 = "0", the IC enters the digital dimming data input mode and a total of 16 bits of data are input.

[Data Format]

1) Display Data Input Mode

Input Data	:	112 bits
VF Display Data	:	111 bits
Mode Select Data (M0)	:	1 bit

Bit	112	111	110	....	97	96	95	94	93	92	91	....	4	3	2	1	First in
	M0	D111	D110	....	D97	D96	D95	D94	D93	D92	D91	....	D4	D3	D2	D1	
	Mode Data (1 bit)	← Display Data (111 bits) →															

2) Bit correspondence between segment outputs and shift registers

	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	SEG
	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	G1
BIT	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	G2
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	G3

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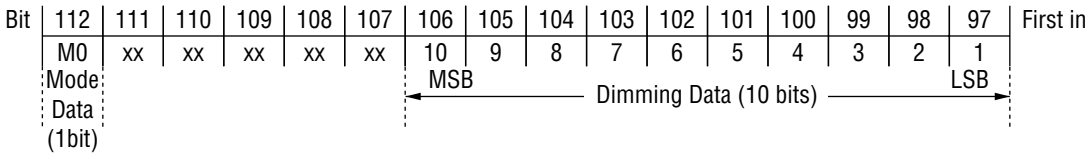
3) Input Format for VF data

Byte	c7	c6	c5	c4	c3	c2	c1	c0
1	D8	D7	D6	D5	D4	D3	D2	D1
2	D16	D15	D14	D13	D12	D11	D10	D9
3	D24	D23	D22	D21	D20	D19	D18	D17
4	D32	D31	D30	D29	D28	D27	D26	D25
5	D40	D39	D38	D37	D36	D35	D34	D33
6	D48	D47	D46	D45	D44	D43	D42	D41
7	D56	D55	D54	D53	D52	D51	D50	D49
8	D64	D63	D62	D61	D60	D59	D58	D57
9	D72	D71	D70	D69	D68	D67	D66	D65
10	D80	D79	D78	D77	D76	D75	D74	D73
11	D88	D87	D86	D85	D84	D83	D82	D81
12	D96	D95	D94	D93	D92	D91	D90	D89
13	D104	D103	D102	D101	D100	D99	D98	D97
14	M0	D111	D110	D109	D108	D107	D106	D105

4) Digital Dimming Data Input Mode
This data consists of 10 bits.
The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99%) for each grid.
The 10-bit digital dimming data is input from the LSB.
Input Data : 16 bits
Digital Dimming Data : 10 bits
Mode Select Data : 1 bit



(MSB)					INPUT DATA					(LSB)	DUTY CYCLE
0	0	0	0	0	0	0	0	0	0		0/1024
0	0	0	0	0	0	0	0	0	1		1/1024
					⋮						⋮
1	1	1	1	1	1	1	0	0	0		1016/1024
					⋮						⋮
1	1	1	1	1	1	1	1	1	1		1016/1024

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5) Input Format for Dimming Data

Byte	c7	c6	c5	c4	c3	c2	c1	c0
1	8	7	6	5	4	3	2	1
2	M0	xx	xx	xx	xx	xx	10	9

6) Function Mode

M0	FUNCTION
0	Display Data Input Mode
1	Digital Dimming Data Input Mode

GRID/SEG Driver Operation and Digital Dimming

Figures 4 and 5 show the timing for the GRID and SEG drivers in universal VFD mode and 1/3 duty VFD mode, respectively.
Figure 6 shows an example of timing for digital dimming operation in 1/3 duty VFD mode. (When the duty cycle in the dimming data is 508/1024)

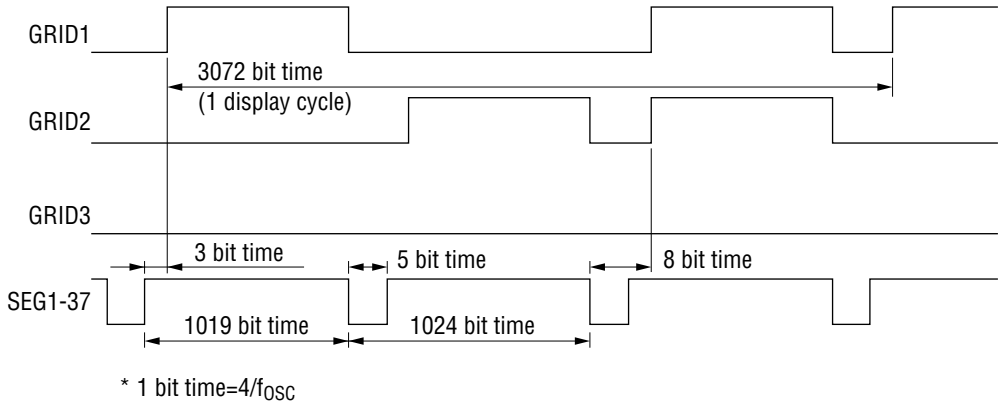

Figure 4. Duty Cycle Timing (Universal VFD Mode)

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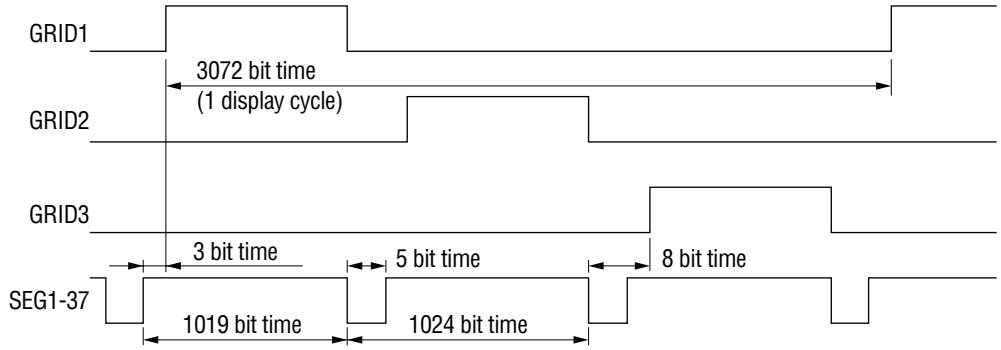

Figure 5. Duty Cycle Timing (1/3 Duty Mode)

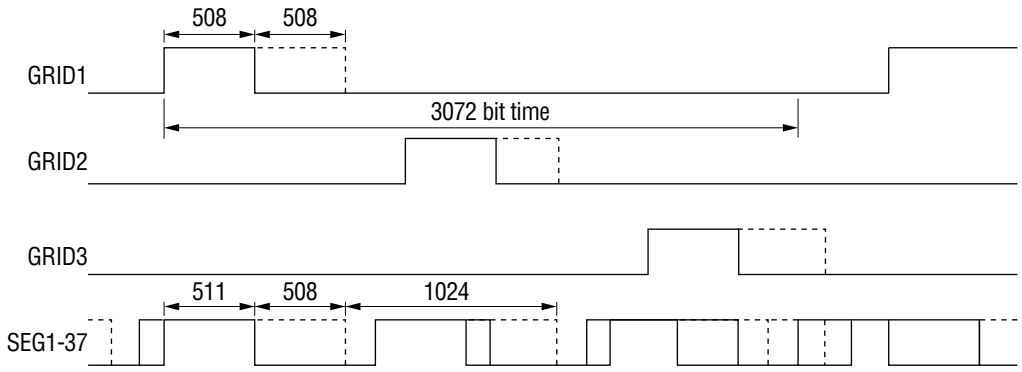

Figure 6. Duty Cycle Timing (1/3 Duty Mode)

(When digital dimming data is changed from 3F8H to 1FFH)

1016 bit time ↑ 511 bit time ↑

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PACKAGE DIMENSIONS

(Unit : mm)

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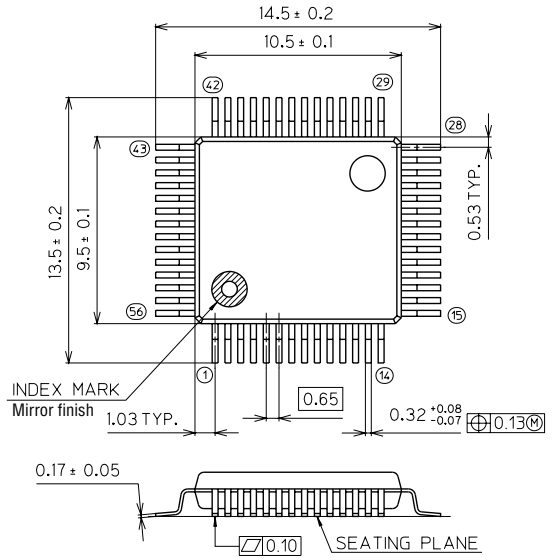

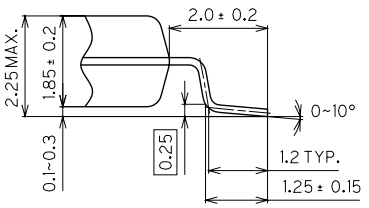

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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