

OKI Semiconductor

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MR27V402D

262,144-Word x 16-Bit or 524,288-Word x 8-Bit

Production Programmed Read Only Memory (P2ROM)

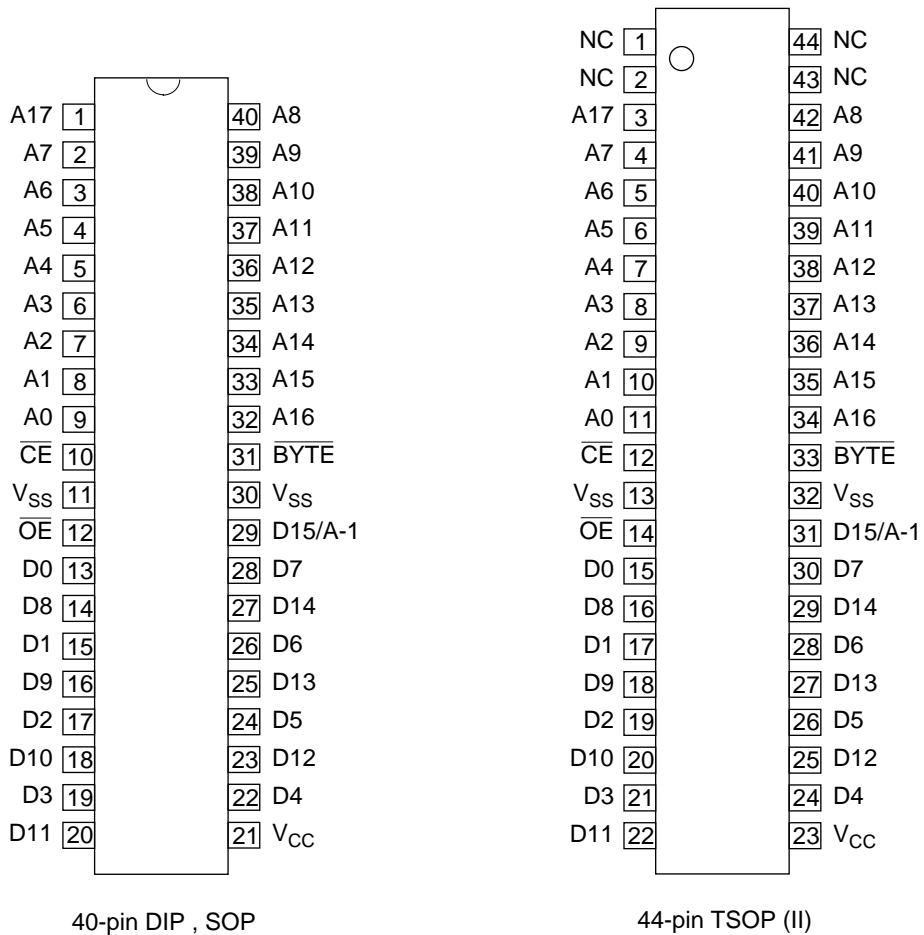
DESCRIPTION

The MR27V402D is a 4Mbit Production Programmed Read-Only Memory (P2ROM) whose configuration can be electrically switched between 262,144 word x 16bit and 524,288 word x 8bit. The MR27V402D operates on a single +3V-3.3V power supply and is TTL compatible. Since the MR27V402D operates asynchronously, external clocks are not required, making this device easy-to-use. The MR27V402D is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 40-pin DIP, 40-pin SOP or 44-pin TSOP packages.

FEATURES

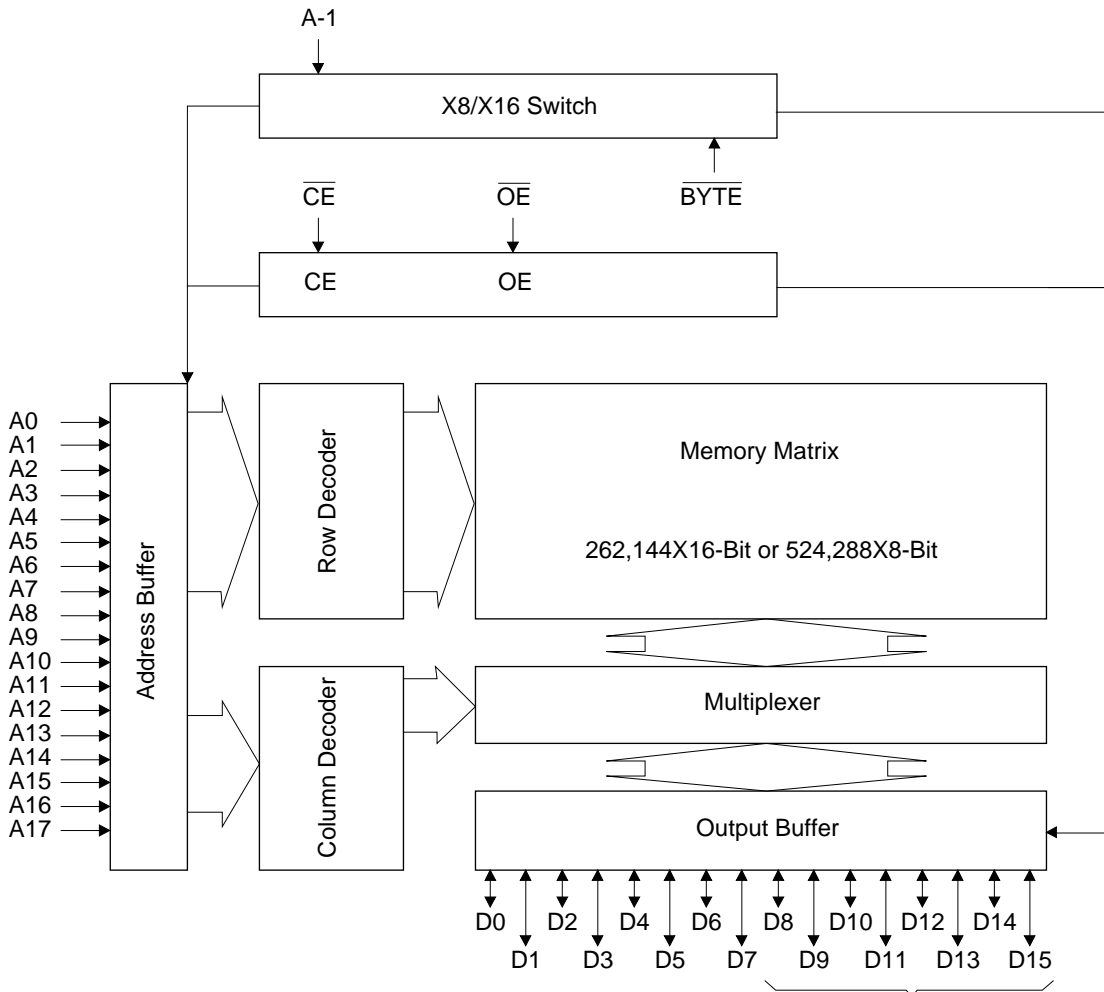
- 262,144 word x 16bit / 524,288 word x 8bit electrically switchable configuration
- Single +3V-3.3V power supply
- Access time 80ns access time (Vcc=+3V)
 70ns access time (Vcc=+3.3V)
- Input / Output TTL compatible
- Three-state output
- Packages
 - 40-pin plastic DIP (DIP40-P-600-2.54) (Product name : MR27V402D-xxRP)
 - 40-pin plastic SOP (SOP40-P-525-1.27-K) (Product name : MR27V402D-xxMP)
 - 44-pin plastic TSOP (TSOP II 44-P-400-0.80-K) (Product name : MR27V402D-xxTP)

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0-A17	Address input
D0-D14	Data output
\overline{CE}	Chip enable
\overline{OE}	Output enable
V_{CC}	Power supply voltage
V_{SS}	GND
BYTE	Mode switch
NC	Non connection

BLOCK DIAGRAM



In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

FUNCTION TABLE

MODE	\overline{CE}	\overline{OE}	\overline{BYTE}	V_{CC}	D0 - D7	D8 - D14	D15/A-1
READ (16-Bit)	L	L	H	3.0V to 3.3V	D_{OUT}		
READ (8-Bit)	L	L	L		D_{OUT}	Hi-Z	L/H
OUTPUT DISABLE	L	H	H		Hi-Z		*
			L		Hi-Z		*
STAND-BY	H	*	H	Hi-Z		*	
			L	Hi-Z		*	

*: Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}		-55 to 125	°C
Input voltage	V_I	relative to V_{SS}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	V_{CC}		-0.5 to 5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	$V_{CC}=2.7V-3.6V$	2.7	-	3.6	V
Input "H" level	V_{IH}		2.2	-	$V_{CC}+0.5^*$	V
Input "L" level	V_{IL}		-0.5**	-	0.6	V

Voltage is relative to V_{SS} * : $V_{CC}+1.5V$ (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

ELECTRICAL CHARACTERISTICS (Read operation)**DC Characteristics 1**(V_{CC}=3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I =0 to V _{CC}	-	-	10	μA
Output leakage current	I _{LO}	V _O =0 to V _{CC}	-	-	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I _{CCST}	$\overline{CE}=V_{IH}$	-	-	1	mA
V _{CC} power supply current (Read)	I _{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc=80ns	-	-	25	mA
Input "H" level	V _{IH}	-	2.2	-	V _{CC} +0.5*	V
Input "L" level	V _{IL}	-	-0.5**	-	0.6	V
Output "H" level	V _{OH}	I _{OH} =-400uA	2.4	-	-	V
Output "L" level	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V

Voltage is relative to V_{SS}* : V_{CC}+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

DC Characteristics 2(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I =0 to V _{CC}	-	-	10	μA
Output leakage current	I _{LO}	V _O =0 to V _{CC}	-	-	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I _{CCST}	$\overline{CE}=V_{IH}$	-	-	1	mA
V _{CC} power supply current (Read)	I _{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc=70ns	-	-	30	mA
Input "H" level	V _{IH}	-	2.2	-	V _{CC} +0.5*	V
Input "L" level	V _{IL}	-	-0.5**	-	0.6	V
Output "H" level	V _{OH}	I _{OH} =-400uA	2.4	-	-	V
Output "L" level	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V

Voltage is relative to V_{SS}* : V_{CC}+1.5V (Max.) when pulse width of overshoot is less than 10nS.

** : -1.5V (Min.) when pulse width of undershoot is less than 10nS.

AC Characteristics 1

($V_{CC}=3V\pm 0.3V$, $T_a=0$ to $70^{\circ}C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	T_C	-	80	-	ns
Address access time	T_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	80	ns
\overline{CE} access time	T_{CE}	$\overline{OE}=V_{IL}$	-	80	ns
\overline{OE} access time	T_{OE}	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T_{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T_{OHZ}	$\overline{CE}=V_{IL}$	0	20	ns
Output hold time	T_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	50pF
Output timing reference level	-----	0.8V/2.0V

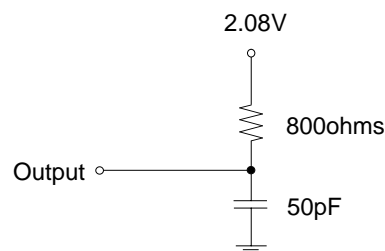
AC Characteristics 2

($V_{CC}=3.3V\pm 0.3V$, $T_a=0$ to $70^{\circ}C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	T_C	-	70	-	ns
Address access time	T_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	70	ns
\overline{CE} access time	T_{CE}	$\overline{OE}=V_{IL}$	-	70	ns
\overline{OE} access time	T_{OE}	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T_{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T_{OHZ}	$\overline{CE}=V_{IL}$	0	20	ns
Output hold time	T_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

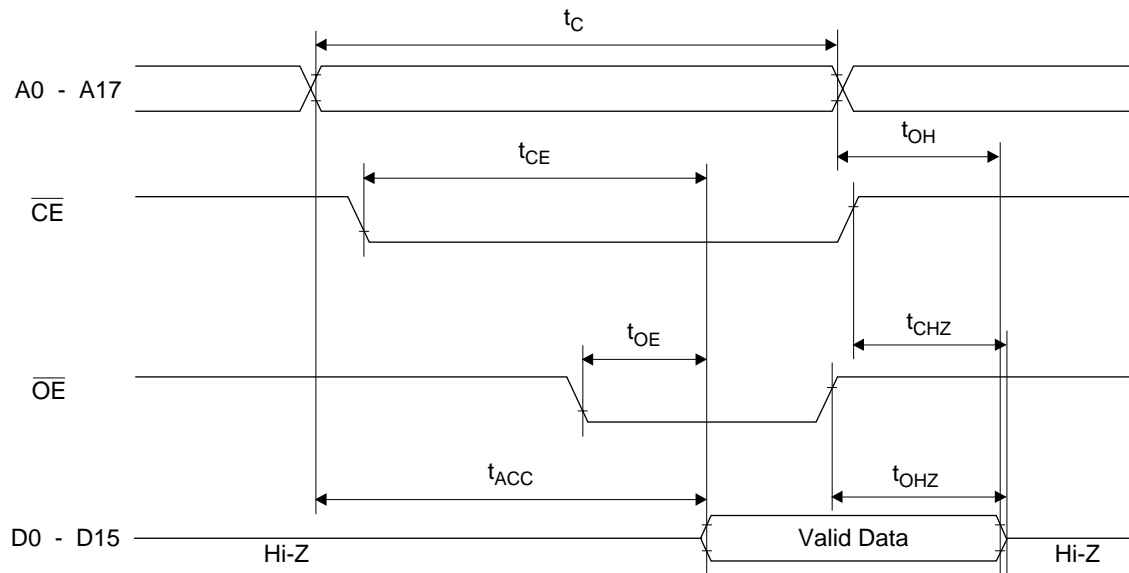
Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	50pF
Output timing reference level	-----	0.8V/2.0V

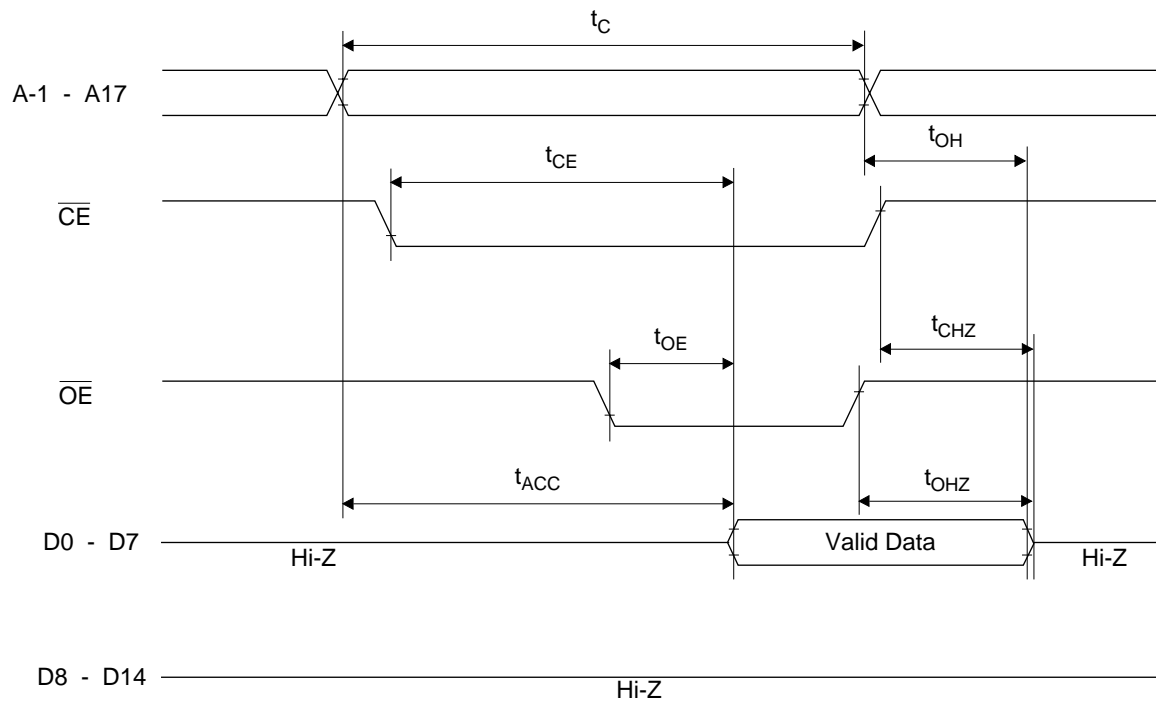


TIMING CHART (READ CYCLE)

16-Bit Read Mode ($\overline{\text{BYTE}}=\text{V}_{\text{IH}}$)



8-Bit Read Mode ($\overline{\text{BYTE}}=\text{V}_{\text{IL}}$)



PIN Capacitance(V_{CC}=3.3V, T_a=25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C _{IN1}	V _I =0V	-	-	8 (10)	pF
BYTE	C _{IN2}		-	-	60	
Output	C _{OUT}	V _O =0V	-	-	10 (12)	

() : DIP only