Oki Semiconductor

ML53101 8-Port Fast Ethernet Controller

10/100 Mbps 8-Port Media Access Controller

The ML53101 is an 8-Port Ethernet / Fast Ethernet Media Access Controller (MAC8110) with 8 MII interfaces on one side and with shared first-in, first-out queue (FIFO) and peripheral component interconnect (PCI) control interfaces on the other side, as shown in the block diagram of Figure 1.

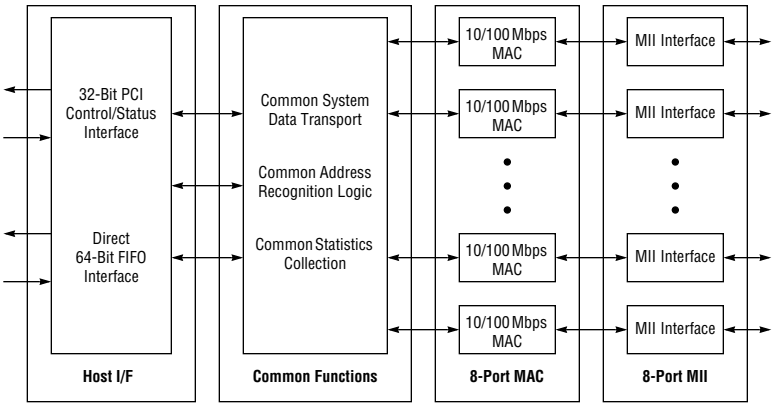

Figure 1. Block Diagram of the Complete 10/100 Mbps MAC

The basic MAC device:

- Performs all IEEE 802.3 layer functions for 10-Mbps and 100-Mbps MAC.
- Integrates full-duplex and half-duplex flow control for high performance connectivity between Ethernet switches and end stations.
- Is fabricated in 3.3-V complementary metal-oxide semiconductor (CMOS) technology .
- Is packaged into a 352-pin ball grid array (BGA) package.

FEATURES

- 8-port full-duplex 10/100 Mbps MAC in one single device.
- 8 independent MACs and MIIs.
- Ports independently selectable for 10/100 Mbps.
- Full CMIB Statistics Information Base for remote monitoring (RMON) support.
- Shared 64-bit, 66-MHz FIFO Interface for TX and RX data transfer.
- FIFO bus bandwidth exceeds 4 Gbps.
- Shared 32-bit PCI interface for control, status, and statistics information exchange.
- RX Frame Status can be appended at the end of a frame as an additional 64-bit data word on the FIFO Interface.
- Independent dual-port RX and TX FlFOs for each MAC.
- Programmable FIFO burst size of 32/64 bytes.
- Transmit FIFO ready signal per channel using the TX FIFO burst size as threshold.
- Auto retransmit of transmit data upon tranmist collision condition.
- Receive FIFO ready signal per channel using the RX FIFO burst size as threshold or end of frame (EOF).
- Receive data ready hold-off enable for minimum receive packet size (runt removal).
- Byte Valid signal for each byte in the 64-bit data word for TX and RX.
- Full-duplex flow control (conformant to the IEEE 802.3x Ethernet standards proposal). Pin-initiated Pause Frame with preprogrammed Pause Time.
- Half-duplex flow control using Carrier Sense (deferral instead of collision).

  Pin-controlled carrier (jam) assertion independently per port.
- 7-wire interface, selectable for connecting to a low-cost l0-Mbps physical layer or for using an MII interface to connect to a 10- or l00-Mbps physical layer using auto-negotiation.
- HUGE Packet Enable on a per-packet basis, always, or never.
- CRC Recalculation Enable on a per-packet basis, always, or never.
- Supports 802.3i, 802.3u, 802.3x, 802.3y and 802.3 IEEE standards as well as 8802-3 ANSI Ethernet standards.
- Technology used is CMOS 0.35 µm, 3.3 V.
- Package is a 352-pin BGA.

SIGNAL DESCRIPTIONS

The signal descriptions for the various MAC interfaces are summarized in the following sections. Active-LOW signals are denoted with an asterisk (*) after the signal name (for example, CS*).

FIFO Bus Interface

Table 1 FIFO Bus Interface Signals

Signal Name	Description	I/O
RXDRDY[7:0]	**Receive Data Ready.** The MAC8110 asserts these signals to indicate that a threshold number of bytes are available in the receive FIFO on the indicated port.	TTL Output
TXDRDY[7:0]	**Transmit Data Ready.** The MAC8110 asserts these signals to indicate that a threshold number of locations are available in the transmit FIFO for new data on the indicated port.	TTL Output
ADDR[2:0]	**Port Address.** The host selects a FIFO port for access on the FIFO bus by placing the binary encoded port address on these inputs.	TTL Input
CS*	**Chip Select.** This pin is asserted LOW when the device is selected for data transfer.	TTL Input
BVAL[7:0]	**Byte Valid.** The FIFO data originator indicates the validity of respective data bytes within the 64-bit FIFO transfer using these signals.	TTL I/O
R/W*	**FIFO Read/FIFO Write.** The host asserts this signal to indicate the data direction for a FIFO bus transfer. When the pin is HIGH a read is indicated; when LOW, the pin indicates a write operation.	TTL Input
TREN*	**Transfer Enable.** Enables FIFO transfers.	TTL Input
SOF	**Start of Frame.** The FIFO data originator asserts this signal HIGH to indicate that the current word being written or read is the first word in the frame.	TTL I/O
EOF	**End of Frame.** The FIFO data originator asserts this signal HIGH to indicate that the current word being written or read is the last word in the frame.	TTL I/O
DATA[63:0]	**FIFO Data Bus.** Carries data for the FIFO interface.	TTL I/O
RESET	**Reset.** When the host asserts this signal HIGH, a general reset of the entire chip occurs.	TTL Input
FCLK	**FIFO Bus Clock.** The host will provide the FIFO bus clock; maximum clock rate equals 66 MHz	TTL Input
CRC_EN	**CRC Enable.** When asserted, the CRC_EN signal indicates that the MAC8110 must recalculate the frame's CRC value.	TTL Input
HUGE_EN	**Huge Enable.** Enables the passage of oversized frames through the MAC8110.	TTL Input
PAD_EN	**Pad Enable.** When asserted, PAD_EN indicates that the MAC8110 must pad undersized frames that pass through it.	TTL Input
FCTL_Start	**Flow Control Start.** Initiates the start of a flow control sequence in both Full-Duplex and Half-Duplex modes.	TTL Input
FCTL_End	**Flow Control End.** Terminates a flow control sequence in Half-Duplex Mode.	TTL Input

PCI Bus Interface

Table 2 PCI Bus Interface Signals

Signal Name	Description	I/O
PCI_AD[31:0]	**PCI Address/Data Bus.** Connect to the AD[31:0] pins of the PCI bus interface.	TTL I/O
PCI_CBE*[3:0]	**PCI Bus Command/Byte Enable.** Connect to the C/BE*[3:0] pins of the PCI bus. During a transaction's address phase, these signals define the bus command. During the data phase, they determine which byte carries valid data.	TTL Input
PCI_PAR	**PCI Parity.** Connects to the PAR PCI bus signal and indicates even parity across AD[31:0] and PCC/PCBE*[3:0]	TTL Output
PCI_CLK	**PCI Clock.** Provides timing for all transactions on the PCI bus. Its frequency can range from 0 Hz to 33 MHz.	TTL Input
PCI_RST*	**PCI Bus Reset.** Used to bring all PCI-specific registers, controls, and signals to a consistent level; also acts as a general chip reset to all internal logic of the chip.	TTL Input
PCI_FRAME*	**PCI Cycle Frame.** Is driven by the current master to indicate the beginning and duration of an access.	TTL Input
PCI_RDY	**PCI Initiator Ready.** Indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.	TTL Input
PCI_IDSEL	**PCI Initialization Device Select.** Used as a chip-select during configuration read and write transactions.	TTL Input
PCI_TRDY*	**PCI Target Ready.** Indicates the readiness of the target agent (selected device) and its ability to complete the current data phase of the transaction.	TTL Output
PCI_Stop*	**PCI Stop.** Indicates the current target is requesting the master to stop the current transaction.	TTL Output
PCI_DEVSEL*	**PCI Device Select.** When asserted LOW, indicates that the driving device has decoded its address as the target of the access.	TTL Output
PCI_PERR*	**PCI Parity Error.** Reports data parity error during any write transaction, except in a special cycle.	TTL Output
PCI_SERR*	**PCI System Error.** Reports an address parity error or data parity error in special cycle commands, or any system error where the result would be catastrophic.	TTL Output

MII Interface

Table 3 MII Interface Signals

Signal Name	Description	I/O
TX_CLK[7:0]	**MII Transmit Symbol Clock.** The physical layer provides an independent transmit nibble or symbol clock of 25 MHz for the 100-Mbps mode or 2.5 MHz in the 10-Mbps mode.	TTL Input
TXD[31:0]	**MII Transmit Nibble Data.** Transmits synchronous data with respect to TX_CLK. For each TX_CLK period in which TX_EN is asserted, the nibble TXD[3:0] is transmitted by the MII interface and accepted by the physical layer. TXD[31:28] correspondes to TXD[3:0] of port 7 MII interface. TXD[27:24] correspondes to TXD[3:0] of port 6 MII interface. TXD[23:20] correspondes to TXD[3:0] of port 5 MII interface. TXD[19:16] correspondes to TXD[3:0] of port 4 MII interface. TXD[15:12] correspondes to TXD[3:0] of port 3 MII interface. TXD[11:8] correspondes to TXD[3:0] of port 2 MII interface. TXD[7:4] correspondes to TXD[3:0] of port 1 MII interface. TXD[3:0] correspondes to TXD[3:0] of port 0 MII interface.	TTL Output
TX_EN[7:0]	**MII Transmit Enable.** Indicates that the reconciliation sublayer is presenting nibbles on the MII interface for transmission.	TTL Output
TX_ER[7:0]	**MII Transmit Error.** Signals transmit synchronously with respect to TX_CLK.	TTL Output
CRS[7:0]	**MII Carrier Sense.** The physical layer asserts one or more of the CRS[7:0] signals HIGH when either the transmit or the receive medium is not idle for the associated port (1 through 7). The physical layer deasserts one or more of the CRS[7:0] signals LOW when both the transmit and receive media are idle on the associated port (0 through 7).	TTL Input
COL[7:0]	**MII Collision.** The physical layer asserts one or more of the COL[7:0] signals HIGH upon detection of a collision on the associated port (0 through 7).	TTL Input
RX_CLK[7:0]	**MII Receive Symbol Clock.** Clock signals from the associated physical layer device.	TTL Input
RXD[31:0]	**MII Receive Nibble Data.** The physical layer transmits data on the RXD[31:0] data bus synchronously with respect to the RX_CLK[7:0] clock signals. For each RX_CLK[7:0] period in which an RX_DV[7:0] signal is asserted, the RXD[31:0] signals transfer 4 bits of recovered data from the physical layer the reconciliation sublayer. RXD[31:28] correspondes to RXD[3:0] of port 7 MII interface. RXD[27:24] correspondes to RXD[3:0] of port 6 MII interface. RXD[23:20] correspondes to RXD[3:0] of port 5 MII interface. RXD[19:16] correspondes to RXD[3:0] of port 4 MII interface. RXD[15:12] correspondes to RXD[3:0] of port 3 MII interface. RXD[11:8] correspondes to RXD[3:0] of port 2 MII interface. RXD[7:4] correspondes to RXD[3:0] of port 1 MII interface. RXD[3:0] correspondes to RXD3:0] of port 0 MII interface.	TTL Input
RX_DV[7:0]	**MII Receive Data Available.** The physical layer asserts one or more of the RX_DV[7:0] signals HIGH to indicate that data is available on the associated port (0 through 7).	TTL Input
RX_ER[7:0]	**MII Receive Error.** The physical layer asserts one or more of the RX_ER[7:0] signals HIGH for one or more RX_CLK[7:0] periods to indicate that it has detected an error somewhere in the frame on the associated port (0 through 7) presently being transferred from the physical layer to the reconciliation sublayer.	TTL Input
MDC	**Management Data Clock.** Provides the Management Data Clock for the Station Management Entity.	TTL Output
MDIO	**Management Data I/O.** Bidirectional signal that can be sourced by the Station Management Entity or the physical layer.	TTL I/O

Miscellaneous

Table 4 Miscellaneous Signals

Signal Name	Description	I/O
VDD[TBD:0]	**Power Pins.** Provide the power for the MAC8110.	Power Supply
VSS[TBD:0]	**Ground Pins.** Provide the ground connections for the MAC8110.	Power Supply
Test[TBD:0]	**Test Mode Enable Pins.** Provide a manufacturing test interface for the MAC8110 and are to be left unconnected or connected to ground.	TTL Input

FUNCTIONAL DESCRIPTION

The MAC8110 consists of the following functional blocks:

- MAC110 (10/l 00-Mbps Media Access Controller) which contains the following blocks:
  - TXFUN Transmit Function Module
  - FCNTL Full-Duplex and Half-Duplex Flow-Control Module
- STL (Status, Control and Statistics Module) which contains the following blocks:
  - STAT Statistics Module
  - SAL Station Address Logic
  - REGS Control/Indication/Status Registers
- MII
- FIFO Interface (64 bit, 66 MHz)
- PCI Interface (32 bit, 33 MHz)

MAC110

The MAC 110 module performs the Carrier Sense, Multiple Access, Carrier Detect (CSMA/CD) functions contained in the ISO/IEC 8802-3: 1993 standard and the supplement IEEE Std. 802.3u-1995 and the 802.3x for flow control. The MAC110 contains the Transmit functions, Receive functions, and the Flow Control Block.

The Transmit function accepts data from the Transmit FIFO, processes it according to 802.3, and presents the data to the physical layer device on the MII for transmission.

The Receive function accepts data from the physical layer device by means of the MII, extracts the data from the received frame, and presents the data to the Receive FIFO.

The Flow Control Module handles the full-duplex flow control frame generation and submission. In half-duplex mode, this module handles the function of jam assertion to the network as a tool for flow control.

STL

The STL Module consists of the Station Address Logic (SAL) Module, the Statistics Collection (STAT) Module, the Control and Status Registers (REGS) Module, and interfaces to the PCI Interface Module.

FIFO Interface

The FIFO Interface function was developed to give the customer the easiest way possible to access all ports from the outside without duplicating the functionality for each port separately (*Figure 2*). The interface supports a common 64-bit wide FIFO data bus for the transmit and receive bit streams on each port. These FlFOs can be addressed independently. The interface operates at a maximum data rate of 66 MHz. The control, status and statistics are handled out of band on a separate 32-bit PCI bus (RX Status optionally inband). The internal statistics counters are 32/64 bits wide, and these (in addition to the per packet statistics available) allow full MIB I and II support.

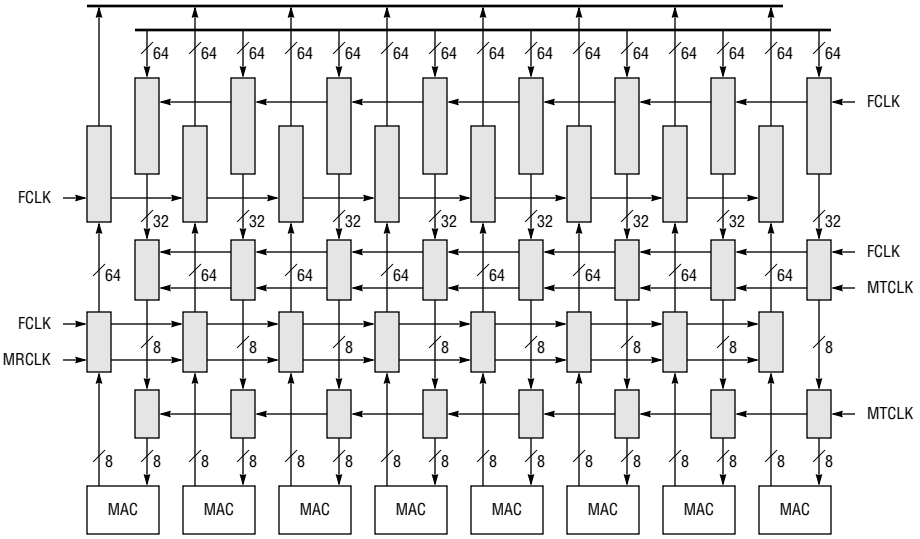

Figure 2. FIFO Structure and Data Flow

Each MAC has a pair of working FlFOs for TX and RX. The RX FIFO is 64 bits wide. The TX FIFO is byte wide internally, with a 64-bit by 8-word gateway FIFO for high speed data transfers from the bus. Programmable threshold block size is 4 and 8 data words of 64-bit width.

External signals provide a means to monitor the FIFO status through the 32-bit PCI bus. There is a transmit FIFO ready signal using the programmable threshold block size. There is a receive FIFO data present signal using the programmable threshold block size (or the EOF signal). Incomplete words are indicated with the Byte Valid signal.

The FIFO host transmit and receive data transfer process is based on a 64-bit bidirectional high-speed bus interface. Each MAC has a 3-bit address, a Device Chip Select, and TX/RX data ready indicators. All data is transferred under control of a host device using the 3-bit address.

The functional timing diagrams at the end of this document illustrate the data flow between the host device and one of the eight MAC FlFOs.

Per Port Block Diagram

Figure 3 shows the major internal blocks of each port and how these blocks interface with the FIFO Interface and the PCI Interface to the Host and with the MII to the physical layer device.

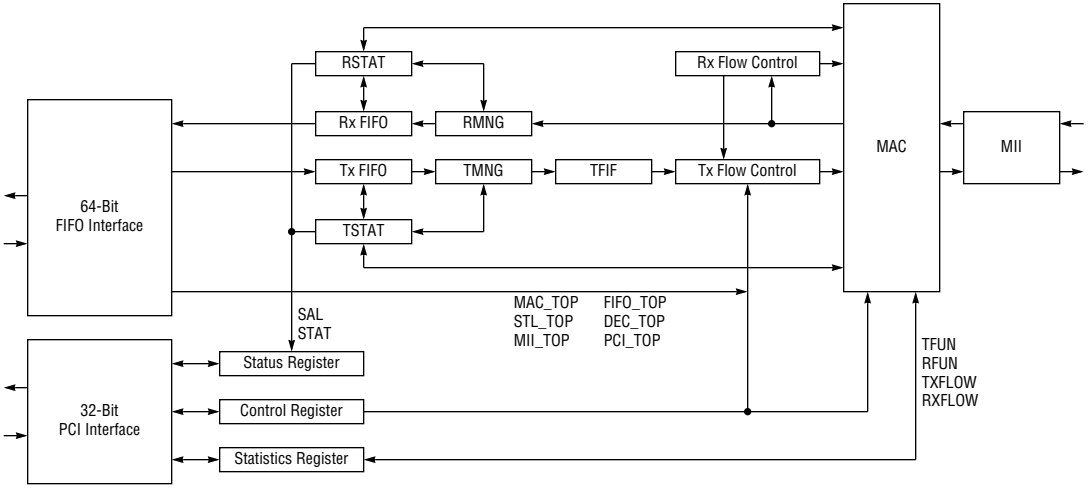

Figure 3. Module Block Diagram for the Individual Ports

REGISTERS

MAC Configuration Register (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00L		Port Active	No Backoff	LCOL-Retry	CRC-Enable	PAD-Enable	F / H-Duplex	Huge-Enable
00H	Soft Reset	LoopBack	TestMode1	TestMode0	—	—	—	—

MAC Test Register (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01L	—	—	—	—	—	—	SIMR	TTXEN

PCS Configuration Register (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02L	—	—	—	—	—	MGTCLK	ENJAB	NOCFR
02H	Soft Reset	LoopBack	TSTMD1	TSTMD0	—	—	EXINT1	EXINT0

Station Address Logic Register (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04	Soft Reset	—	TestMode1	TestMode0	—	Auto Zero	RXEN	ITXA

Station Address Logic Test Register (per port)

Register No.	Register Type	Function	Width (bits)	Direction
05	SAL Test	Station Address Logic Test Register	16	R/W

Transfer FIFO Buffer Test Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
06	TFBC	—	16	R/W
07	TFBT	—	16	R/W
08	TFBR	TFB FIFO Status Read Access	16	R
0A	TFB0	TFB Test MUX [31:0]	32	R/W
0B	TFB1	TFB Test MUX [63:32]	32	R/W
0C	TFB2	TFB Test MUX [95:64]	32	R/W
0D	TFB3	TFB Test MUX [127:96]	32	R/W
0E	THLD	TFB Hold, for loading test registers	16	R/W

Transmit Function Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
10	IPGT	Back-to-Back Interpacket Gap	16	R/W
11	IPGR	Non Back-to-Back Interpacket Gap	16	R/W
12	CLRT	Collision Window / Collision Retry Register	16	R/W
14	TBCT0	Transmit Byte Counter	32	R/W
15	TBCT1	Transmit Byte Counter	32	R/W
18	PNCT	Transmit Packet Nibble Counter	16	R/W
1A	RETX	Transmit Retry Counter	16	R/W
1B	RNG	Transmit Random Number Generator	16	R/W
1C	RNB	Transmit Masked Random Number	16	R/W
1D	ECTDC	Transmit Counter Decodes	16	R
1E	TECTCL	Test Operate Transmit Counters	16	W

Receive Function Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
21	ECRDC	Receive Counter Decodes	16	R/W
22	RECTCL	Test Operate Receive Counters	16	R/W
28	RBCT0	Receive Byte Counter	32	R/W
29	RBCT1	Receive Byte Counter	32	R/W

Receive Function Register Detail (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
21L	—	—	—	—	—	—	—	—
21H	—	—	—	—	—	—	—	—
22L	—	CLR	—	—	—	—	—	—
22H	—	INC	—	—	—	—	—	—
28L	—	—	—	—	—	—	—	—
28H	—	—	—	—	—	—	—	—

Pause Timer Counter Preload Register (per port)

Register No.	Register Type	Function	Width (bits)	Direction
31	Pause Timer	Pause Timer Register	16	R/W

10-Mbps Register (per port)

Register No.	Register Type	Function	Width (bits)	Direction
40	JBCT	Jabber Counter	16	R/W
41	DTLC	Loss of Carrier Counter	8	R/W

MII Resource Register (per port)

Register No.	Register Type	Function	Width (bits)	Direction
50	MCMD	MIIM Command Register	16	W
51	MADR	MIIM Address Register	16	R/W
52	MWTD	MIIM Write Data Register	16	R/W
53	MRDD	MIIM Read Data Register	16	R
54	MIND	MIIM Indicators Register	16	R

Statistics Resources (per port)

Register No.	Register Type	Function	Width (bits)	Direction
60	CRCE	CRC Error Counter	32	R/W
61	ALGN	Alignment Error Counter	32	R/W
62	CERR	Code Error Counter	32	R/W
63	LFRM	Long Frame Counter or Jabber Counter	32	R/W
64	SFRM	Short Frame Counter or Frame Fragments Counter	32	R/W
65	LCOL	Late Collisions Counter	32	R/W
66	EDEF	Excess Deferral Counter	32	R/W
67	MCOL	Maximum Collision Counter	32	R/W
68	FTOC	Transmit Good Frames	32	R/W
69	SCFS	Single Collision Frames	32	R/W
6A	MCFS	Multiple Collision Frames	32	R/W
6B	FROK	Receive Good Frames	32	R/W

Address Filter Register (per port)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
70	—	—	—	—	Promiscuous	MCastQ	MCast	Accept BCast

Station Address (per port)

Register No.	Register Type	Function	Width (bits)	Direction
71	SA1	Station Address	16	R/W
72	SA2	Station Address	16	R/W
73	SA3	Station Address	16	R/W

Hash Table (per port)

Register No.	Register Type	Function	Width (bits)	Direction
74	HT0	Hash Table	16	R/W
75	HT1	Hash Table	16	R/W
76	HT2	Hash Table	16	R/W
77	HT3	Hash Table	16	R/W

FIFO Bus Interface Configuration Registers (global)

Register No.	Register Type	Function	Width (bits)	Direction
90	BIFCFG	FIFO Bus Interface Configuration Register	8	R/W

FIFO Bus Interface Configuration Register (detail)

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90	—	—	—	—	RXSRM	—	Burst-Length	Burst-Length

Global Status Registers (cleared on read)

Register No.	Register Type	Function	Width (bits)	Direction
91	SPREG	Status Pending Register	32	R
92	SPTH	Status Pending Threshold Register	32	W

The Global Status registers provide the host control, process control, and status regarding the data frames transferred over the FIFO bus. A detailed explanation follows.

Global Status Pending Register (detail)

	Transmit Side								Receive Side							
Ports	Port7	Port6	Port5	Port4	Port3	Port2	Port1	Port0	Port7	Port6	Port5	Port4	Port3	Port2	Port1	Port0
SPREG	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0
SPTH	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0	B1 B0

The Status Pending Register (SPREG) has 2-bit entries for each port and for each data path (TX and RX). In the table, B1 and B0 are the bit 1 and bit 0 positions. The 2-bit value represents the number of unread status words in the port's TX or RX frame Status Register Stack. The SPREG Register is used in conjunction with a similar Status Pending Threshold Register (SPTH) which contains the stack depth at which an interrupt will be generated due to activity on the particular port and channel. B1 in the table represents bit 1 of the stack depth and B0 represents bit 0. A threshold value of zero (0) indicates a disabled interrupt condition. The maximum value of three (3) is not recommended. The output interrupt flag is the OR of all the individual port and channel interrupt conditions. Interrupt conditions are cleared by reading the respective Status Register Stacks until all stack depths have been reduced below the threshold values.

Transmit FIFO Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
A8	TFAD	Transmit FIFO Read/Write Addresses	32	R/W
A9	TFDA	Transmit FIFO Read/Write Data	32	R/W
AA	TFCT	Transmit FIFO Counter	32	R/W
AB	TFCC	Transmit FIFO Counter Control	32	R/W
AC	TFSM	Transmit FIFO State Machine States	32	R
AD	TFMS	Transmit FIFO Miscellaneous	32	R

Transmit Status Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
B0	TSRD	Transmit Status Register	32	R
B1	TSMSK	Transmit Status Mask Register	8	R/W

Transmit Status Stack Register (detail)

The Transmit Status Stack Register is three words deep per port. Only the top-level word can be written or read.

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B0LL	TXBCNT7	TXBCNT6	TXBCNT5	TXBCNT4	TXBCNT3	TXBCNT2	TXBCNT1	TXBCNT0
B0LH	COLCNT3	COLCNT2	COLCNT1	COLCNT0	LCOL	TXBCNT10	TXBCNT9	TXBCNT8
B0HL	XDEFABRT	XCOLABRT	URUNABRT	HUGEABRT	PACKDEF	BCAST	MCAST	CRC-ERR
B0HH							TXDONE	LCOLABRT

Transmit Status Mask Register (detail)

The Transmit Status Mask Register is per port and is used to filter the receive status stack entry.

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B1		TXDONE	LCOLABRT	XDEFABRT	XCOLABRT	URUNABRT	HUGEABRT	CRC-ERR

Receive FIFO Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
D8	RFAD	Receive FIFO Read/Write Addresses	32	R/W
D9	RFCT	Receive FIFO Counters	32	R/W
DA	RFDA	Receive FIFO Data	32	R/W
DB	RFCC	Receive FIFO Counter Control	32	R/W
DC	RFSM	Receive FIFO State Machine States	32	R

Receive FIFO Registers (per port) (Continued)

Register No.	Register Type	Function	Width (bits)	Direction
DD	RFMS	Receive FIFO Miscellaneous	32	R
DE	RFSM	Receive FIFO Data	32	R
DF	RFMS	Receive FIFO Data Control	32	R

Receive Status Registers (per port)

Register No.	Register Type	Function	Width (bits)	Direction
F0	RXSTAT	Receive Status Stack Register	32	R
F1	RXSTAT_EN	Receive Status Enable Register	32	W
F2	DFRAME	Receive Frame Drop Count	32	R

The Receive Status registers provide the host control process per port control and status for FIFO transfers on the receive channel. The RXSTAT register for a particular port is the output of a 3-word FIFO stack of receive frame status words, as detailed below. The RXSTAT_EN register for a particular port masks status words on input to the stack. Only status words masking to a non-zero value are actually placed in the stack. The value placed on the stack, if any, is the raw status, prior to mask. The DFRAME word for a port maintains a running count of dropped frames and is reset upon read.

Receive Status Stack Register (detail)

The Receive Status Stack register is three words deep per port. Only the top-level word can be written or read.

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F0LL	RBCT07	RBCT06	RBCT05	RBCT04	RBCT03	RBCT02	RBCT01	RBCT00
F0LH	CRCERR	DRIBBLE	CODERR	LONG	SHORT	RBCT10	RBCT09	RBCT08
F0HL	Reserved	Reserved	Reserved	CARVNT	RXDVNT	RCVOK	BCAST	MCAST
F0HH	DFC	TRFR	TRDR	OVDA	OVDR	OVTR	FLDR	SFDR

The register represents receive status as derived both from the MAC engine and subsequent I/O processing. The frame's receive byte count (RBCT10 - RBCT00), the success or failure indication (RCVOK), and other status, such as long or short packet indicators, are derived from the MAC. The upper byte count contains status about I/O processes subsequent to reception, including the reasons for the truncation or dropping of frames prior to this frame. Since multiple frames may have been dropped between successful frames, and since no status word occurs unless a frame is delivered, multiple bits may have been set and may refer to separate and/or multiple frames. The dropped frame counter should be used in conjunction with this information.

Receive Status Enable Register (detail)

The Receive Status Enable register is per port and is used to filter the receive status stack entry.

Register No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F1LL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
F1LH	CRCERR_EN	DRIBBLE_EN	CODERR_EN	LONG_EN	SHORT_EN	Reserved	Reserved	Reserved
F1HL	Reserved	Reserved	Reserved	CARVNT	RXDVNT	RCVOK	BCAST	MCAST
F1HH	CDFCT_EN	TRFR_EN	TRDR_EN	OVDA_EN	OVDR_EN	OVTR_EN	FLDR_EN	SFDR_EN

The RXSTAT_EN register for a particular port masks status words on input to the stack. Only status words with a non-zero mask are actually placed in the stack, which allows the host control and status process to limit the rate at which interrupts occur. Note that there is no mask on the receive byte count. Reserved bits should be set to zero. Changing values in this register will only affect subsequent entries to the stack.

TIMING DIAGRAMS

The following diagrams (*Figures 4-7*) show various receive FIFO interface timing scenarios.

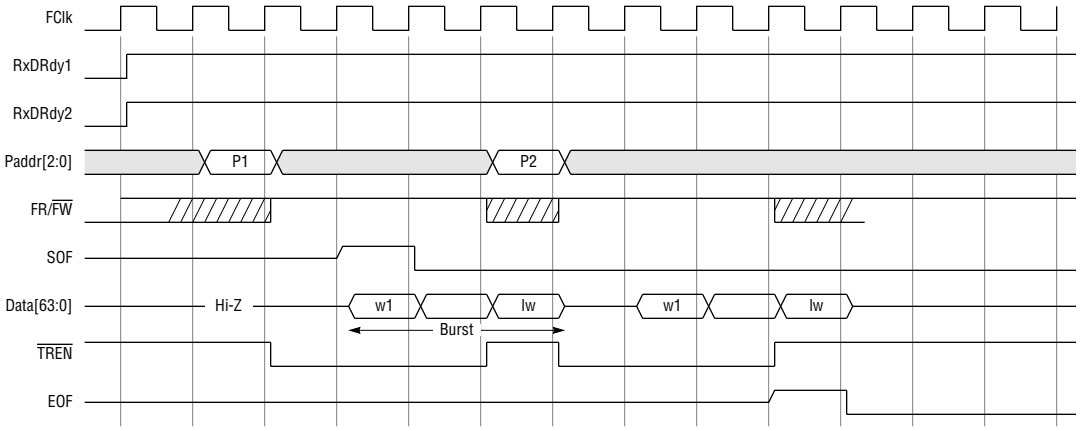

Figure 4. Receive Packet Transfer—Bus Switches from P1 to P2

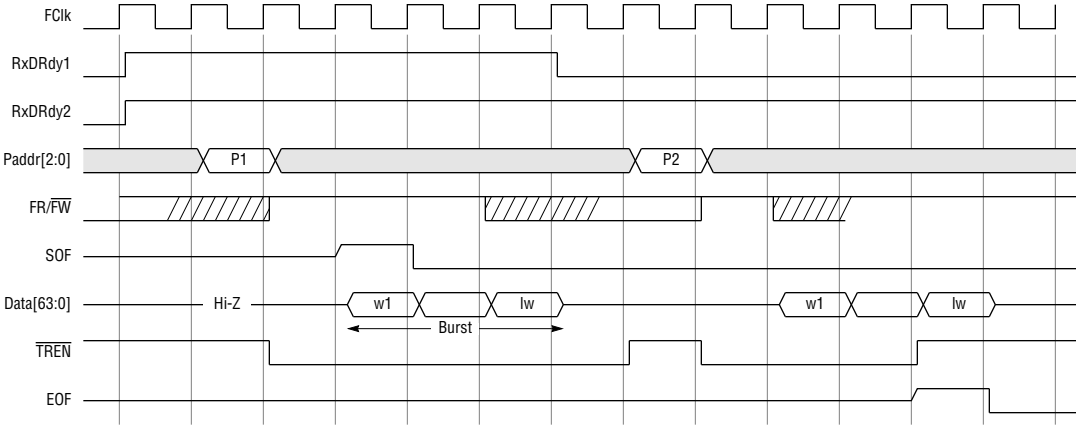

Figure 5. Receive Packet Transfer—P1 FIFO Empty, Bus Switches to P2

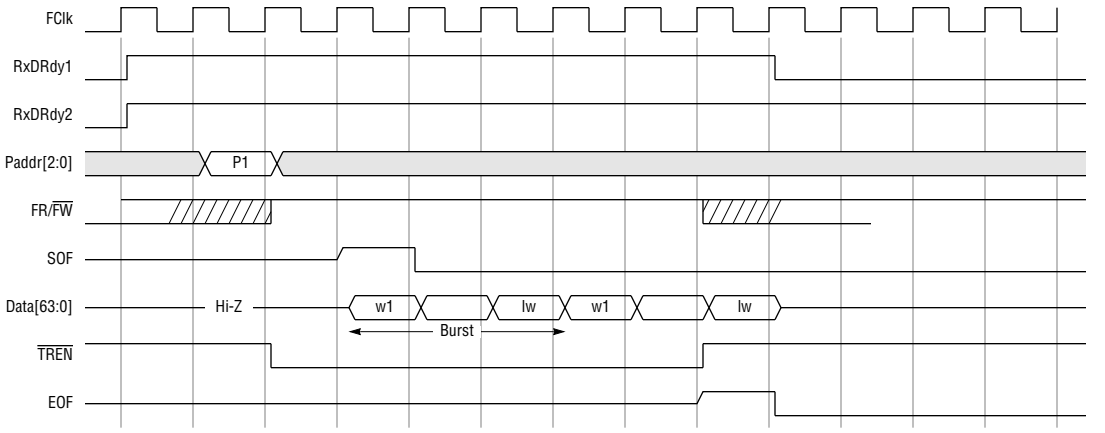

Figure 6. Back-to-back Receive Packet Transfer on the Same Port

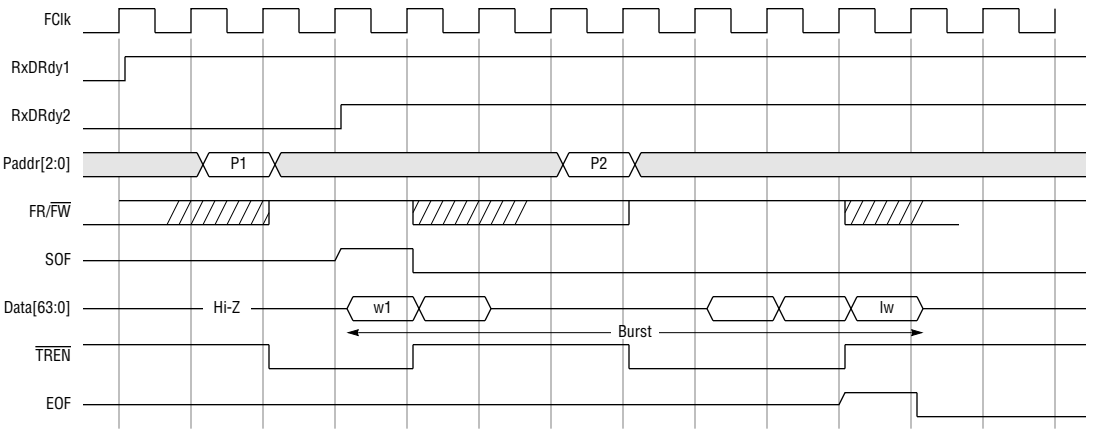

Figure 7. Receive Packet Transfer Interrupt During Burst

Notes:

Notes:

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